Intel Semiconductor Education and Research Program for Ohio

Request for Proposals (RFP)

GENERAL TERMS OF THIS REQUEST

• This request for proposal is for institutions located in Ohio.
• Responses should be provided and prepared in a format consistent with the RFP instructions provided.
• Intel Corporation reserves the right to reject any and all proposals.
• Intel Corporation reserves the right to enter into negotiations with one or more respondents to the RFP or with none of such respondents.
• Intel Corporation reserves the right to enter into a contractual or other arrangement for any or all of the proposals that are the subject of this exercise or for none of such proposals.
• All discussions and communications related to this RFP are preliminary and by no means constitute any agreement.
• Any cost incurred by any proposer to participate in the RFP is at the proposer’s expense.
• Your response to this RFP shall in no way guarantee the selection of your institution as to this Request for Proposal.
• Intel is unable to receive proposals under any obligation of confidentiality; do not submit confidential information in a proposal.
• This is a Request for Proposal only. This document is not a forecast of Intel demand for product or services or technology, nor is it an offer or a commitment to purchase products or services or provide any funding.
• All proposers must comply with all applicable laws, including export, against bribery and anti-corruption laws.
• No agency, partnership, joint venture, franchise, or employment is created between Intel and Ohio or any proposers as a result of this RFP. Neither Intel nor Ohio nor any proposer is authorized to create any obligation, express or implied, on behalf of others. No one is assuming any liability for the actions or omissions of others.
• **This RFP does not constitute or create a legally binding obligation on the part of either Intel or the proposers.**

SUBJECT

Intel Corporation, through its University Research & Collaboration Office (“URC”), requests proposals for academic research and higher-education readiness to establish the Intel® Semiconductor Education and Research Program for Ohio to enable and support Semiconductor
Fabrication in the State of Ohio. Intel intends to fund a total of $50M in grants and other investments over the next ten years. The document below outlines the key topics in which the investments will be focused.

KEY DATES

1st Information Session for Proposers:  March 24, 2022
The Intel team would be available for a conference call on 24th March, 9-10 am PST (conference call details to be shared upon request) to answer questions and provide additional clarifying information regarding the RFP. Additional information sessions (up to two more, dates TBD) may be scheduled based on requests.

Proposal Submission Deadline (PIs):  May 31, 2022 at 5pm PST
Proposal Responses from Intel:  June 30, 2022
Planned Start:  August 2022

OVERVIEW
Intel is dedicated to establishing a comprehensive collaborative program with Ohio higher education institutions to accelerate readiness and enable the workforce needed for operations of its new semiconductor fabrication facilities in the State of Ohio.

Intel invites institutions of higher education in the state of Ohio to submit proposals from academic researchers, faculty, and educators to establish the Intel® Semiconductor Education and Research Program to innovate and develop new capabilities with an emphasis on semiconductor manufacturing.

Intel would like to expand its collaboration with academia in the area of semiconductor fabrication. This may include providing resources for the creation of new curriculum for associate and undergraduate degrees, certifications, faculty training, reskill and upskills programs for existing workforce, laboratory equipment upgrades, and research that supports innovation in semiconductor fabrication.

PROGRAM SCOPE AND FUNDING
Intel intends to fund a new, collaborative, multi-institution research and education program addressing the five key topics (KT) described in detail below. We suggest that each submitting organization focus their proposal on one or two topics (in line with their primary expertise) and identify key contributions that are expected.

KT1: Curriculum Development; KT2: Faculty Training; KT3: Laboratory Equipment Upgrades; KT4: Novel Research to Advance Semiconductor Fabrication; KT5: Student Experiential Opportunities.

KEY TOPICS IN DETAIL
KT1: CURRICULUM DEVELOPMENT
GOAL: The goal of this topic is to provide resources to improve curriculum content in alignment with critical skills needed for semiconductor manufacturing. The curriculum may be targeted to relevant associate degrees, undergraduate degrees, certifications, or reskill/upskilling programs that enable workforce retraining. Curriculum content may include measurement of effectiveness of the training.

Examples of desirable curriculum content are the following:

- Fundamentals of Semiconductor Device Fabrication and Processing including the following:
  - Introduction to semiconductor industry, semiconductor device physics, transistor technology, process technology, and volume production
  - Silicon and wafer preparation, chemicals in semiconductor fabrication
  - Contamination control in wafer fabs – particles, metallic impurities, organic contamination, native oxides, electrostatic discharge
  - Basics of IC fabrication process workflows – diffusion (oxidation, deposition and doping, lithography, etch, thin films, ion implantation, and polish, planarization, wafer test, assembly and packaging)
    - Lithography, both traditional photolithography and more recent patterning technologies such as directed self-assembly
    - Semiconductor Deposition Processes such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and atomic layer deposition (ALD)
    - Semiconductor Removal Processes such as dry etch with plasma, wet etch, and chemical-mechanical planarization (CMP)
    - RF circuits, power supply tuning, safety
    - Basics of Implant and Diffusion in Semiconductor Processing
    - Semiconductor metrology including optical microscopy, electron microscopy, ellipsometry, and other relevant spectroscopy techniques
    - Wafer test – in-line parametric test, wafer sort, yield, wafer sort yield models
    - Basic understanding of Statistical Process Control for semiconductor manufacturing, tool matching and calibration, data modelling, linear regression
    - Understanding of Clean Room Environment – humidity and temperature control, HEPA filters, air turbulence, sources of contamination and prevention
  - Advanced Process Control

- Manufacturing Science
  - Factory physics
  - Capacity planning and modeling
  - Production planning, scheduling and control (WIP management)
  - Semiconductor manufacturing complexity and operational optimization
  - Design for Manufacturability (DFM) and for Cost (DFC)

- Equipment operation and maintenance fundamental skills such as:
  - Vacuum System Basics, Pneumatics, Robotics troubleshooting and repairs, Power Supply/Electronics troubleshooting and schematics reading, 3D model piping, gas line schematics, electrical systems, mass flow controllers (MFCs), Industrial Hand tools overview, i.e., calibrated torque wrenches, cleanroom protocols, etc.
o Tool qualification, troubleshooting, preventive maintenance
o Understanding tool availability and uptime, and impact to factory performance and efficiency
o Technical specification (work procedure instructions) writing, writing procedures; follow chain of command, manufacturing culture

- Hand Tools, Safety, Ergonomics, Skills for Wellbeing, Statistical Analysis, Basic Schematics
- Experiment Design, Measurement & Data Collection, Data Analysis & Visualization
- Circuit Design, Digital Design, VLSI, Pre and Post-Silicon Validation
- Automation, Smart Manufacturing Technology
- Sustainability best practices in any of the above topics, and including water treatment/recycling, abatement systems, etc., to align with Intel’s sustainability goals [1].
- Social and career growth skills such as Problem Solving & Design, Critical Thinking, Computational Thinking, Social Perceptiveness, Leadership, Organizational Skills, Leadership and Communication skills.

A select number of **Manufacturing Internship Opportunities (MIOs)** for students at Intel fabs and labs with emphasis on gaining real-world experience in the areas highlighted above may be available and should connect with KT2, KT4, and/or KT5.

Curriculum developed under this initiative is intended to be provided to the academic community with open access over several years:

- In contributing funding to this proposal, Intel requests that the content hosted on institute, university or faculty websites allows the broader academic community to access content to incorporate into their respective course syllabuses.
- Intel requests that faculty allow Intel the right to host their course content link and associated course description on an Intel website (or Intel designated website) and on college/university program websites.
- Intel requests that faculty allow Intel the opportunity to review course content prior to publication of the material for sharing within the broader academic community.

Proposals that have identified paths to disseminate curriculum within the broader academic community through workshops, conferences and other collaborative associations are of considerable interest. Proposals that include adapting existing and/or designing new curriculum (on the key topics listed above) for virtual learning environments, including flexible delivery of courses (e.g., online, synchronous, in-person, hybrid, etc.) are strongly encouraged.

Curriculum developed under this initiative should be piloted in a classroom setting at the college or university. Proposals have flexibility to identify the most appropriate course intercept for the targeted material based on course teaching imperatives and prerequisites. This RFP specifically targets associate’s degree and undergraduate level courses.

**KT2: FACULTY TRAINING**

**GOAL:** This KT aims to improve the skills and experiential programs for faculty that will deliver new curricula content. This KT aims to support programs and training methodologies to foster long-term collaborations between universities and community colleges. A reciprocal exchange of expertise between educators, faculties, and researchers is envisioned. The educators, faculties, and researchers should work together to identify best teaching, training, and pedagogical
methodologies to deliver content developed herein, and highlight programs such as faculty exchange/sabbatical programs, faculty authored trainings, workshops, conferences, train-the-trainer programs, etc., to further strengthen partnerships between community colleges and universities. Proposals that support diverse participation will be given significant consideration.

Examples of desirable training topics:

- New curriculum content training (on topics listed in KT1)
- Semiconductor Fundamentals, Principles of Semiconductor Devices
- Thermodynamics and Transport Process in Semiconductors
- Electronic, optical, magnetic properties of materials
- Characterization of Semiconductor Materials, Metrology, Semiconductor Fault Isolation and Failure Analysis
- Microelectronics and Packaging
- Semiconductor fabrication processes, safety and cleanroom protocols.
  - Beyond the basics on reducing contamination (contamination control), e.g., clean rooms and bunny suits, we would like to encourage students to learn about hazardous materials and energies, e.g., HF and chemical handling and hazardous energies, and efforts to reduce them with new research into mitigation and abatement of these chemicals.
- Advanced Process Control
- Fundamentals of Machine Learning and Artificial Intelligence, especially in its application to semiconductor fabrication
- Computer vision, sensing techniques, robotics, human-machine interaction, social aspects of automation, interdisciplinary component of responsible design and use of data and AI (see Resources section for more details on Intel’s Digital Readiness Program [2] and IEEE ICICLE Program [3])
- Semiconductor design practices and methodologies. Intel may provide process design kits (PDKs) and support to select faculty and students in advanced engineering studies to practice and gain hands-on experience in the design of semiconductors, the utilization of foundry tools, or on designs using an Intel shuttle.

To support student MIOs, corresponding instructors, educators or faculty may have the opportunity to tour an Intel fab or lab physically or virtually for student’s MIO.

**KT3: LABORATORY EQUIPMENT UPGRADES**

**GOAL:** This KT may include financial resources to upgrade compute and laboratory equipment to enable changes or new curricula topics associated with KT1 and training programs included in KT2. Proposals in KT3 should include details on how these equipment upgrades will help further topics in KT1 and KT2. If multiple universities and colleges are involved, the proposal should clearly highlight which of these resources will be shared, and who the beneficiaries of these resources would be.

Examples of Laboratory Equipment upgrades:

- Computation hardware
- Lab scale metrology and fabrication equipment for semiconductor materials and devices
- Safety equipment critical in semiconductor fabrication

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1 Note, Intel’s separate University Shuttle Program is an invitation-only program unrelated to this RFP.
- Software or licenses needed for the operation of laboratory equipment
- Upgrades at the university level, e.g., to shared-user facilities, may be considered if it is shown that they would significantly improve the ability of the academic institute to better enable curricula and research aligned with KT1.

Intel’s Academic Compute Environment (ACE) Resources [4] may be available upon request.

**KT4: NOVEL RESEARCH TO ADVANCE SEMICONDUCTOR FABRICATION**

**GOAL:** This KT aims to advance the state of semiconductor fabrication in areas such as novel materials, beyond-CMOS digital logic technologies and heterogeneous design integration, and other areas in support of KT1 Fundamentals of Semiconductor Device Fabrication and Processing.

Examples of desirable outcomes for this KT:

- Materials Research into new photoresist materials needed for next-generation high-NA EUV photolithography that push the limits of current photoresist resolution, sensitivity, and line-edge roughness
- Materials Research enabling new materials for newer patterning technologies
- Novel ALD precursors and techniques with improved selectivity such as area-selective ALD (AS-ALD) and higher throughput, e.g., spatial ALD (SALD)
- Reduction of environmentally unwanted chemicals typically used in semiconductor fabrication through discovery of more benign substitutes or abatement techniques
- Design for materials recovery and recyclability, reverse supply chain management
- Materials Research for new backend on-chip interconnect materials beyond Cu for ultra-scaled interconnect lines, including novel elementals metals, alloys, 2D materials, and liners with realistic paths to integration
- Silicon-based photonics
- Heterogenous design and integration
- New electronic packaging materials that enhance power and performance of finished semiconductor devices
- Disruptive materials and methods including 3D-printing for packaging, new deposition techniques, CNT interconnects and/or transistors, and 2D materials for front-end or back-end applications
- Novel Semiconductor metrology techniques with high throughput and for ultra-scaled dimensions below 10nm for defect detection, failure analysis, and assessment of device and interconnect yield
- Novel application of machine learning and AI for Process Control for semiconductor manufacturing
- Novel device integration for both frontend and backend devices, including backend memory options
- Social scientific, managerial, and/or policy research on approaches to ensuring shared prosperity and equitable social outcomes in the context of automation
- Human-machine interaction approaches to amplifying human potential in a semiconductor manufacturing context.

**KT5: STUDENT EXPERIENTIAL OPPORTUNITIES**

**GOAL: IMPACTFUL OPPORTUNITIES TO ENHANCE STUDENT EDUCATION**

In all of the above key themes it is possible to create an experiential opportunity that enhances student education and allow “learning by doing,” for example, through the proposed MIOs.
would like to enable programs that support students’ hands-on activities that enhances their education. The selection of students may be done on the basis of academic achievements and ensure a diverse cohort of students.

Examples of student programs:

- Graduate research grants
- Undergraduate research experience
- Undergraduate and Associates semiconductor summer boot camps
- Manufacturing Internship Opportunities (MIOs)
- Reskill and upskill training opportunities (see KT1)
- Returning workforce training opportunities (see KT1).

A select number of Manufacturing Internship Opportunities (MIOs) for students at Intel fabs and labs with emphasis on gaining real-world experience in the areas highlighted in the fundamentals of semiconductor processing in KT1 are anticipated to be available. Internship programs may target associate, undergraduate, and graduate level students. Intel anticipates communicating the availability of these opportunities early in the academic year.

KT5 is intended to be part of KT5s 1-4, and not intended as a stand-alone submission. Proposals may include three KT5s if KT5 is included (please see FAQ).

**FUNDING DETAILS**

Intel anticipates allocating cumulative funds of $5M per year across the different KT5s for three years for this RFP call. In Year 1, the majority of the funds (~60%) are anticipated to be allocated to KT3 and KT4, and the remaining (~40%) may be distributed across KT5s 1, 2, and 5. Please note that funding for KT5 is anticipated to be available only in Year 1. For Years 2 and 3 of this program, ~25% of the funds may be allocated to KT4, ~40% for KT5 (including MIOs), and the remaining 35% may be distributed across KT5s 1 and 2.

Intel anticipates funding ~5-10 proposals starting FY2022, subject to the availability of funds, the quality of the proposals and coverage of KT5s. This allocation is subject to change.

<table>
<thead>
<tr>
<th>Key Topics (KT)</th>
<th>Approximate Anticipated Funding Allocations²</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>July 2022</td>
</tr>
<tr>
<td>KT1: Curriculum Development</td>
<td>15%</td>
</tr>
<tr>
<td>KT2: Faculty Training</td>
<td>15%</td>
</tr>
<tr>
<td>KT3: Laboratory Equipment Upgrades</td>
<td>30%</td>
</tr>
<tr>
<td>KT4: Novel Research to Advance Semiconductor Fabrication</td>
<td>30%</td>
</tr>
<tr>
<td>KT5: Student Experiential Opportunities &amp; IMO</td>
<td>10%</td>
</tr>
<tr>
<td>Total</td>
<td>100%</td>
</tr>
</tbody>
</table>

² Based on proposals and coverage of different KT5s, Intel may adjust the funds allocated across the different KT5s (subject to fund availability).
PROPOSAL FORMAT

Please note that Intel is unable to receive proposals under an obligation of confidentiality. All proposals submitted should therefore include only public information.

Proposals should be 4-8 pages, not including citations or cost volume. We prefer proposals that aim at defining projects for up to three years. We want to encourage institutions to submit a single proposal with several Principal Investigators (PIs) rather than multiple proposals submitted by individual PIs. We also encourage multiple institutions to partner in the creation of proposals; for example, structuring collaborative agreements that enable networks or hub and spoke models of collaboration.

Collaborative proposals between PIs with complementary domain expertise are also encouraged; for example, one PI with expertise in silicon circuit design may collaborate with another PI on novel semiconductor materials. An individual researcher, educator, or faculty can be the lead PI on only one proposal but may be a co-PI or senior investigator on other proposals.

Each proposal should comprise the following sections:

- **Proposal cover page (max 1 page)**
  - Organization
  - List of PIs and the main contact person
  - List one or at most two targeted key topics
  - Executive summary including intended outcomes. Summarize the key elements of the proposal.

- **High-level motivation, preliminary results, approach, and proposed goals (<= 3 pages).**
  Briefly describe the motivation for the proposed project, preliminary results, techniques (especially novel ones) that underpin the approach, and the plan of tackling the proposed key topics. Summarize what will have been accomplished after 3 years if all goes according to plan. Be sure to detail the current state of the art for the proposed technology (or nearest related technologies). If applicable, this section must also include an explicit statement of the Intellectual Property (IP) status for all background IP related to this technology (i.e., are the property rights to this technology protected, and if so, who owns those rights).

- **Statement of work, schedule, milestones, success criteria and deliverables (<=1 page).**
  For each of the goals addressed, outline the 3-year scope of the effort including tasks to be performed, schedule, milestones, deliverables, and success criteria. It is understood that aspects of the program’s effort may be exploratory in nature and schedules/deliverables reflect intentions rather than a firm commitment.

- **Potential for scalability.** Proposals that have identified paths to disseminate curriculum within the broader academic community through workshops, conferences and other collaborative partnerships will be given significant consideration (e.g., multiple course offerings, number of students impacted, adoption by other universities/organizations, online course offerings, participation in relevant education conferences/workshops).

- **Personnel plan and expertise statement (max. 1/4 page per Researcher).** Include a list of key personnel plus a statement on each person’s role and time commitment. For each person, please add a brief bio or web page link and list their 6 most relevant prior publications (within the last 8 years) for the selected research questions.

- **Student plan (<1 page).** Please provide information about the students and postdocs you envision to assign to this project (if known). Outline the approach and plan whereby
students will be recruited and incorporated into the team, and any plans for encouraging/supporting those students in projects for Intel (e.g., availability for internships should a mutually interesting opportunity arise). If the PIs have a pre-existing relationship and history of student hiring by Intel, please discuss issues/plans/ideas to continue or strengthen that connection.

- **Diversity and Inclusion (<1 page).** Intel is committed to advancing diversity and inclusion (D&I) at every level in our company and the broader industry. It is foundational to our business and purpose, as outlined in the Intel RISE 2030 (CSR) strategy [1]. In alignment with these core values, please address the following: (a) Your organization’s commitment to D&I with respect to race, national origin, gender, veterans, individuals with diverse abilities and LGBTQ, (b) A summary of your performance in this area and any initiatives you are pursuing, and (c) Metrics defined to track inclusive and diverse practices within your proposal.

- **Prior Intel Collaborations (max 1/3 page per project).** If you collaborated with Intel in the past, please list the project/institute, the year, and the main contact(s) at Intel. Furthermore, add a short abstract outlining the scope.

- **Past Successful Teaching and/or Training Program Implementations and/or Technology Transfers (<1 page).** The extent to which expertise and prior experience bear on the problem at hand. Elaborate on relevant experience in the targeted domain and any notable teaching and training recognitions. Evidence of past successful industry collaborations, curriculum implementation and technology transfers. Examples include startups, products, and other evidence of tangible business impact of the involved academics.

- **Budget and Financials (1/3 page).** Typical grants are USD$200K-1M per year for three years. We plan to work under an open intellectual property model (results are published and to be in the public domain, code is open sourced). Our goal is to maximize the available funds for our fixed amount of total funding. Universities may propose how to achieve this. Please also indicate how many researchers (FTE) can contribute their research for the proposed funding.

- **IP-compatible funds amplification (no limit).** If the team can obtain funding for related work from other sources (including the University) and the sponsor commits to follow a public dedication approach (to the public domain) for that project or provide Intel with non-exclusive, royalty-free research and commercial licenses to any IP, the team may list funding that would be considered to amplify the proposed project.

- **Citations {unlimited}.**

- **Cost volume {unlimited}.** Cost proposal in Excel or another format as appropriate.

- **File format.** Proposals may be submitted either as a Word document or pdf. The file name must be in the following format:
  - `<KT#>.<ABC University>.<Last Name of Lead PI>
  Example: KT1.2.5.ABC University.Smith`

**EVALUATION CRITERIA**

In order of importance, the evaluation criteria for this Request for Proposals are as follows:

1. **Potential contribution and relevance to Ohio, Intel, and the broader industry:** The proposed programs should directly support a solution that addresses the KTs outlined above, leading to student preparation, laboratory upgrades or technological advances with the potential for ongoing technology transfer in collaboration with Intel and the broader industry.
2. **Technical Merit:** The extent to which the proposed curriculum and training methodologies are feasible to address the targeted teaching and training imperatives. Proposed solutions of interest should clearly push the boundaries of technical innovation and advancement. Feasibility of new algorithms/techniques should be demonstrated through SW/HW implementations.

3. **Clarity of overall objectives, intermediate milestones and success criteria:** The proposed Program Plan should clearly convey that the PIs have the knowledge and capability to achieve the stated goals. It is understood that any program will have uncertainties and unanswered questions at the proposal stage, but a clear path forward in key challenge areas must be identified and justified. Teams are expected to demonstrate progress toward project goals at quarterly milestones and monthly project status updates. As detailed in the “Program Scope and Funding” section, the proposal should explicitly point out which KT is being addressed, the synergy among them if more than one KT, the plan and milestones towards building research prototypes, plan for ongoing technology transfers, and the anticipated proof of concept outcome. Strength of project management will also be considered.

4. **Qualifications of participating researchers, educators or faculty:** The extent to which expertise and prior experience bear on the problem at hand. Please elaborate on track records of building new curriculum, producing effective training materials, teaching experience, building research prototypes (e.g., open-source research code/collaterals on GitHub) and resulting publications from past relevant projects.

5. **Potential for scalability:** Proposals that have identified paths to disseminate curriculum within the broader academic community through workshops, conferences and other collaborative partnerships will be given significant consideration (e.g., multiple course offerings, number of students impacted, adoption by other universities/organizations, online course offerings, participation in relevant education conferences/workshops).

6. **Cost effectiveness and cost realism:** The extent to which the proposed work is both feasible and impactful within the proposed resource levels will be examined.

7. **Potential for co-funding:** Opportunity for closely synergistic matching grants and co-funding with other funding entities, such as SRC, NSF, DARPA, NSERC, etc., and/or leveraging existing funding will be given significant consideration.

8. **Potential for broader impact:** As an industry leader, Intel pushes the boundaries of technology to make amazing experiences possible for every person on earth. From powering the latest devices and the cloud you depend on to driving policy, diversity, sustainability, and education, we create value for our stockholders, customers, and society. Intel expects the academic community to be strong partners in making Intel successful through support of Intel’s goals and commitments to diversity, sustainability, and education. Intel supports the advancement of computing education and diverse participation in STEM. Significant consideration will be given to proposals in which the outcome of the program and research can influence the development of new curriculum initiatives impacting associates, undergraduate or graduate education at the respective colleges and universities (e.g., exposure to latest industry technologies/tools in classroom setting). Proposals are encouraged to elaborate on how the proposed work is anticipated to impact student education on campus and/or the broader academic community.
Proposals that support diverse participation in engineering education and prioritize sustainability in line with Intel’s RISE 2030 goals [1], will be given significant consideration.

**PI MEETINGS AND COLLABORATION STRUCTURE**

Intel personnel would be deeply engaged with the Intel® Semiconductor Education and Research Program for Ohio and may assign partner technologists/collaborators across KTs to interact with the academic community to produce a stream of capable students, innovation proof points, publications, demonstrations, and technology transfers into Intel and the broader industry throughout the duration of the program. We aim for the interaction to be bi-directional where Intel collaborators are part of the program or research team. Not only would they provide feedback, but they may also actively contribute and co-develop the research to amplify the program outcome and enable continuous workforce and technology transfers into Intel and the broader industry.

It is expected that the PI and student researchers will collaborate on a daily or weekly basis. Monthly PI, student, and Intel collaborator meetings will be used to review research results, present significant updates, and provide feedback.

Semi-annual face-to-face or virtual meetings will be held to facilitate program-wide information exchange, review, and discussion of research. Researchers and Faculty should anticipate one annual face-to-face meeting to be held at an Intel site in the US and one annual face-to-face meeting to be held at a university associated with this program. Associated travel costs for two annual meetings should be considered and included in the proposed budget. In the event unexpected travel restrictions prohibit a face-to-face meeting, a virtual meeting will be held.

To aid in collaboration across projects within the program and communication of program findings to the public, it is anticipated that a program website will be established, hosted, and maintained, and Intel requests the right to host the associated website link on their respective university program websites.

Intel may offer free access to Intel’s Academic Compute Environment [4], a resource for academia researchers in the program to exercise their workloads on Intel’s latest hardware.

For those researchers who are already funded and seek collaboration opportunities with Intel and other researchers in the area of this RFP, please let us know. One option is to participate in program activities (e.g., seminars, workshops, and hardware access) without Intel funding.

**ELIGIBILITY**

This request for proposal is only for institutions in Ohio. Proposers may freely select additional academic collaborators; however, the lead institution must be an institution from the state of Ohio (please see FAQ for clarification). Any questions regarding eligibility should be directed to Gabriela Cruz Thompson or Sowmya Venkataramani (contact info below).

**INTELLECTUAL PROPERTY**

This Request for Proposals affords proposers the choice of submitting complete program proposals for the award of a gift, grant, Sponsored Research Agreement, or other agreement as appropriate. Intel reserves the right to negotiate the final choice of agreement.

The final award terms are expected to follow a public dedication model, which is Intel’s preference. Therefore, Intel and the higher education institution will jointly agree that all academic curriculum and research in the program be placed in the public domain (all IP, including,
patentable inventions dedicated to the public and source code distributed under an open-source license similar to the Apache, BSD or MIT license).

**INTEL TEAM CONTACT INFO**
The following individuals from Intel Labs are actively involved with the creation of this program.

- Gabriela Cruz Thompson, University Research and Collaboration Director, gabriela.cruz.thompson@intel.com
- Sowmya Venkataramani, Program Director, University Research and Collaborations, sowmya.venkataramani@intel.com

Please send proposal submissions and related inquiries to both Gabriela Cruz Thompson and Sowmya Venkataramani. Please include “Submission for “Intel® Semiconductor Education and Research Program for Ohio” in the Subject of your email.

**FAQ**

**What is the typical grant size?**

Proposals generally request grants in the range of $200K -1M per year, largely dependent on the KT's being addressed. All proposals must justify the proposed budget in terms of the resources needed to carry out the proposed work.

**What is the envisaged project duration?**

Three years (There is a renewal process each year. Proposals should outline all 3 years with more details on year 1.) Intel expects to release a second and third call for proposals in 2024 and 2026. At that time, some programs may be renewed, and KT's may be modified to meet the needs in the future.

**Can you specify which researchers have been invited to this RFP?**

We don’t release the names of invited researchers. Keep in mind that if you are seeking to partner with a specific academic PI, your partners do not have to be invited; you can choose to partner with any PI and share the RFP with them.

**Can a proposal include more than one key topic (KT)?**

Each proposal can include one or two KT's at the most, if including KT's 1 through 4. However, proposals can include three KT's, if KT5 is included as the third topic, supporting the other KT's. For example, a proposal containing KT1, 2, and 5 is acceptable, but a proposal containing KT1, 2, and 3 will be rejected. KT5 is not a stand-alone topic for funding, proposals addressing only KT5 will be rejected.

**Does the lead PI submitting a proposal need to be a faculty Member in a university?**

The lead PI need not necessarily be a faculty member in a university; they could be a researcher, or educator, affiliated with a college or university based in Ohio.

**Can you specify who can submit proposals?**

This RFP call is open to all Ohio based institutions, and proposals can be submitted in one of the two ways listed below:
“Single Institution Submission:” Faculty members, researchers, and educators from the same Ohio-based institution are encouraged to collaborate therewithin and submit a single proposal from that institution.
“Multi-Institution Submission:” (1) Faculty members, researchers, and educators from different institutions based in Ohio may submit a multi-institution proposal. Any of the collaborating institutions can submit the proposal as the lead institution. (2) Faculty members, researchers, and educators from Ohio-based institutions are encouraged to collaborate with PIs from institutions outside of Ohio; however, the lead PI and the lead institution submitting the proposal must be from an Ohio-based institution.

Are we encouraged to seek co-funding opportunities?
While co-funding is not required, a proposal with co-funding or matching funding would be a strong plus.

As an outcome of this RFP, will there be a physical space created for the PROGRAM?
Intel® Semiconductor Education and Research Program for Ohio is envisioned as a comprehensive collaborative program for a group of higher education institutions to work together in their existing space to innovate and develop new capabilities with an emphasis on semiconductor manufacturing. Building of a physical space to house this collaborative program is outside the scope of this RFP call.

RESOURCES