

Industry Recognizes Node Naming Inconsistency



"The picture the semiconductor technology node system paints is false. Most of the critical features of a 7-nm transistor are actually considerably larger than 7 nm, and that disconnect between nomenclature and physical reality has been the case for about two decades."

Samuel K. Moore



"We believe Intel 10SF is competitive with TSMC 7nm. I would expect Intel 7nm to be competitive with TSMC 3nm and Intel 5nm to be competitive with TSMC 2nm."

Scotten Jones

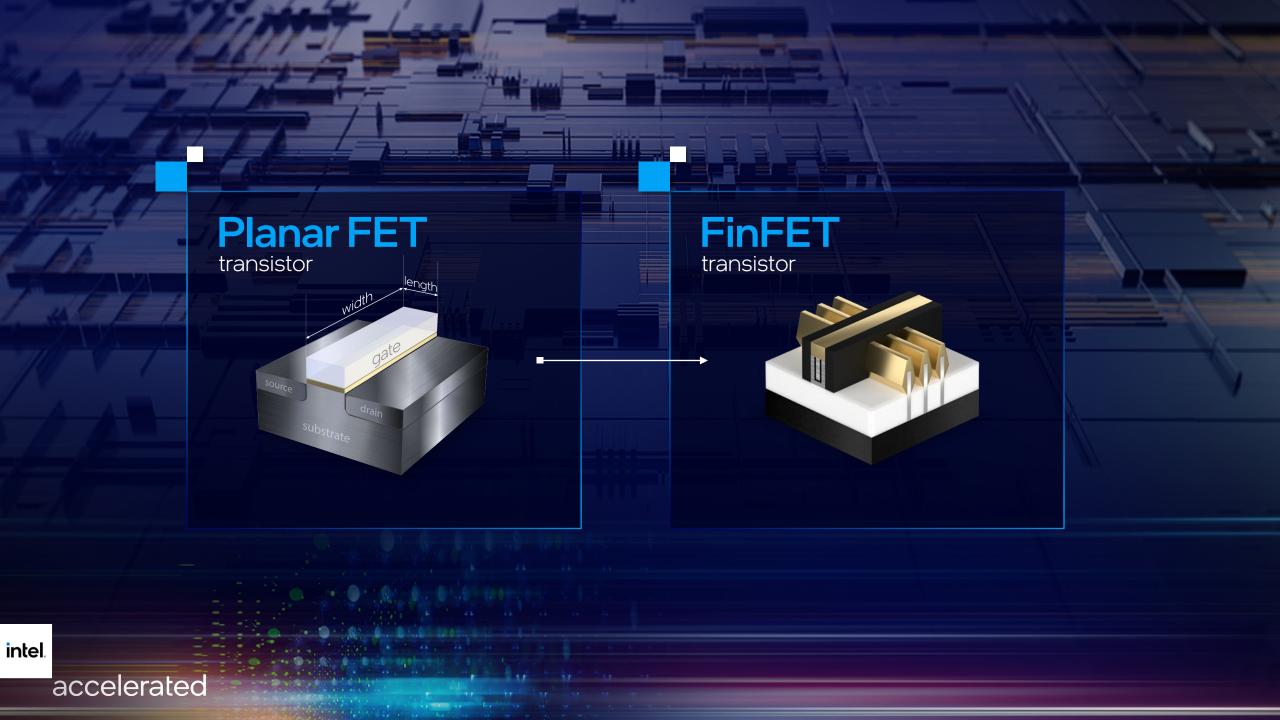


"Samsung and TSMC have made it to 7nm — roughly the equivalent of Intel's 10nm — and both are now actively pushing to 5nm and 3nm. But logic density will only carry a design so far."

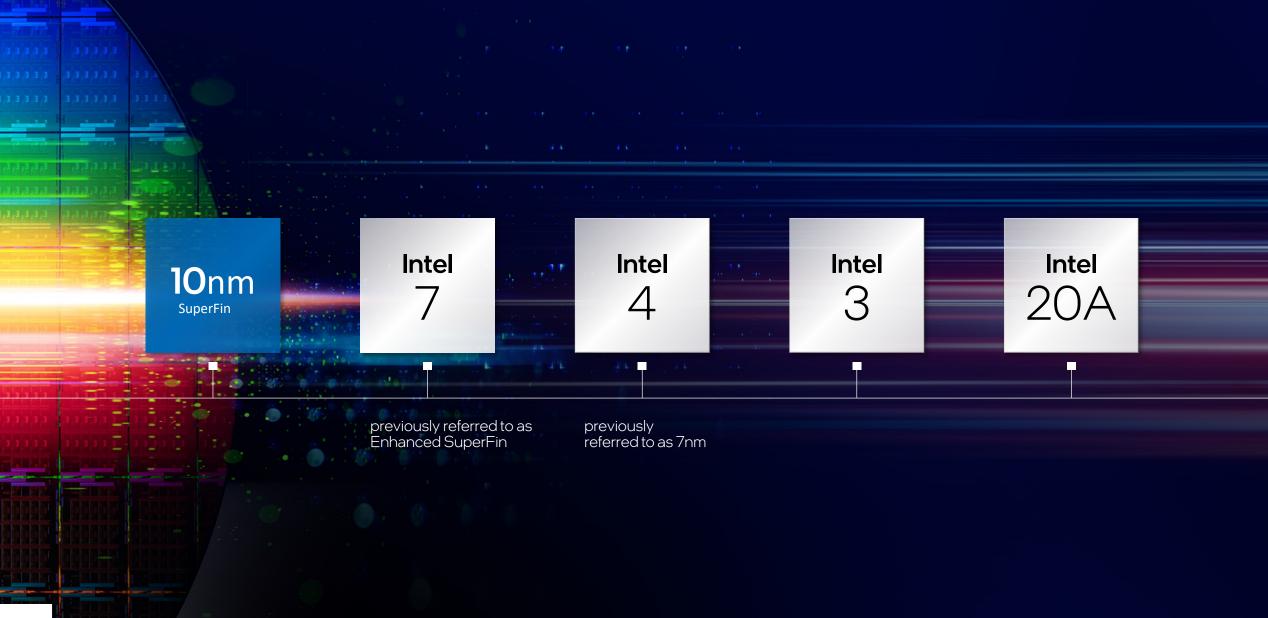
Ed Sperling

"Today these numbers are just numbers. They're like models in a car...
it's just a designation for the next technology node....
So let's not confuse the name of the node with what the technology actually offers."

Philip Wong
VP of Corporate Research TSMC, Hot Chips 31 Keynote







intel.

accelerated

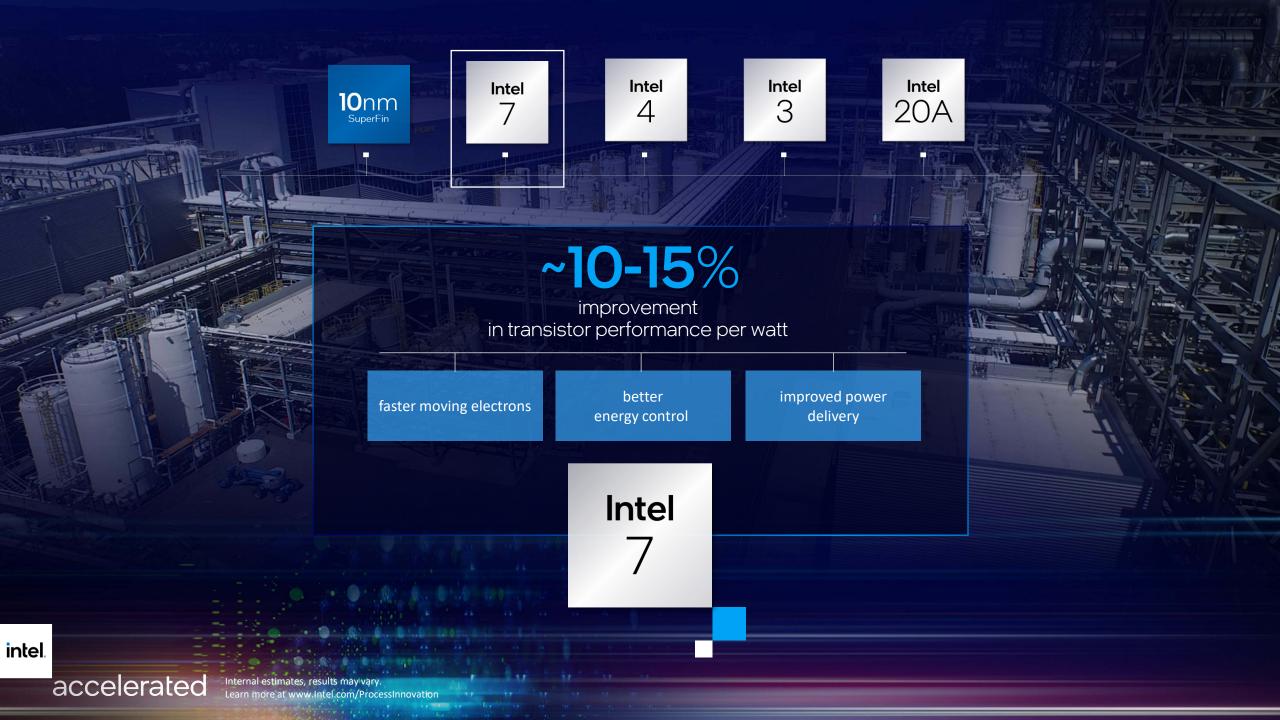
www.Intel.com/ProcessInnovation

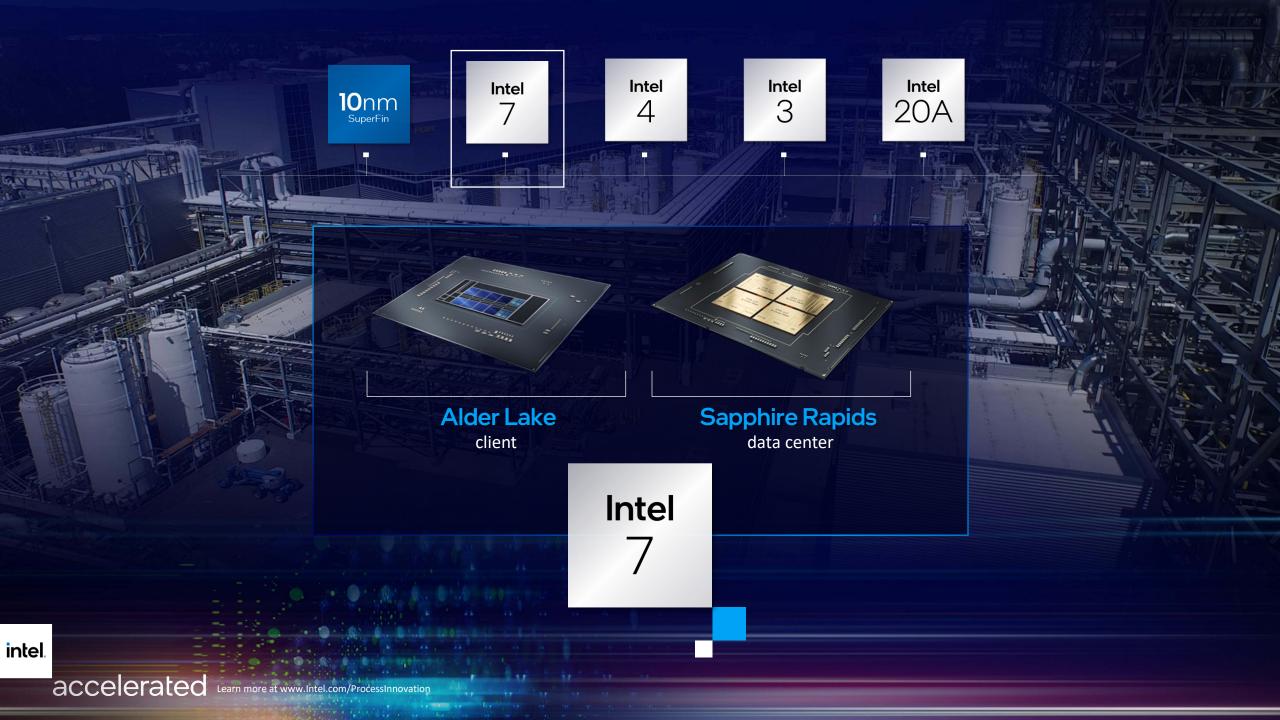
the angstrom era of semiconductors Intel accelerated

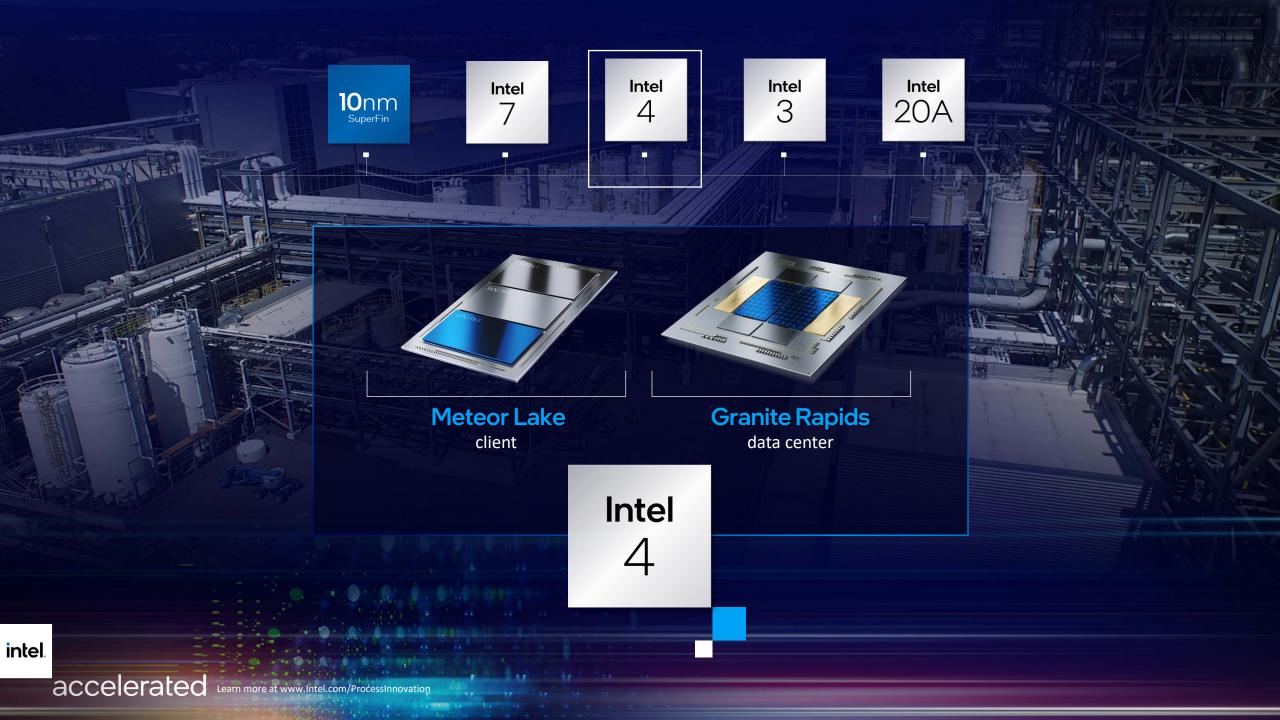
intel.



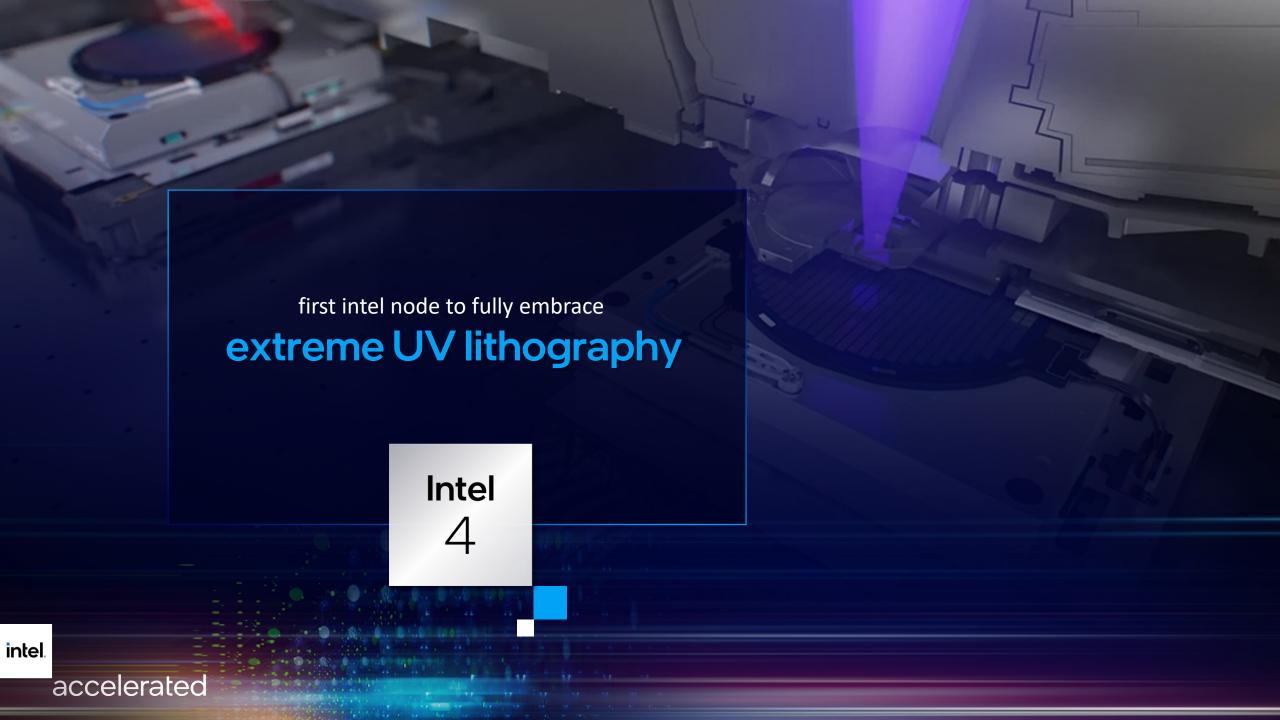








Meteor Lake taped-in client compute tile Q2 2021 Intel intel. accelerated



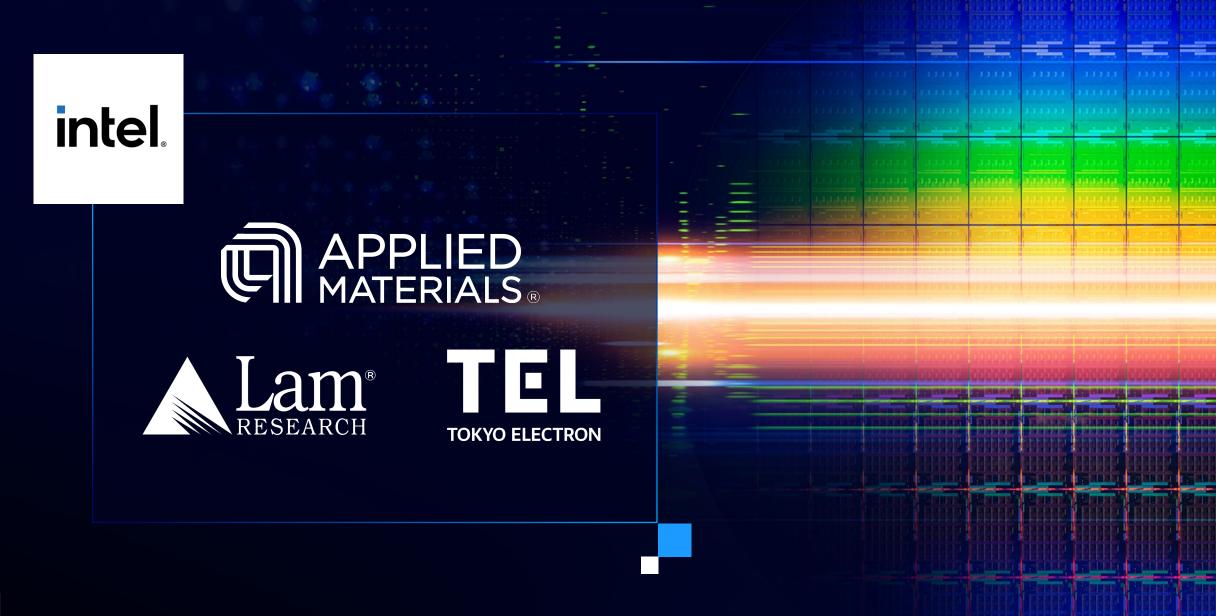


ASML

"Together, Intel and ASML are on the leading edge of Extreme UV lithography technology. As Intel expands its global fab network, we stand ready to supply the cutting edge EUV tools that will contribute to future innovations. We're especially excited about the next generation High-NA EUV tools, which will enable even greater advances in silicon technology."

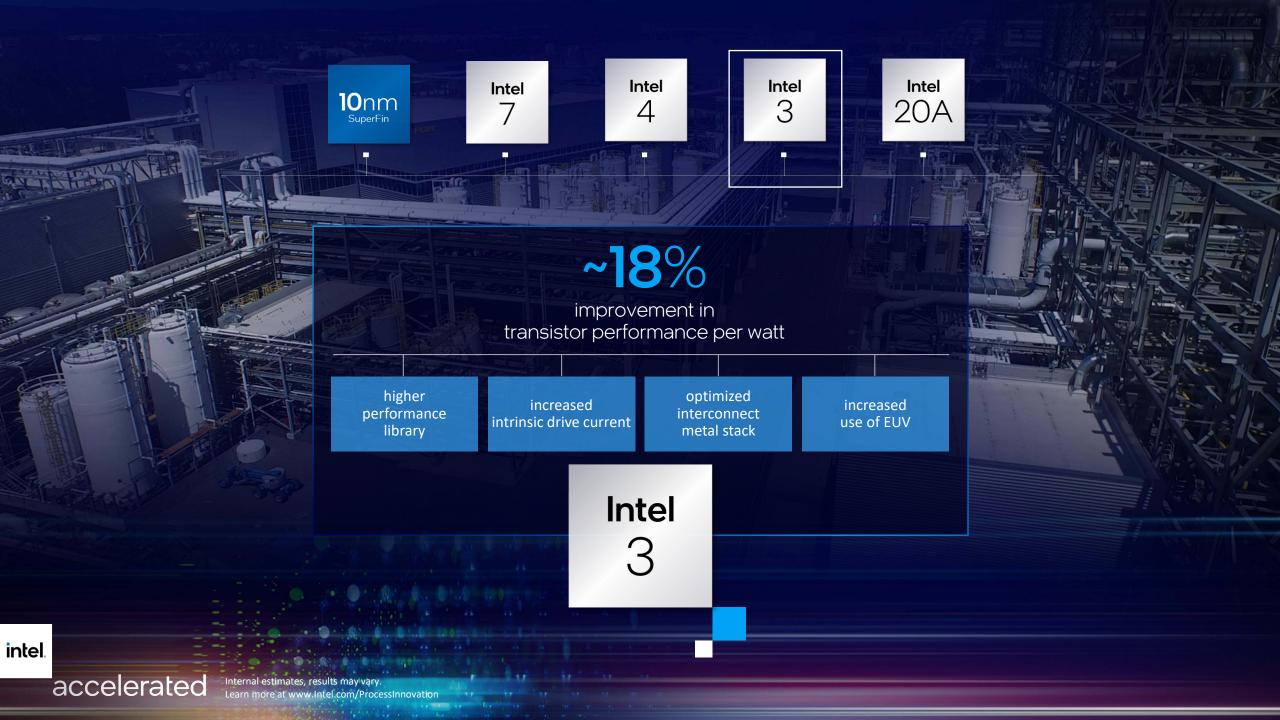
Peter Wennink

CEO and president, ASML



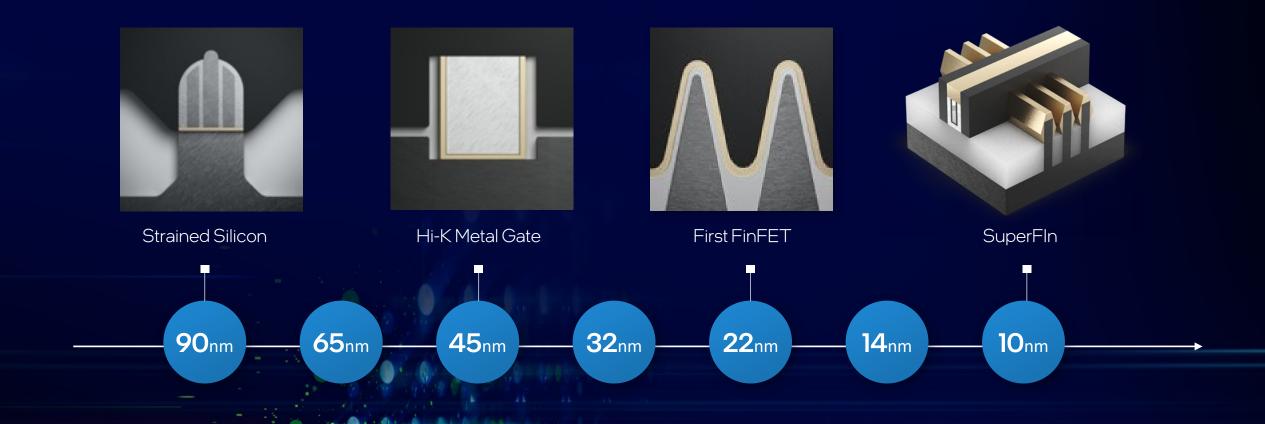
intel.

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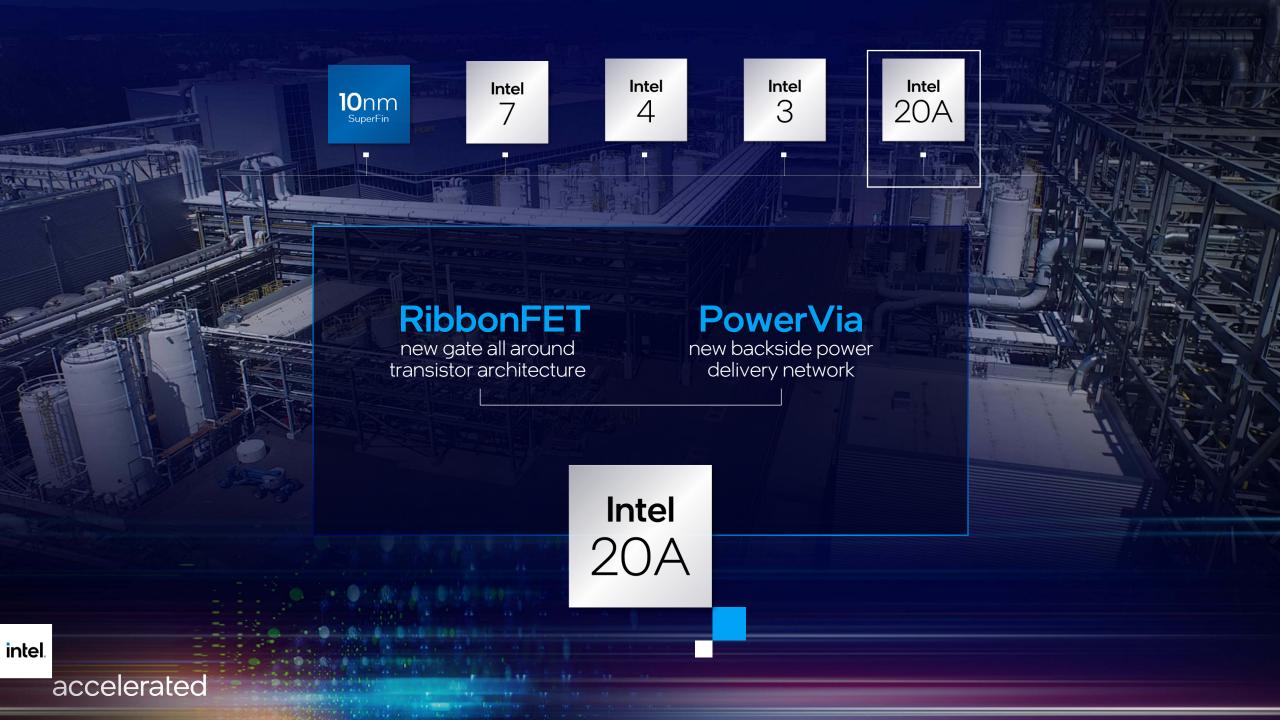


Process Innovations

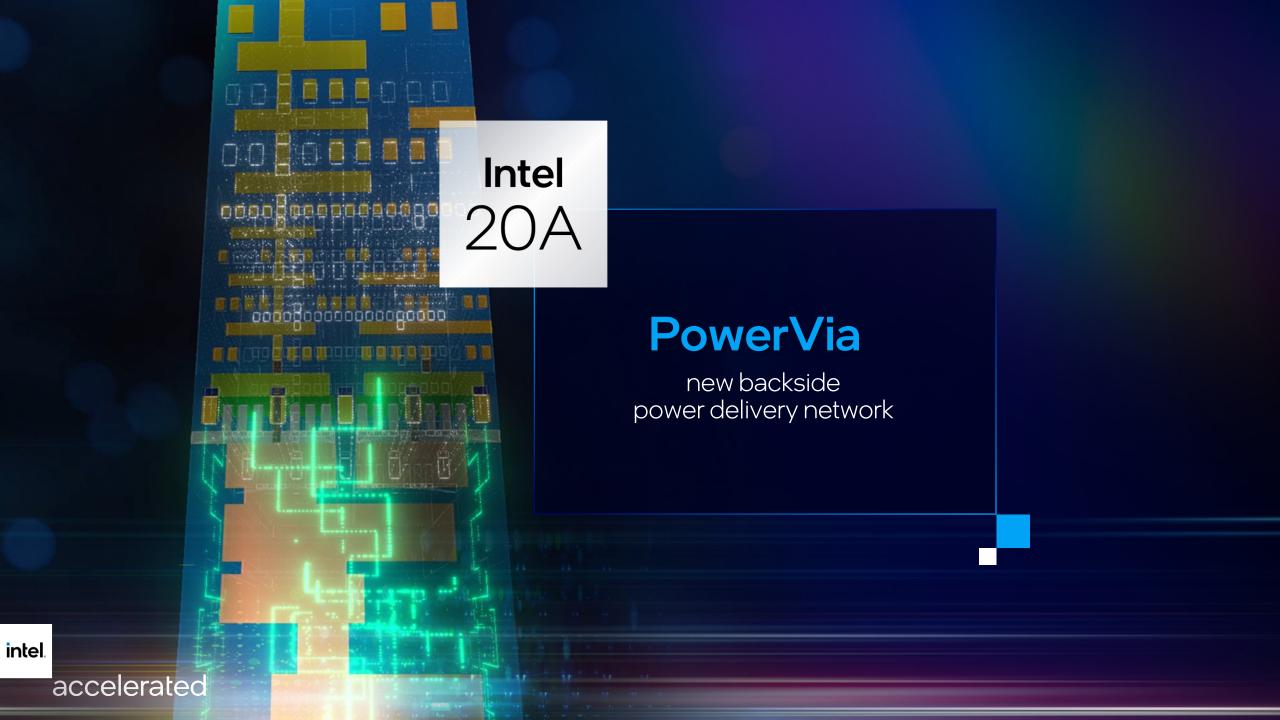


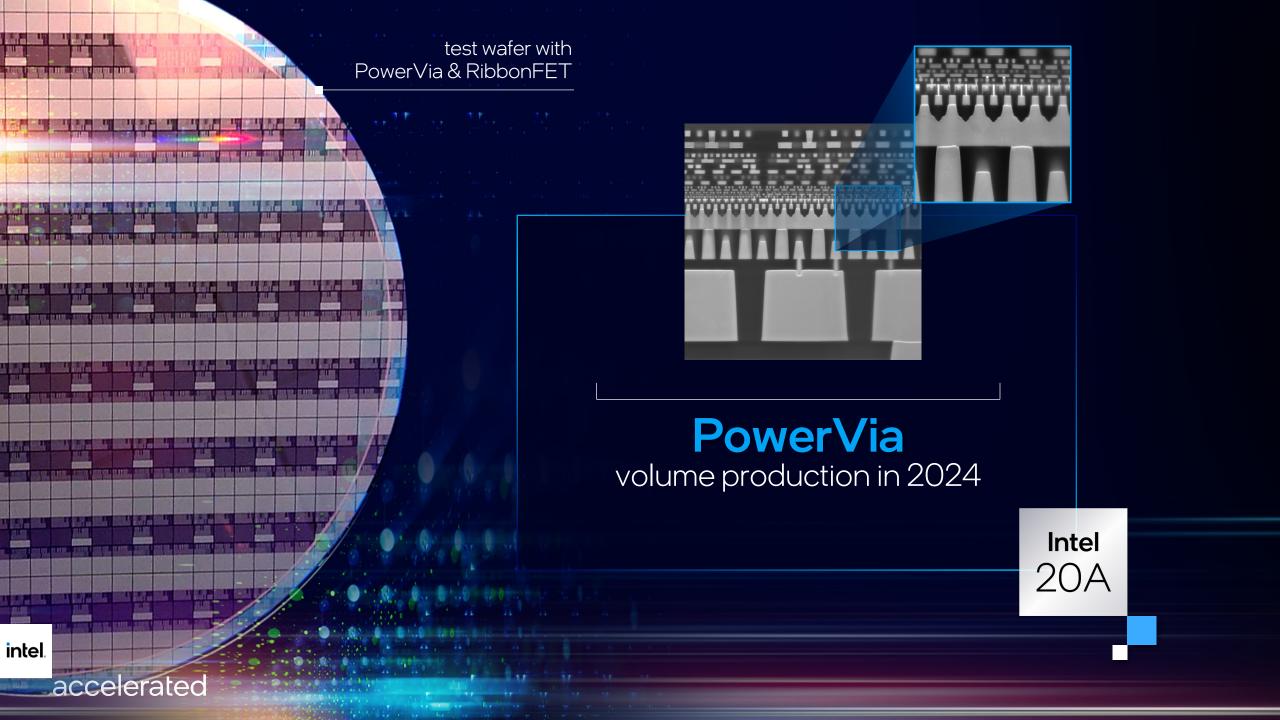
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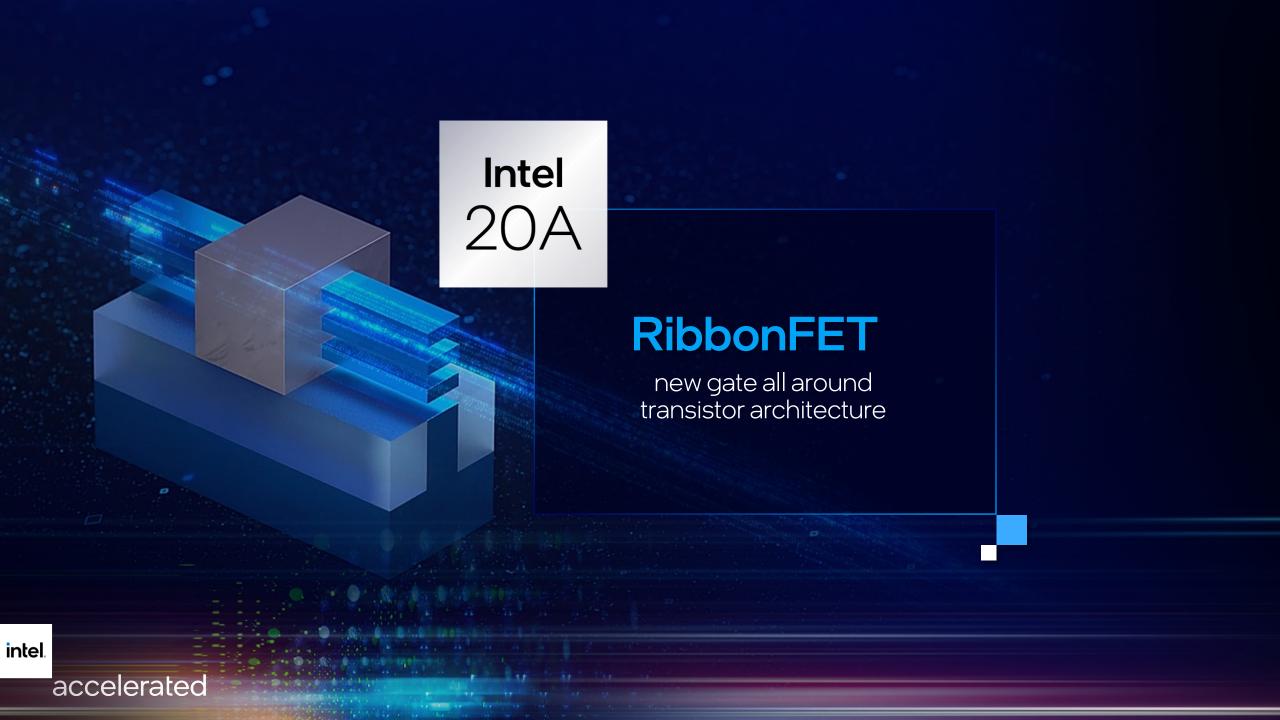
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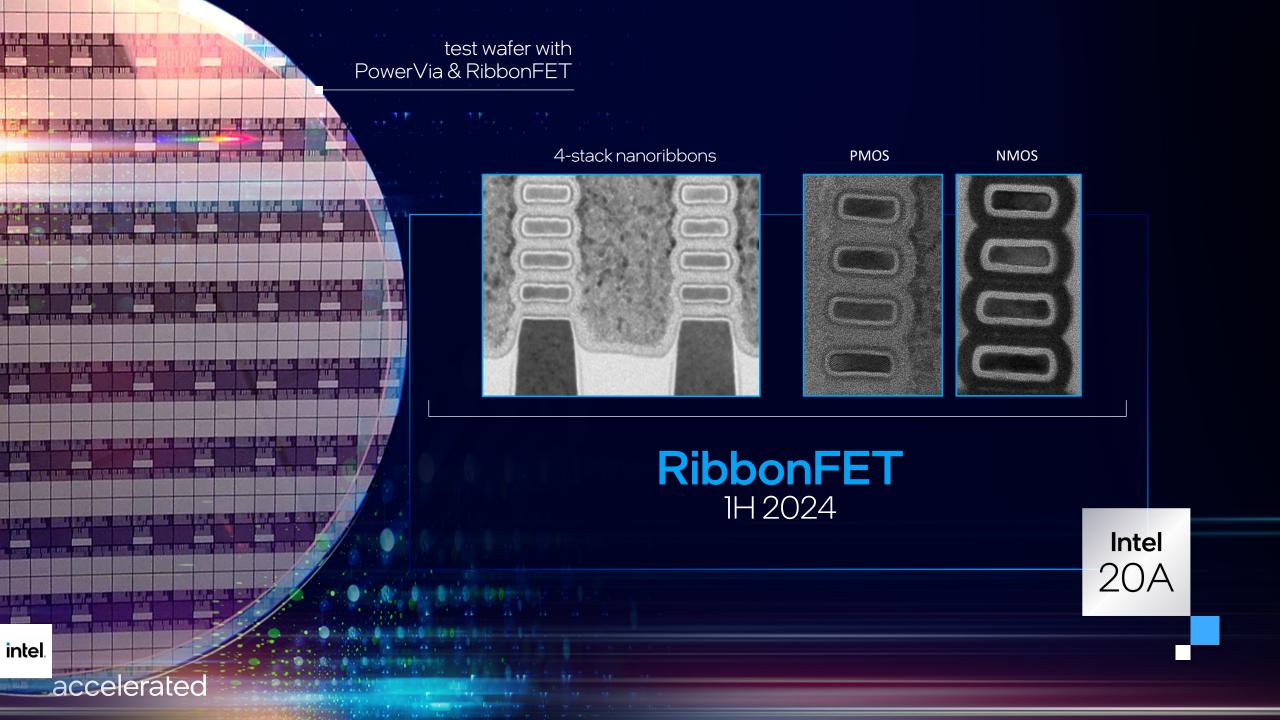












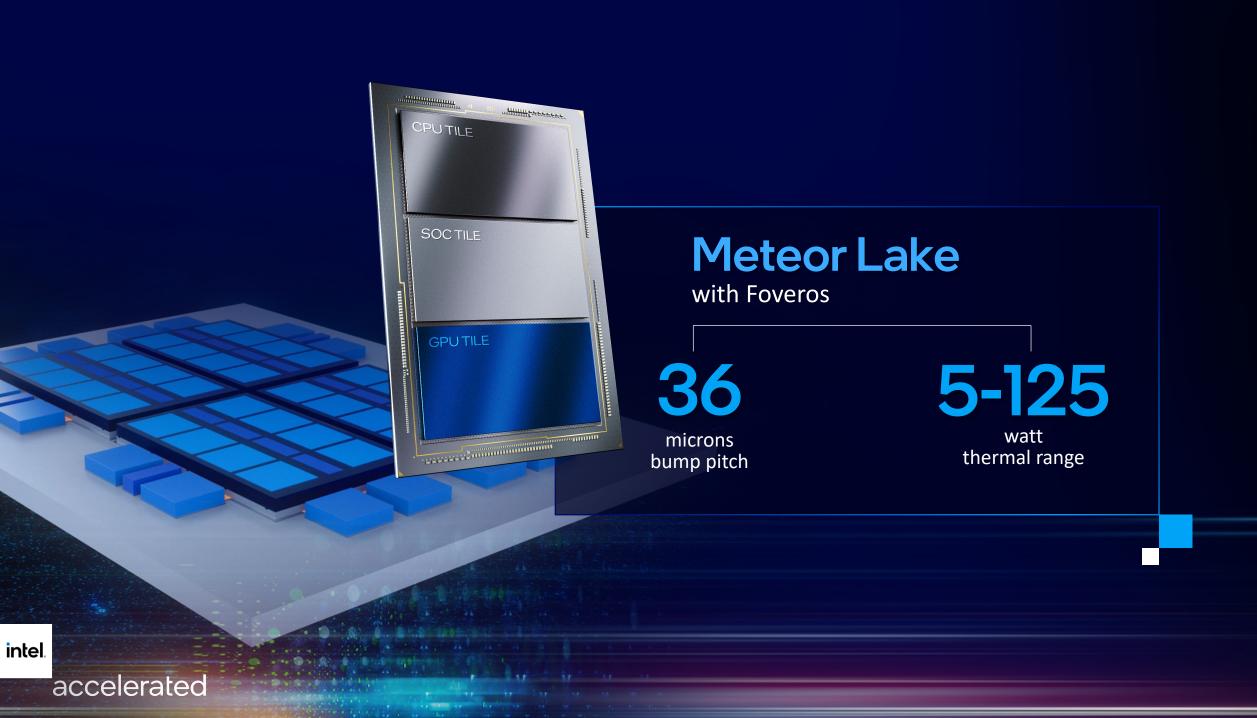
Intel 18A in development for e

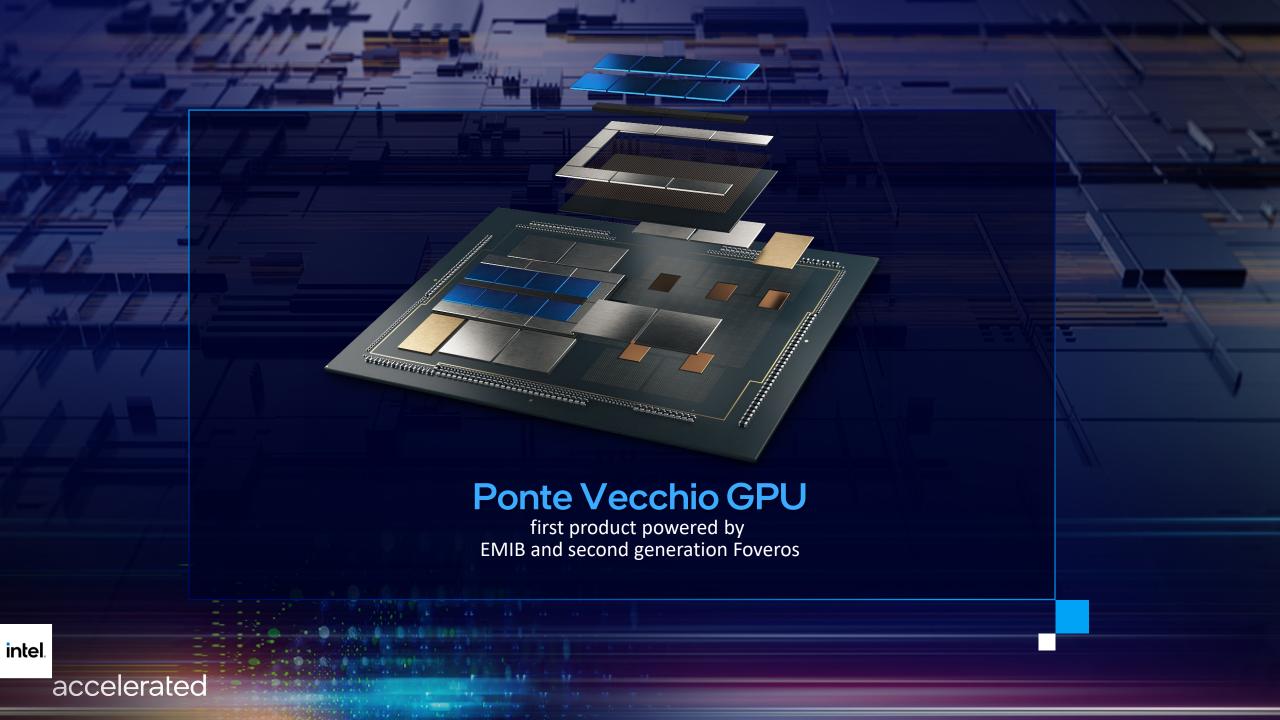
in development for early 2025













Continued leadership in advanced packaging

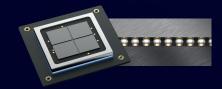
Embedded Multi-die Interconnect (EMIB)



bump pitch **50-40 microns**

- leads industry
- first 2.5D embedded bridge solution
- products shipping since 2017

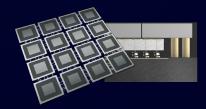
Foveros Technology



bump pitch 50-36 microns

- wafer-level packaging capabilities
- first-of-its-kind 3D stacking solution

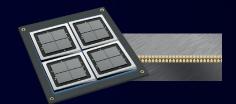
Foveros Omni



bump pitch ~25 microns

- next gen Foveros technology
- unbounded flexibility with performance 3D stacking technology for die-to-die interconnect and modular designs

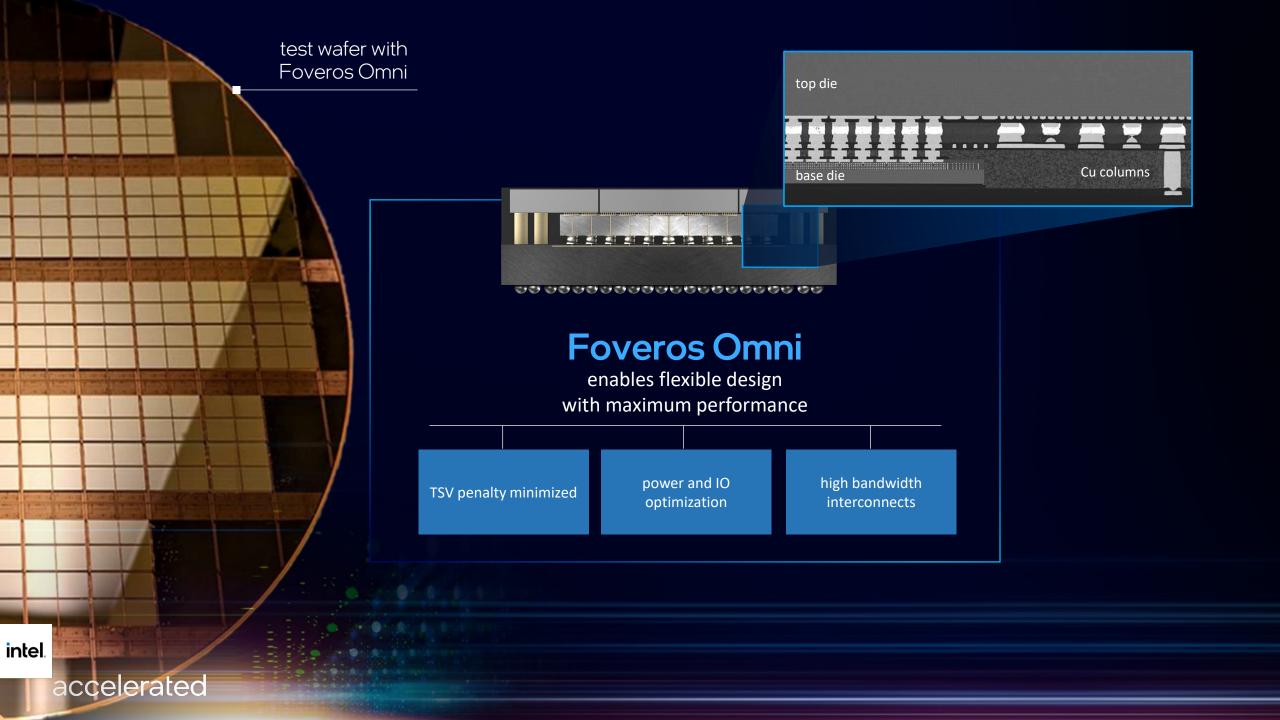
Foveros Direct



bump pitch < 10 microns

- direct copper-to-copper bonding for low resistance interconnects
- blurs the boundary between where the wafer ends and the package begins





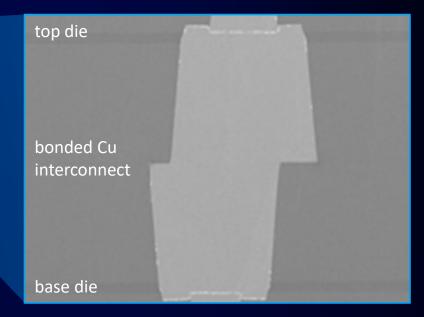


Foveros Direct

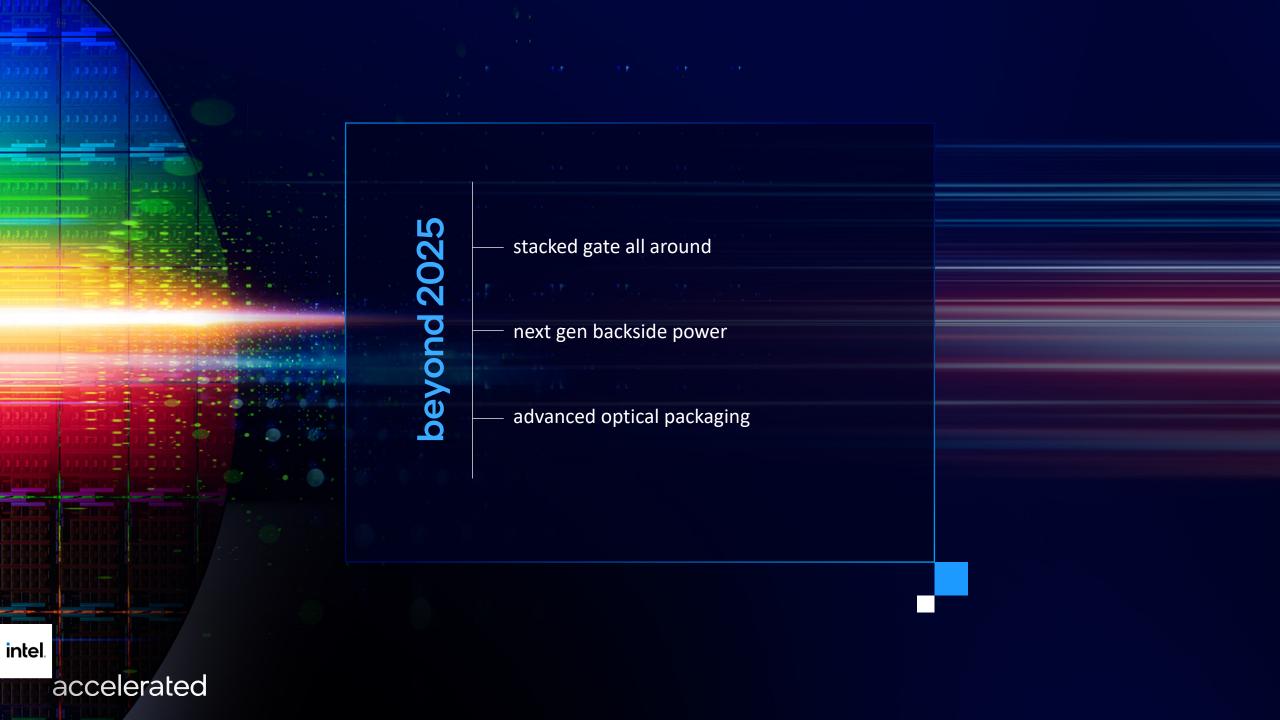
direct copper-to-copper bonding which enables low resistance interconnects

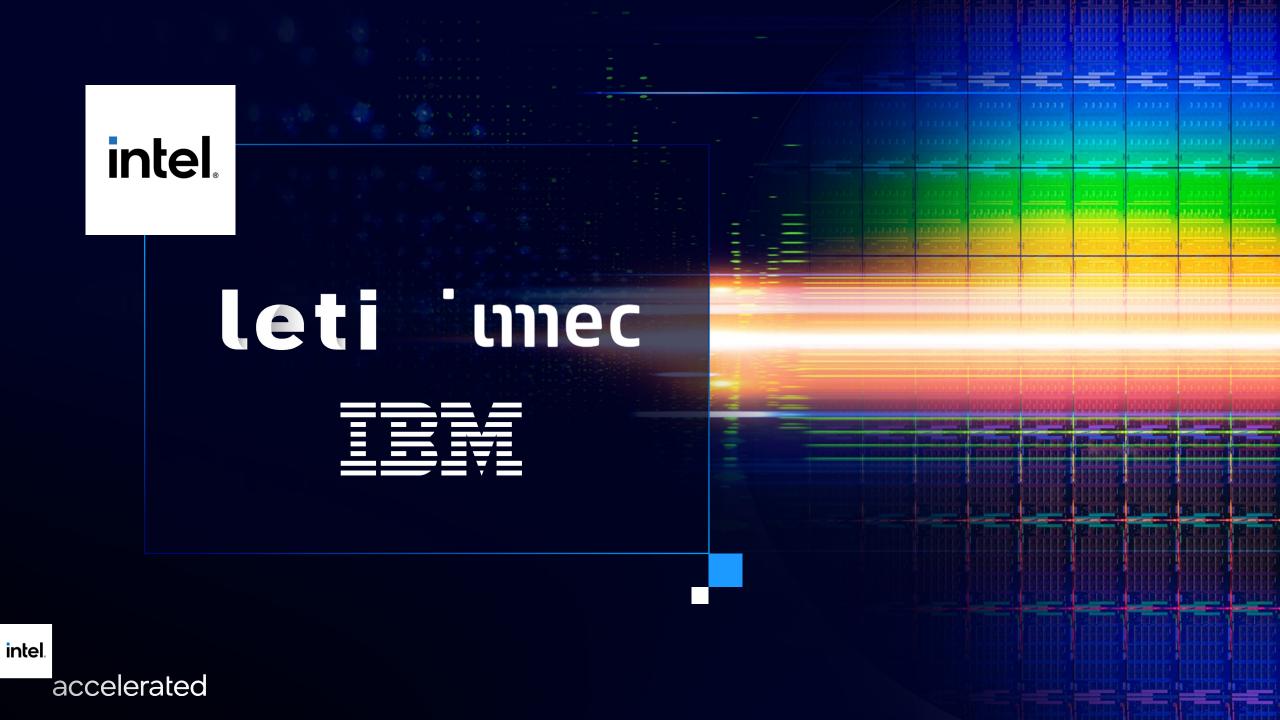
bump density increases to 10K/mm²

functional block level partitioning

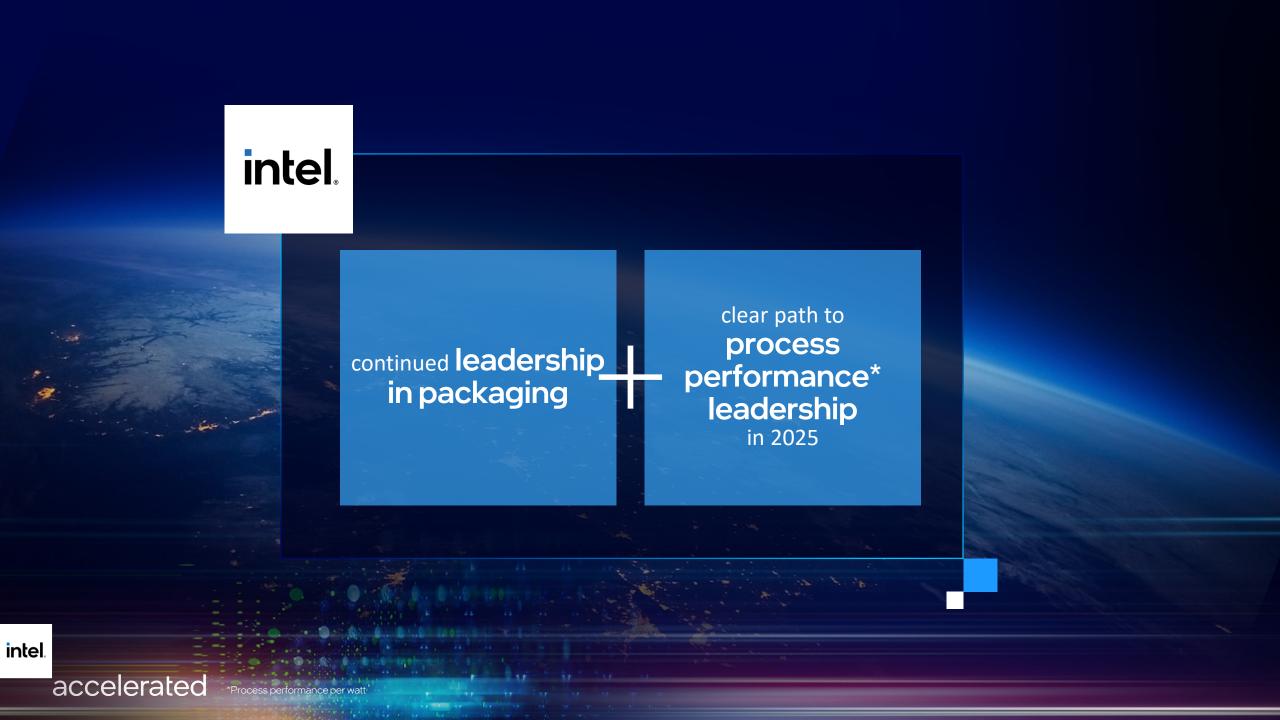


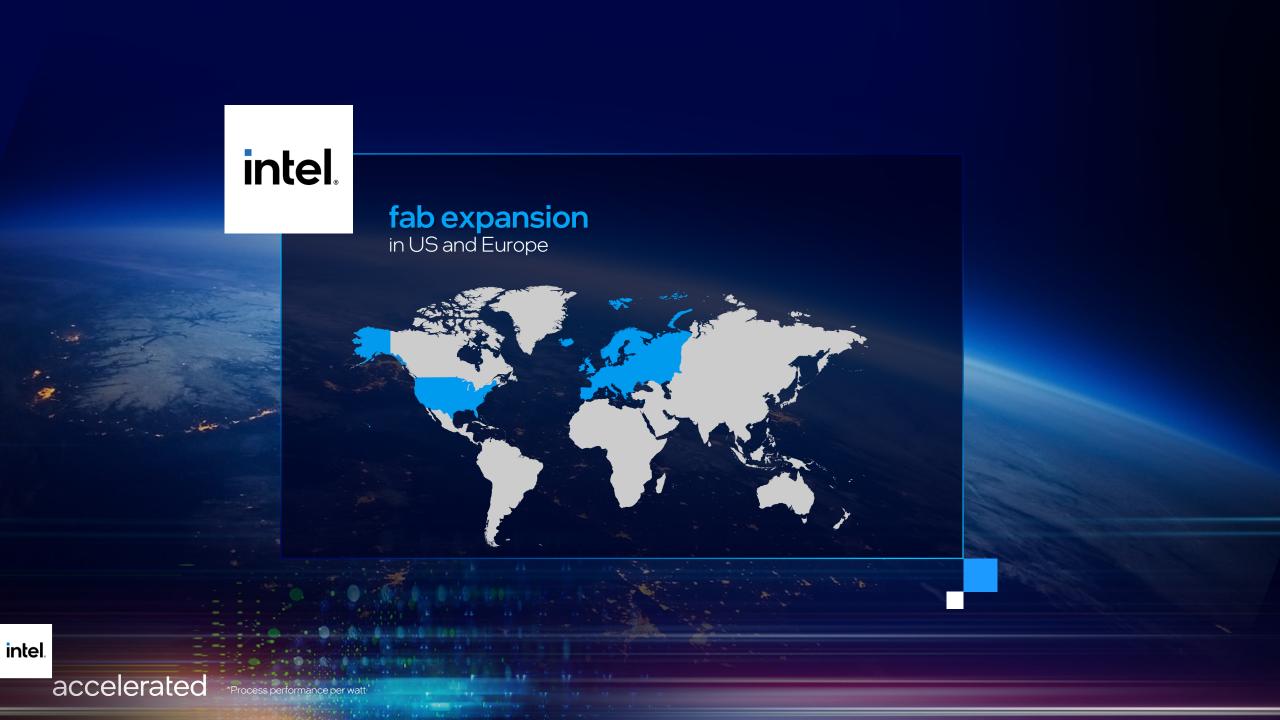


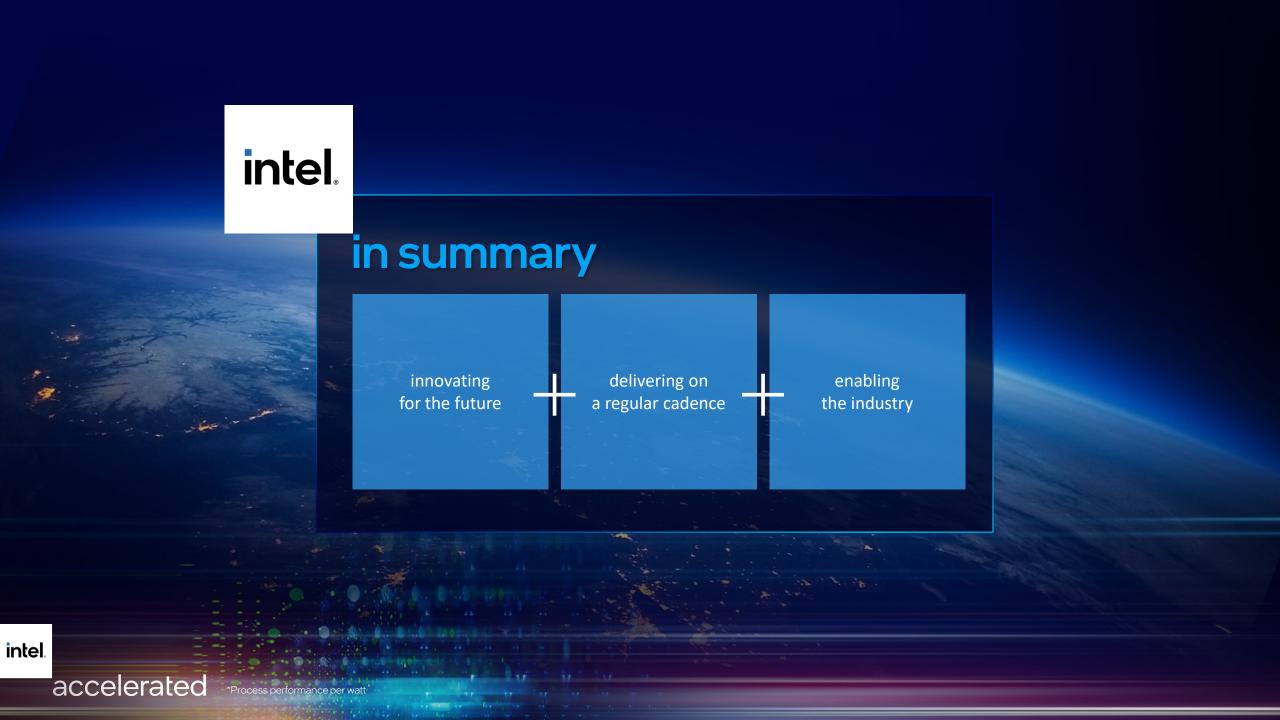
















intel Innovation October 27 and 28th in San Francisco intel. accelerated

