

News Byte

December 18, 2017

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The Intel® Stratix® 10 MX FPGA is the industry's first field programmable gate array (FPGA) with integrated High Bandwidth Memory DRAM (HBM2).
(Credit: Intel Corporation)

Intel today announced the availability of the Intel® Stratix® 10 MX FPGA, the industry's first field programmable gate array (FPGA) with integrated High Bandwidth Memory DRAM (HBM2). By integrating the FPGA and the HBM2, Intel Stratix 10 MX FPGAs offer up to 10 times the memory bandwidth when compared with standalone DDR memory solutions¹. These bandwidth capabilities make Intel Stratix 10 MX FPGAs the essential multi-function accelerators for high-performance computing (HPC), data centers, network functions virtualization (NFV), and broadcast applications that require hardware accelerators to speed-up mass data movements and stream data pipeline frameworks.

In HPC environments, the ability to compress and decompress data before or after mass data movements is paramount. HBM2-based FPGAs can compress and accelerate larger data movements compared with stand-alone FPGAs. With High Performance Data Analytics (HPDA) environments, streaming data pipeline frameworks like Apache* Kafka and Apache* Spark Streaming require real-time hardware acceleration. Intel Stratix 10 MX FPGAs can simultaneously read/write data and encrypt/decrypt data in real-time without burdening the host CPU resources.

More: [Intel Stratix MX FPGAs](#) | [Intel Embedded Multi-die Interconnect Bridge \(EMIB\) Whitepaper](#) | [Intel Programmable Solutions Group News](#)

"To efficiently accelerate these workloads, memory bandwidth needs to keep pace with the explosion in data" said Reynette Au, vice president of marketing, Intel Programmable Solutions Group. "We designed the Intel Stratix 10 MX family to provide a new class of FPGA-based multi-function data accelerators for HPC and HPDA markets."

The Intel Stratix 10 MX FPGA family provides a maximum memory bandwidth of 512 gigabytes per second with the integrated HBM2. HBM2 vertically stacks DRAM layers using silicon via (TSV) technology. These DRAM layers sit on a base layer that connects to the FPGA using high density micro bumps. The Intel Stratix 10 MX FPGA family utilizes Intel's Embedded Multi-Die Interconnect Bridge (EMIB) that speeds communication between FPGA fabric and the DRAM. EMIB works to efficiently integrate HBM2 with a high-performance monolithic FPGA fabric, solving the memory bandwidth bottleneck in a power-efficient manner.

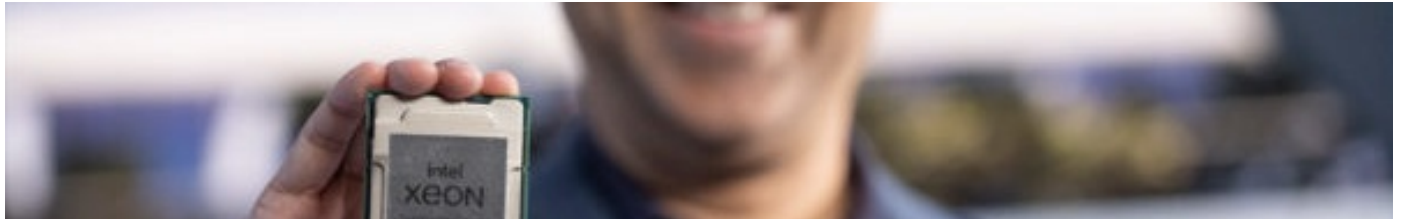
Intel is shipping several Intel Stratix 10 FPGA family variants, including the Intel Stratix 10 GX FPGAs (with 28G transceivers) and the Intel Stratix 10 SX FPGAs (with embedded quad-core ARM processor). The Intel Stratix 10 FPGA family utilizes Intel's 14 nm FinFET manufacturing process and incorporates state-of-the-art packaging technology, including EMIB.

¹As compared to a standard DDR 2400 DIMM. See the “Intel® Stratix® 10 MX Devices Solve the Memory Bandwidth Challenge White Paper” at https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-01264-stratix10mx-devices-solve-memory-bandwidth-challenge.pdf for more information.

Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

Tags: [FPGA](#), [Intel Stratix 10](#)

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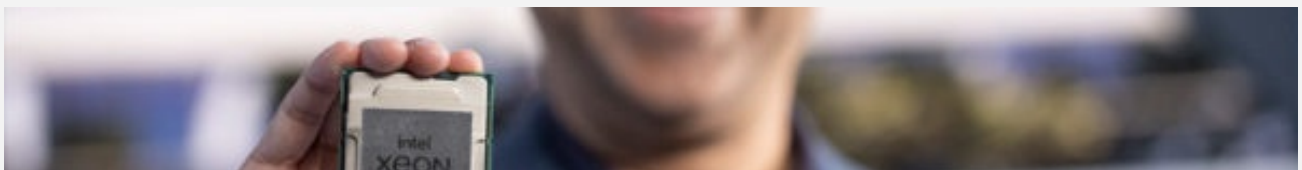
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