Tri-Gate Transistor Architecture with High-k Gate Dielectrics, Metal Gates and Strain Engineering

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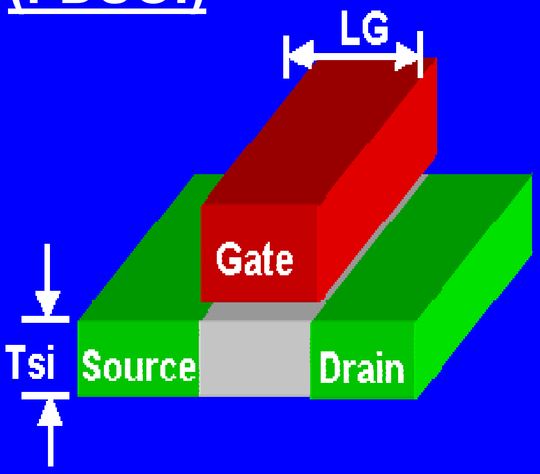
Outline

- Introduction – Why Tri-Gate
- Trigate CMOS Fabrication
- Trigate Physics
  - Electrostatics
  - Parasitics
  - High-k / Metal Gates
  - Carrier Transport
- Trigate Performance
- Conclusions

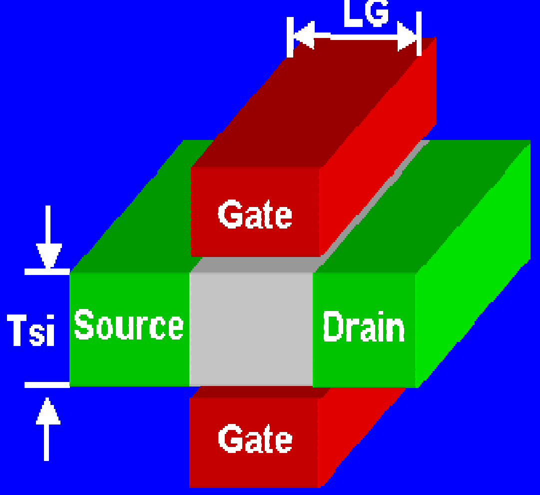
Fully Depleted Transistor Structures

Planar Single Gate (FDSOI)



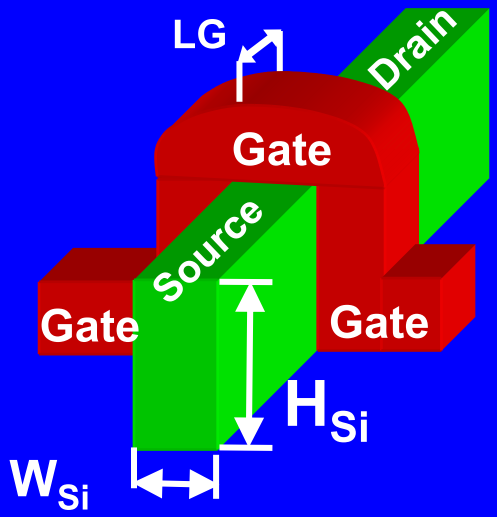
1. Ultra thin Tsi
2. Limited to SOI

Planar Double-Gate



1. Wider Tsi than planar
2. Non Self-aligned

Non Planar Tri-Gate



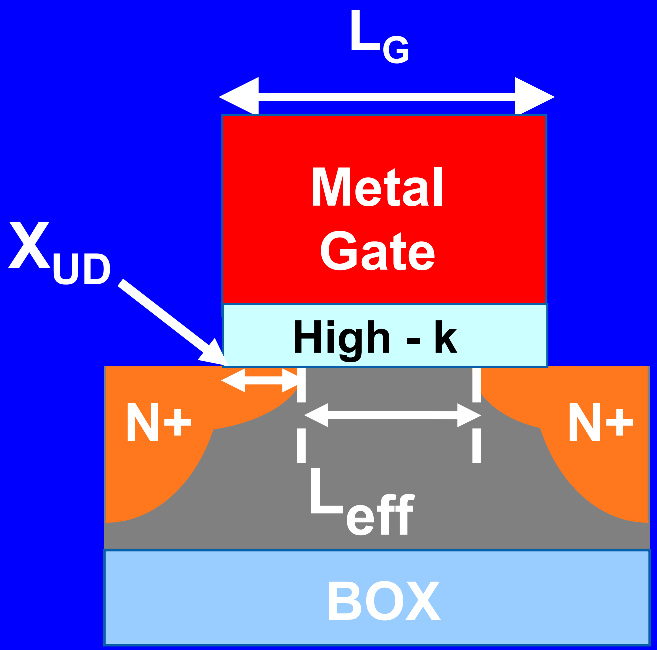
1. FIN W_{Si} is wider than planar T_{Si}
2. Self-Aligned gates
3. Bulk-Si or SOI

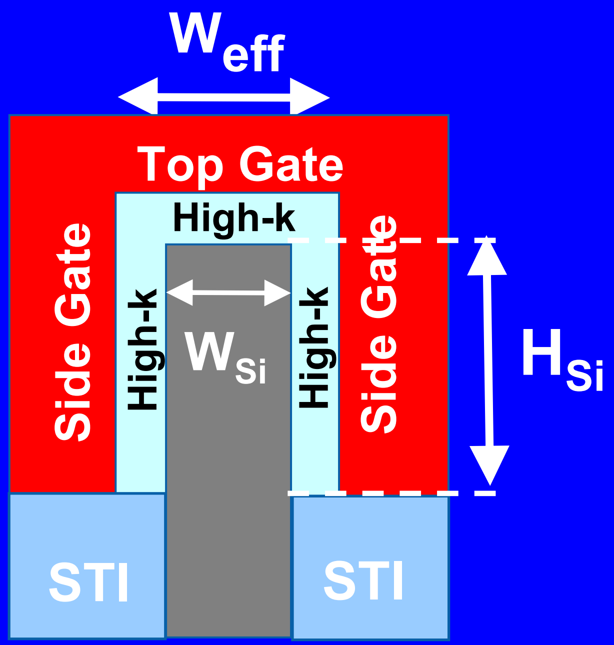
- Fully depleted thin-body devices improve SCE performance.
- Tri-Gate is the most favorable architecture for L_G scaling.

Tri-Gate CMOS Fabrication

1. Tri-Gate Critical Dimensions
2. FIN / Channel profile engineering
3. Poly / Metal Gate / High-k Stack Etch
4. 3-D Spacer formation
5. Dual Epitaxial raised Source/Drains

Tri-Gate Critical Dimensions



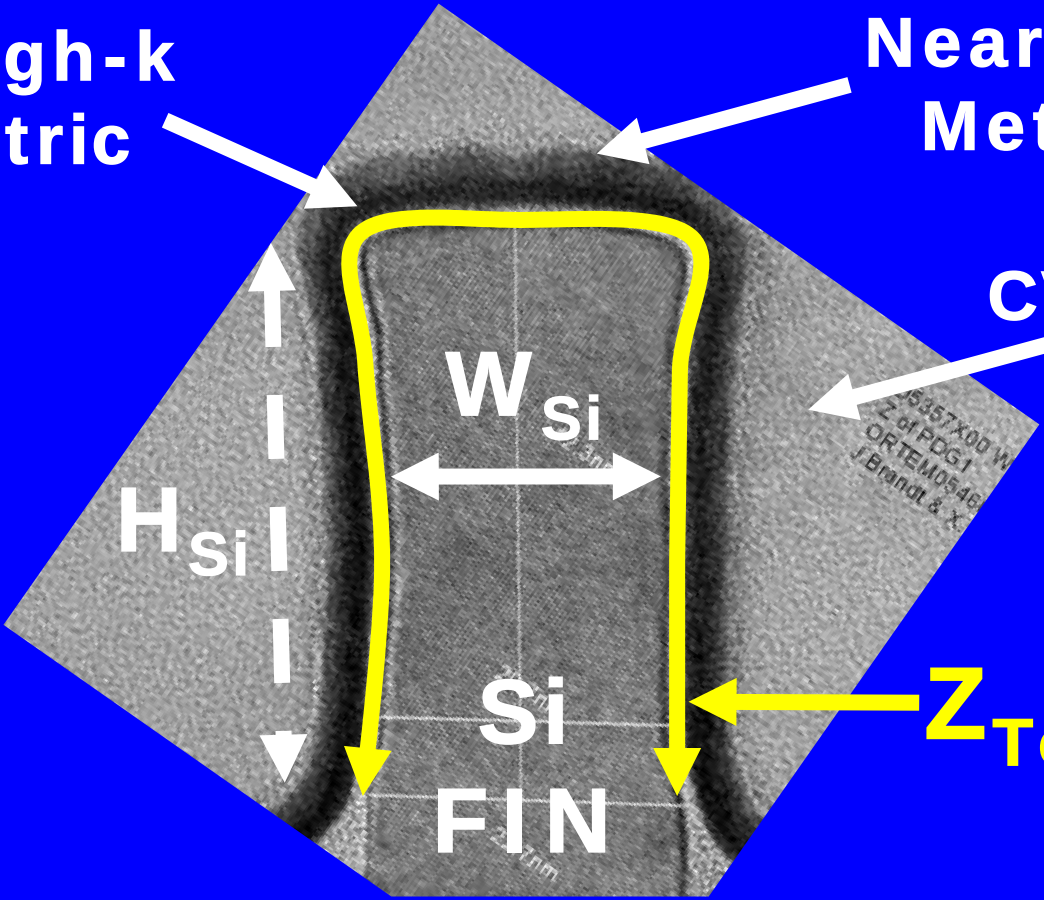


- I_{DSAT} is normalized by $Z_T = W_{Si} + 2 * H_{Si}$
- Tri-gate electrostatics strongly depend on the ratio of L_{eff} / W_{eff} as defined by:

$$L_{eff} = L_G - 2 * X_{UD}$$

$$W_{eff} = W_{Si} + 2(\varepsilon_{Si} / \varepsilon_{OX}) * T_{OX}$$

Tri-Gate FIN Critical Dimensions



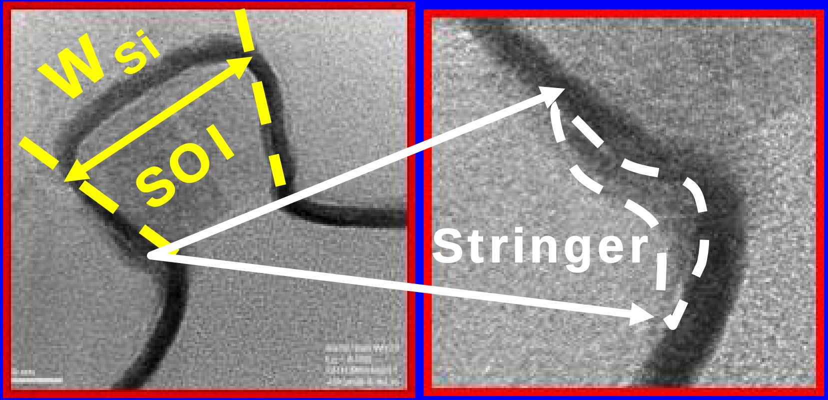
HfO_2 High-k Dielectric

Near Mid-Gap Metal Gate

CVD Poly

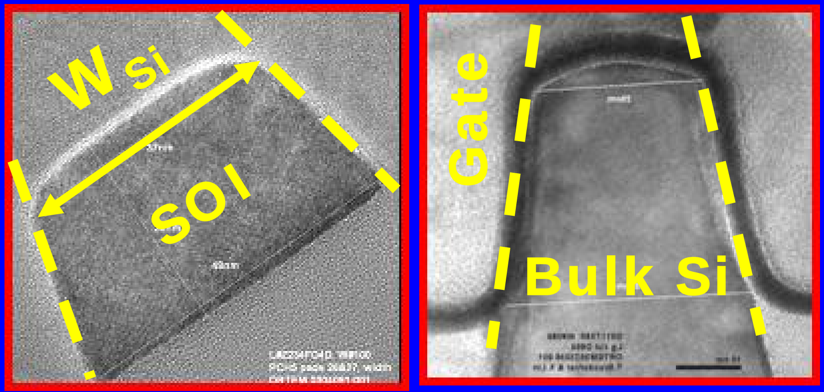
Z_{Total}

FIN Profile Optimization



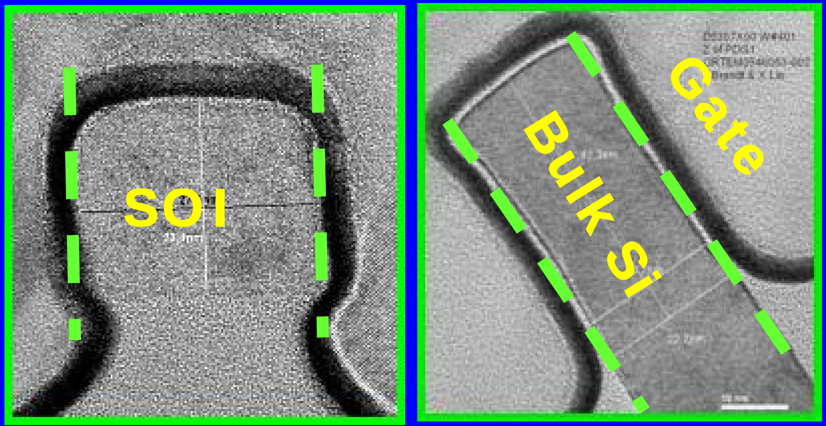
Notched FIN

- Narrowing FIN W_{Si} - Better SCEs
- Yield Impact - Poly / MG stringers



Tapered FIN

FIN widens - Degraded SCEs

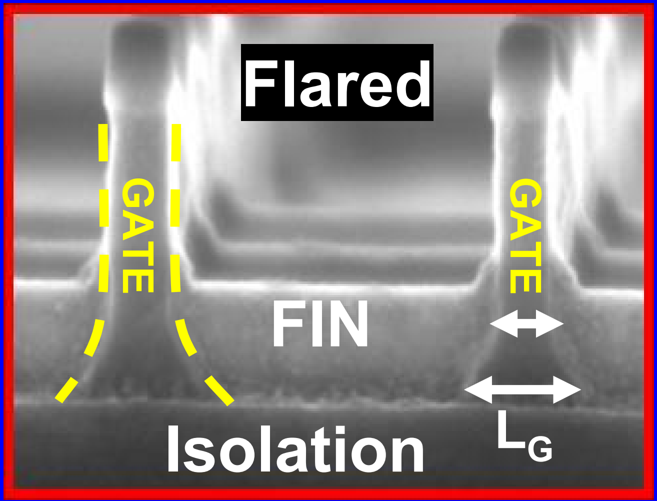


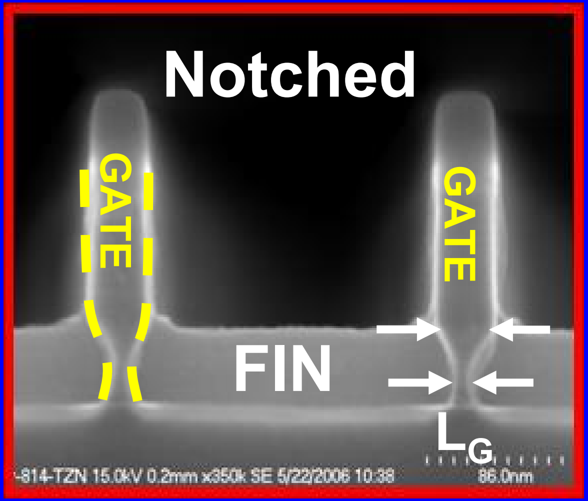
Vertical FIN – Ideal

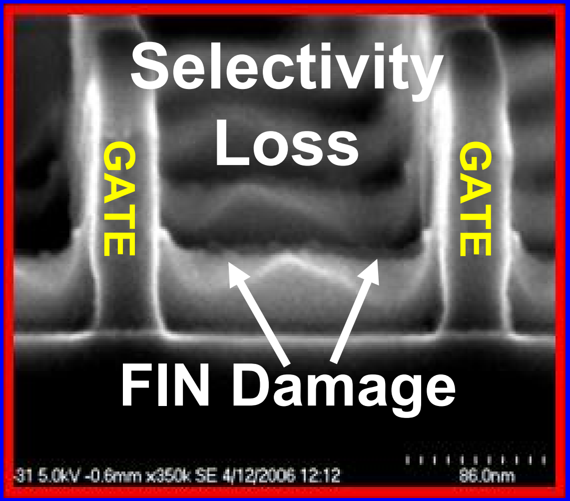
- Improved SCEs
- No additional process complexity

3-D Poly/Metal Gate Stack Etch

<u>Challenge:</u> Significant over-etch required to clear the Poly/Metal spacers on the FIN sidewall



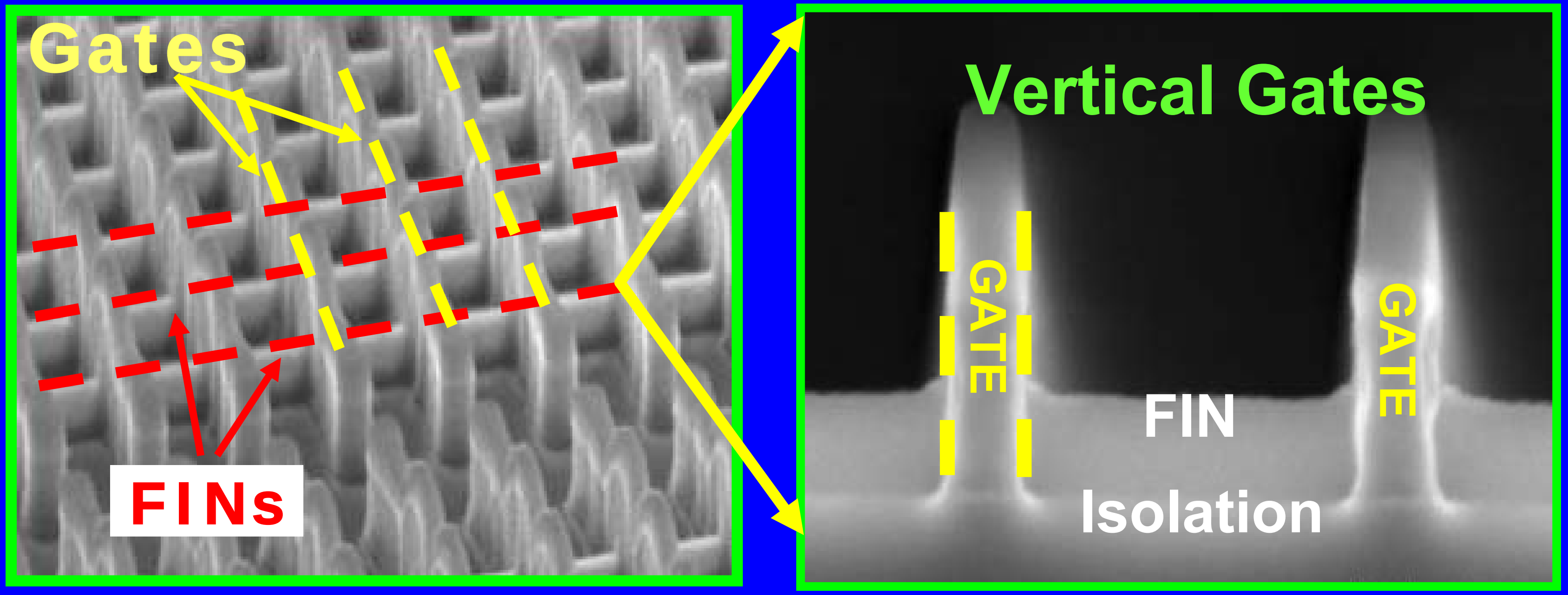




- Etch Charging, Micro-Loading lead to variable L_G
- Selectivity Loss during over-etch damages Si-FIN

3-D Poly/Metal Gate Stack Etch

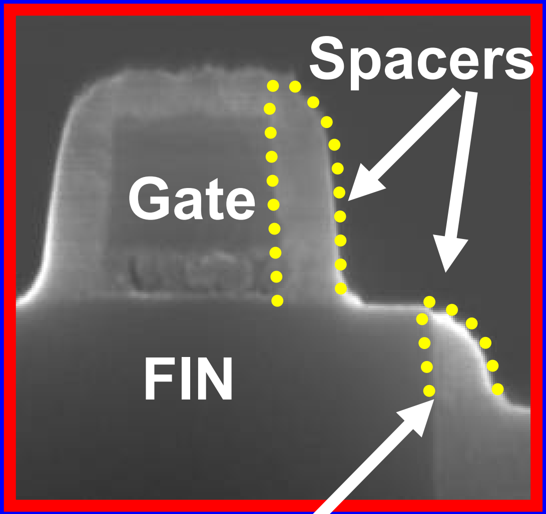
Nested FIN & Gate Array **3-D Gate Profiles**



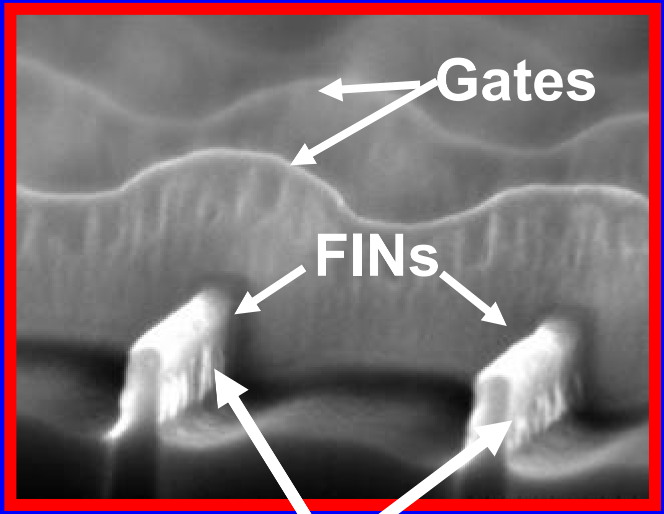
Careful optimization of dry and wet etch modules has produced 3-D gates with no L_G variation or FIN loss.

3-D Spacer Formation

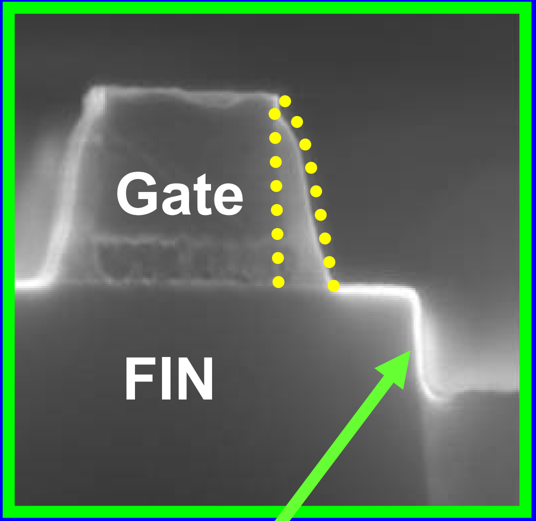
Challenge: Significant over-etch required to clear the offset spacer on the FIN sidewall for epi-raised S/D growth



FIN Spacer Blocks Raised S/D Epi Growth which will Increase R_{EXT}



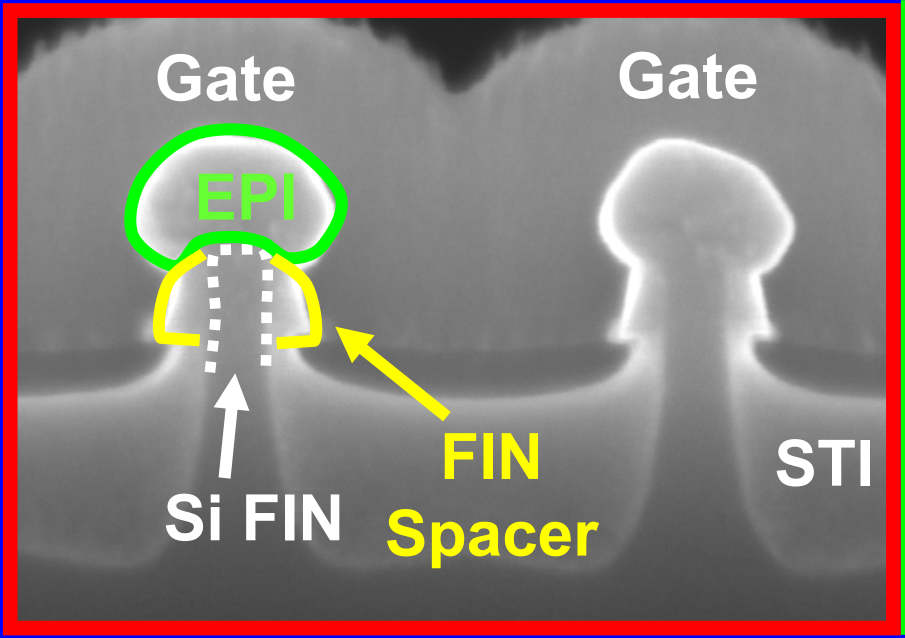
Standard Dry Spacer Over-etch Is non-uniform & leaves behind Spacer Stringers

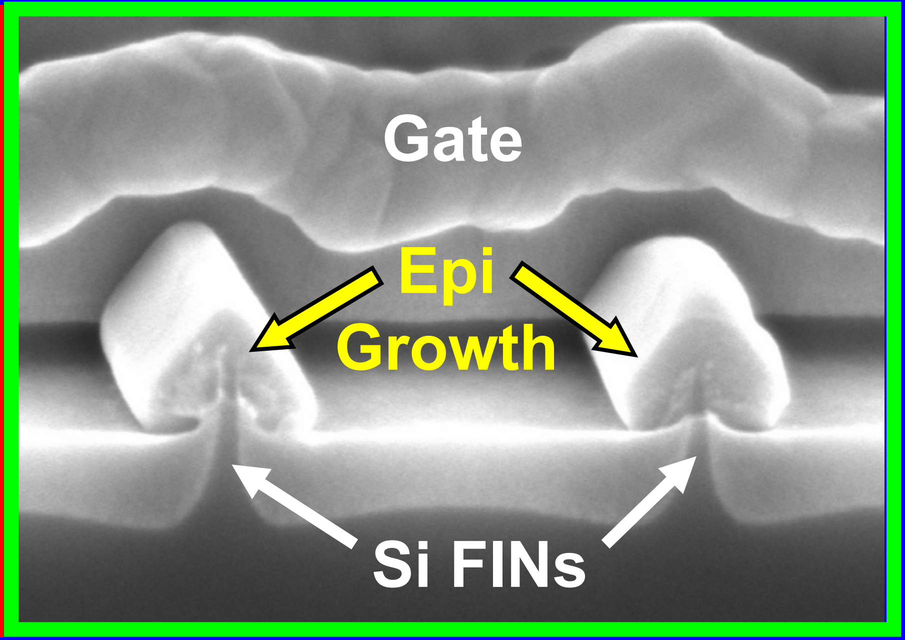


FIN Spacer Removed!

For a 2:1 Gate:FIN ratio we optimize the etch to remove the FIN spacer

3-D Spacer Formation



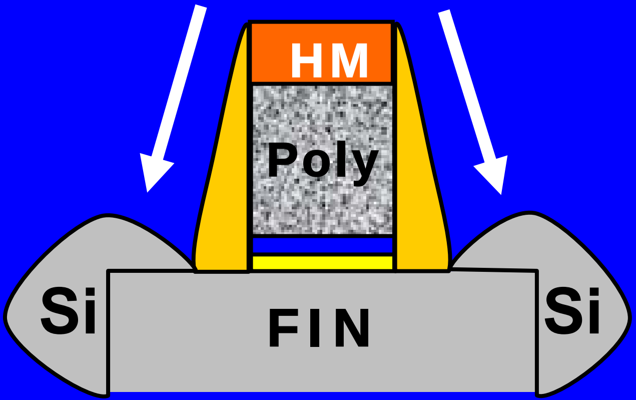


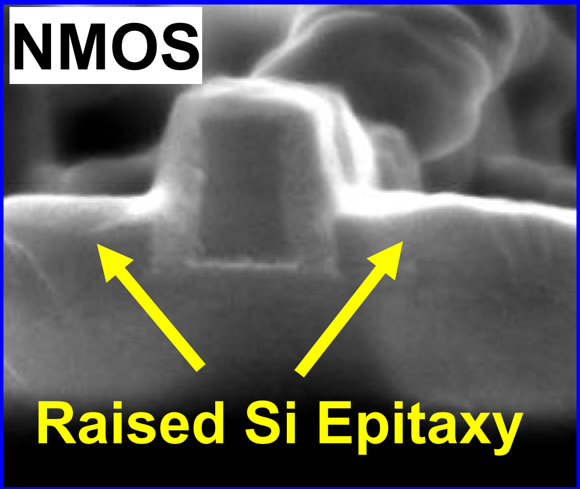
Epi Growth Blocked by the FIN Spacers

Spacers completely removed allowing for epitaxial raised S/D formation

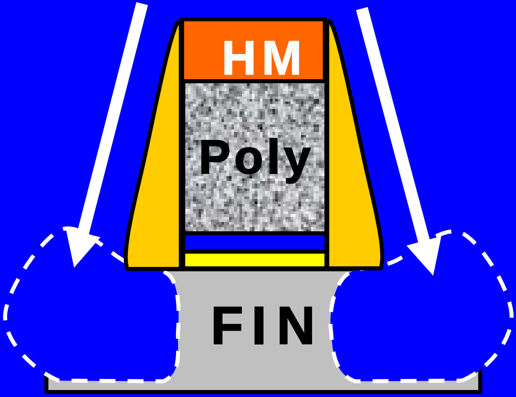
Dual Epitaxial Raised S/D

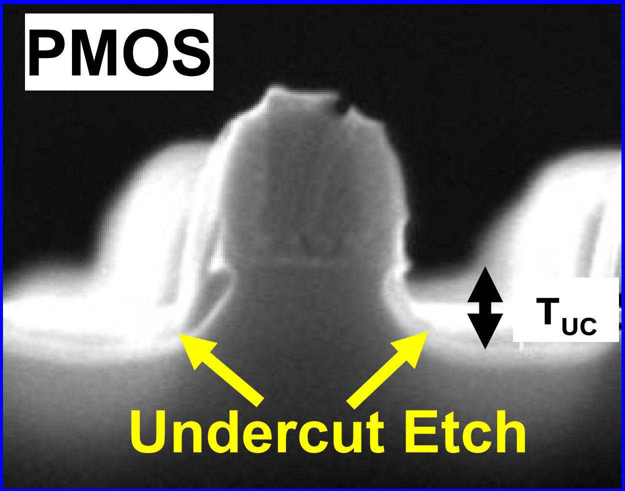
Blanket Epitaxial Si Raised S/D Growth



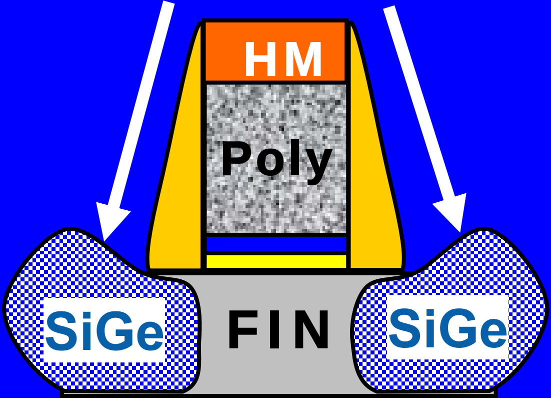


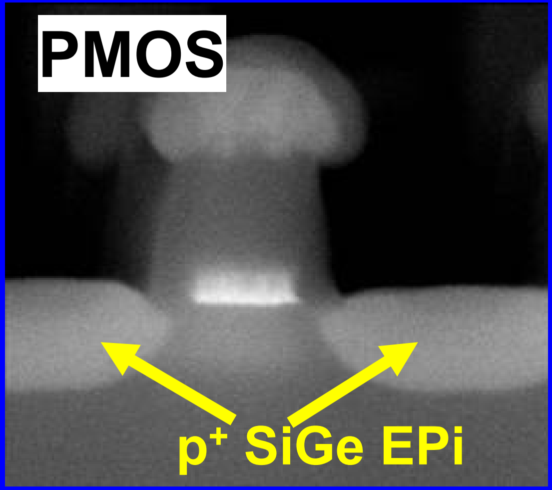
Selective Undercut Etch PMOS regions





In-Situ doped p^+ SiGe Epitaxy

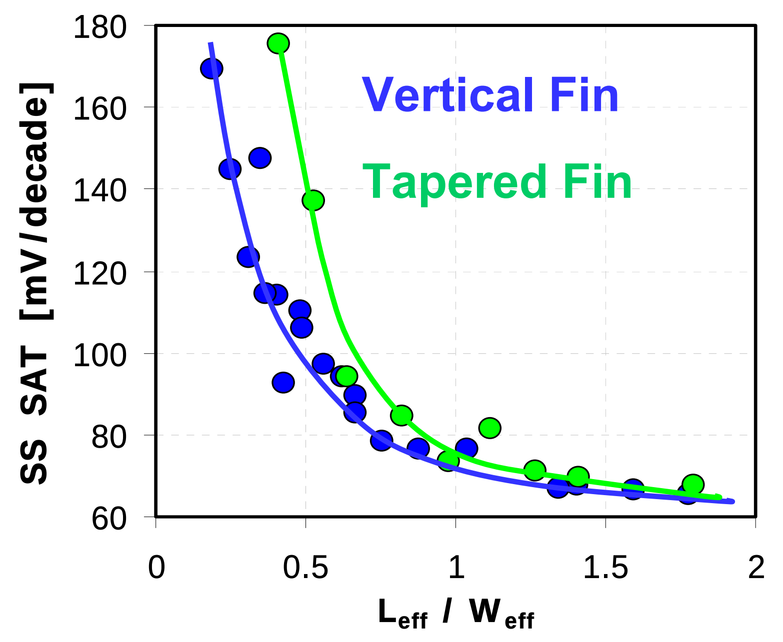


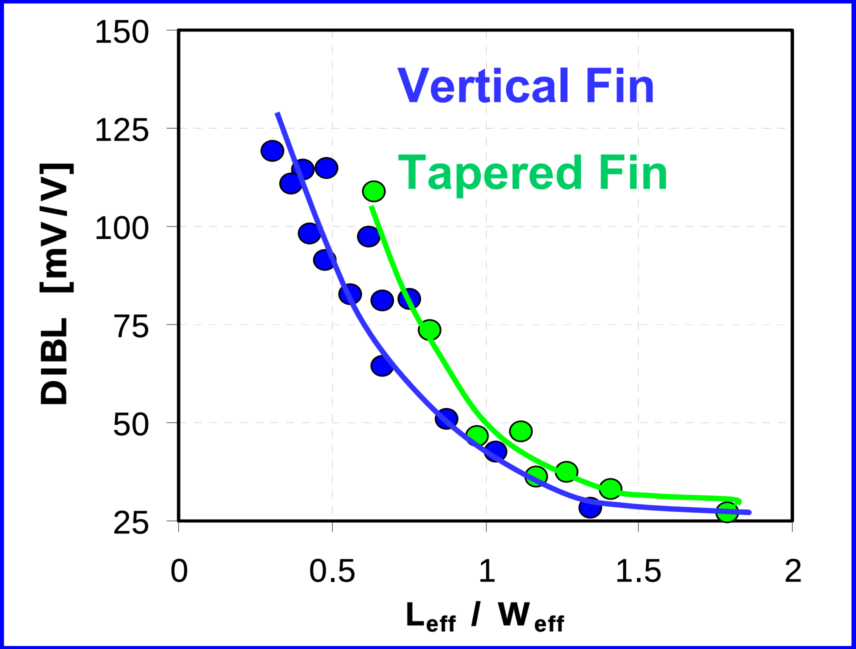


Tri-Gate Physics

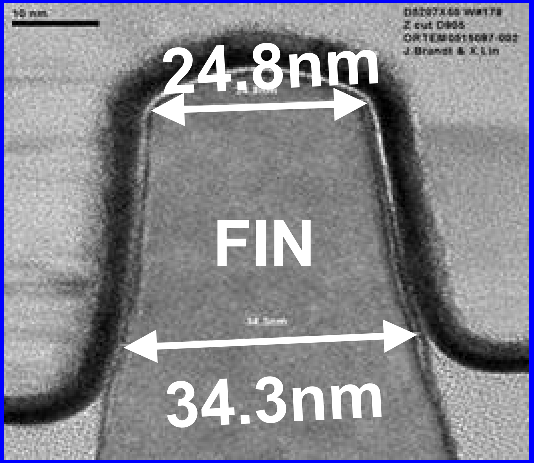
1. Trigate Electrostatics – L_G Scaling
    - FIN Profile
    - FIN Doping
2. Parasitics
    - FIN aspect ratio – R_{EXT}
    - Corner Device suppression
3. Carrier Transport
    - <001> vs. <011> mobility
    - Process Induced Strain

Impact of Fin Profile

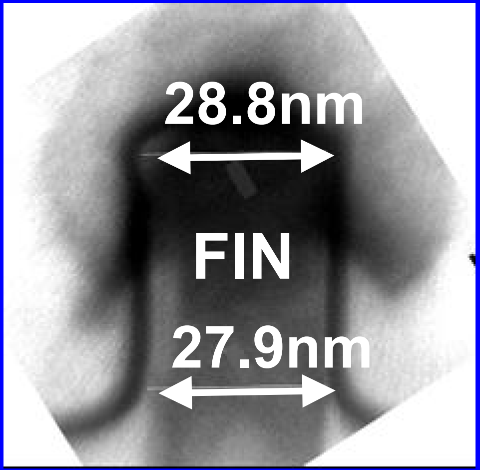




45% FIN Taper



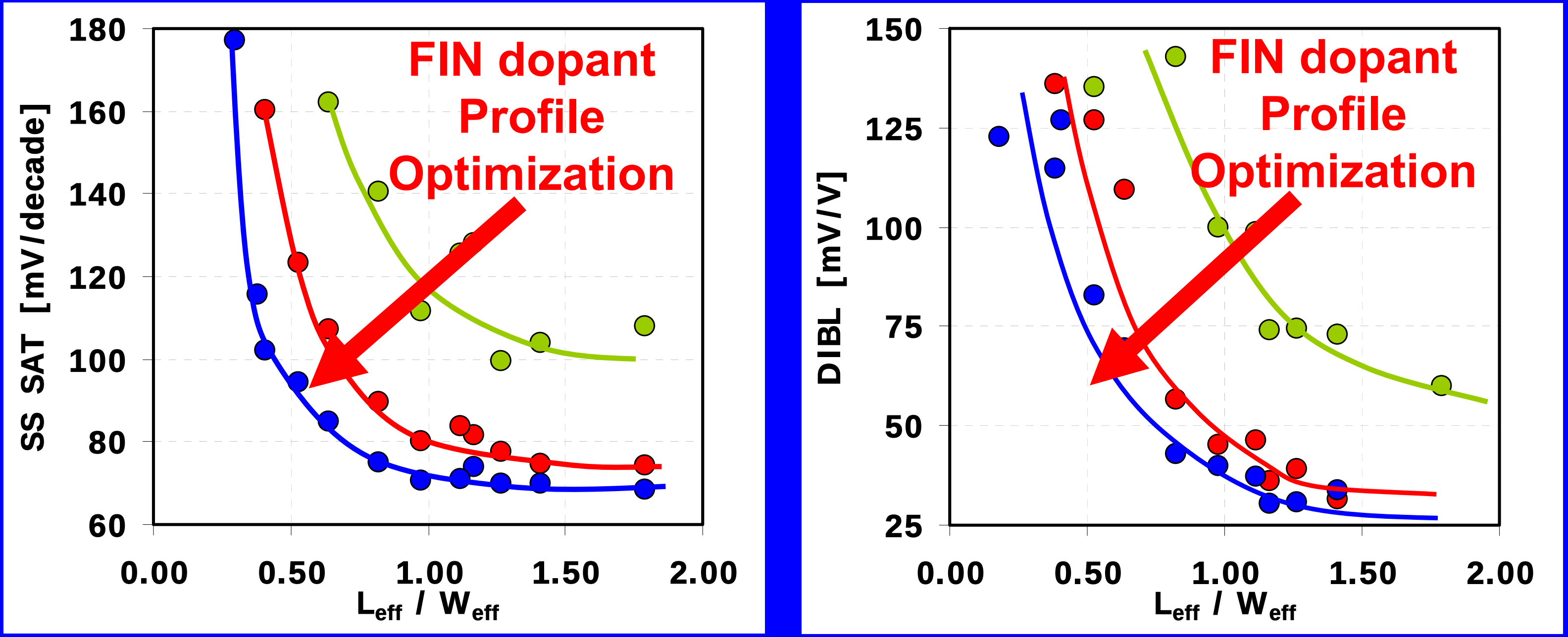
Vertical FIN



Rectangular Fin profile improves SCEs for L_G scaling:

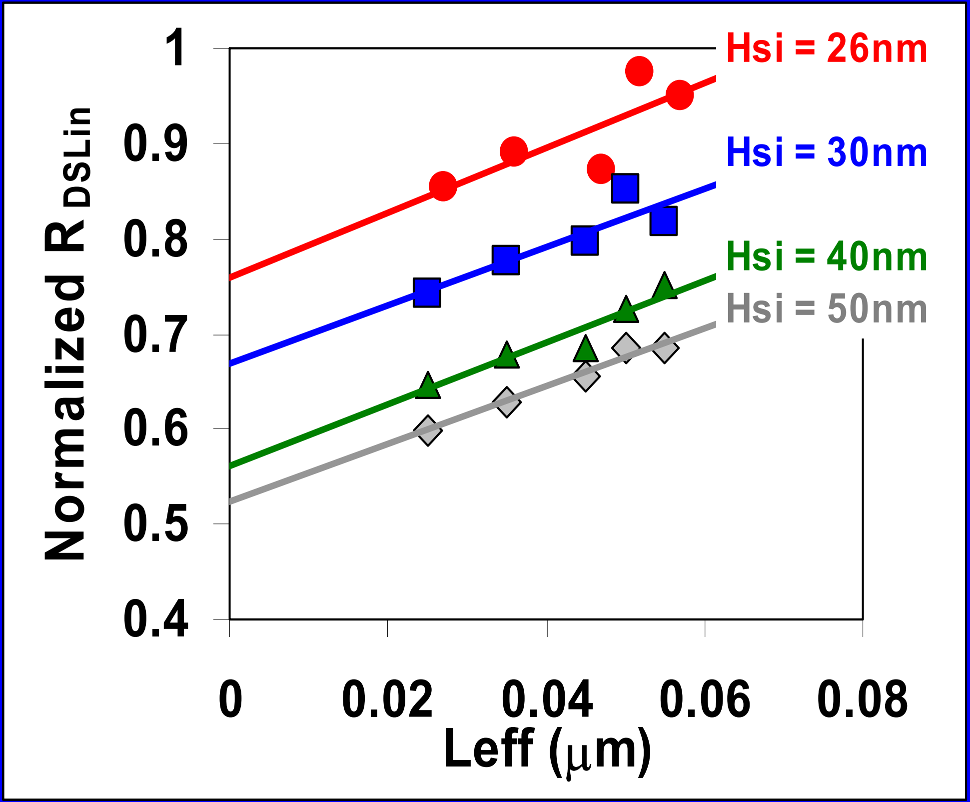
- **Lowers ΔS_{SAT}**
- **Lowers DIBL**

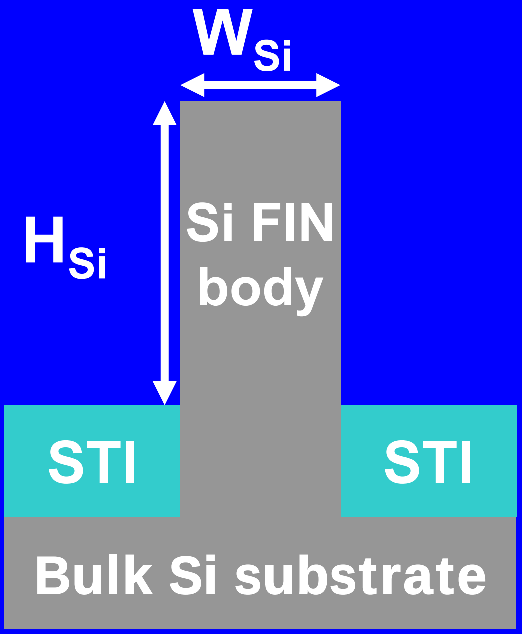
FIN Doping & L_G Scaling



- High-k with near mid-gap workfunction metal gates enable lower dopant values for targeting V_T
- 3-D dopant profile optimization further improves SCE's – ΔS and DIBL

Tri-Gate R_{EXT}: Fin Aspect Ratio

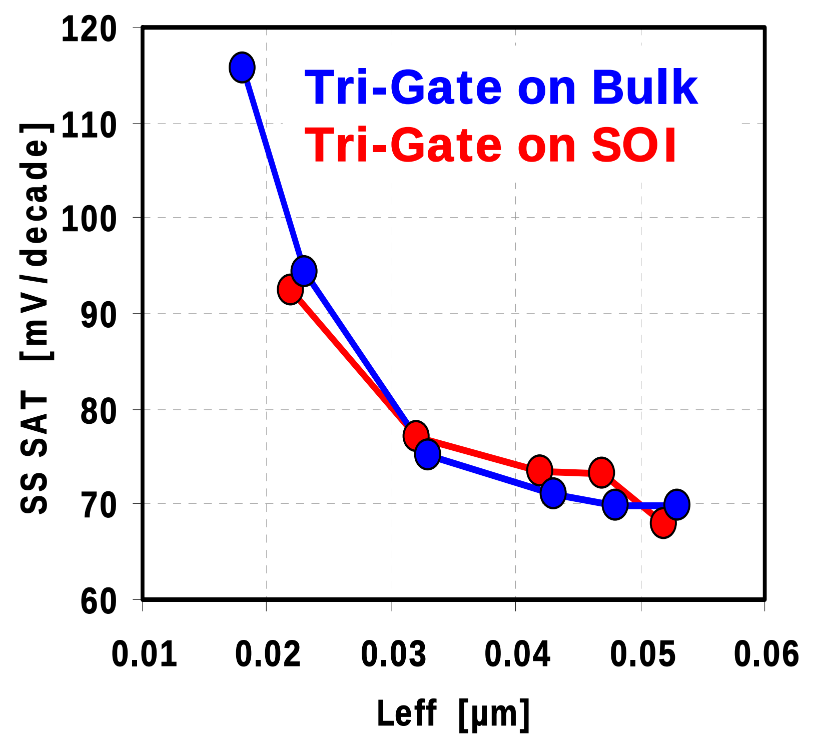


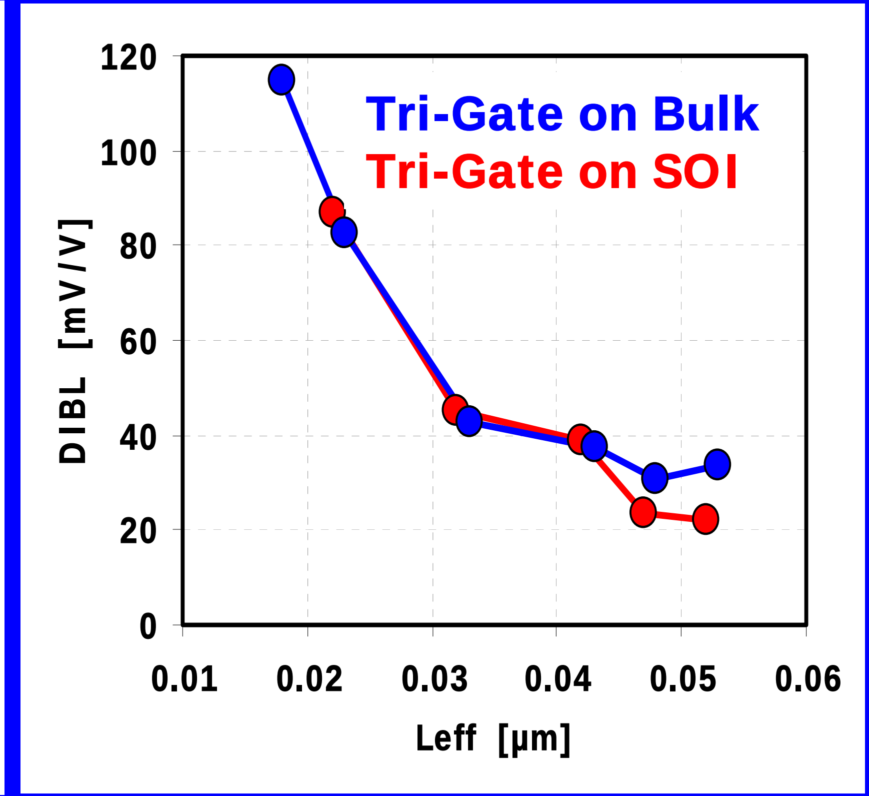


$Z_T = W_{Si} + 2*H_{Si}$

For a given W_{Si} increasing H_{Si} will lower R_{EXT} as the larger FIN/channel x-section improves current flow

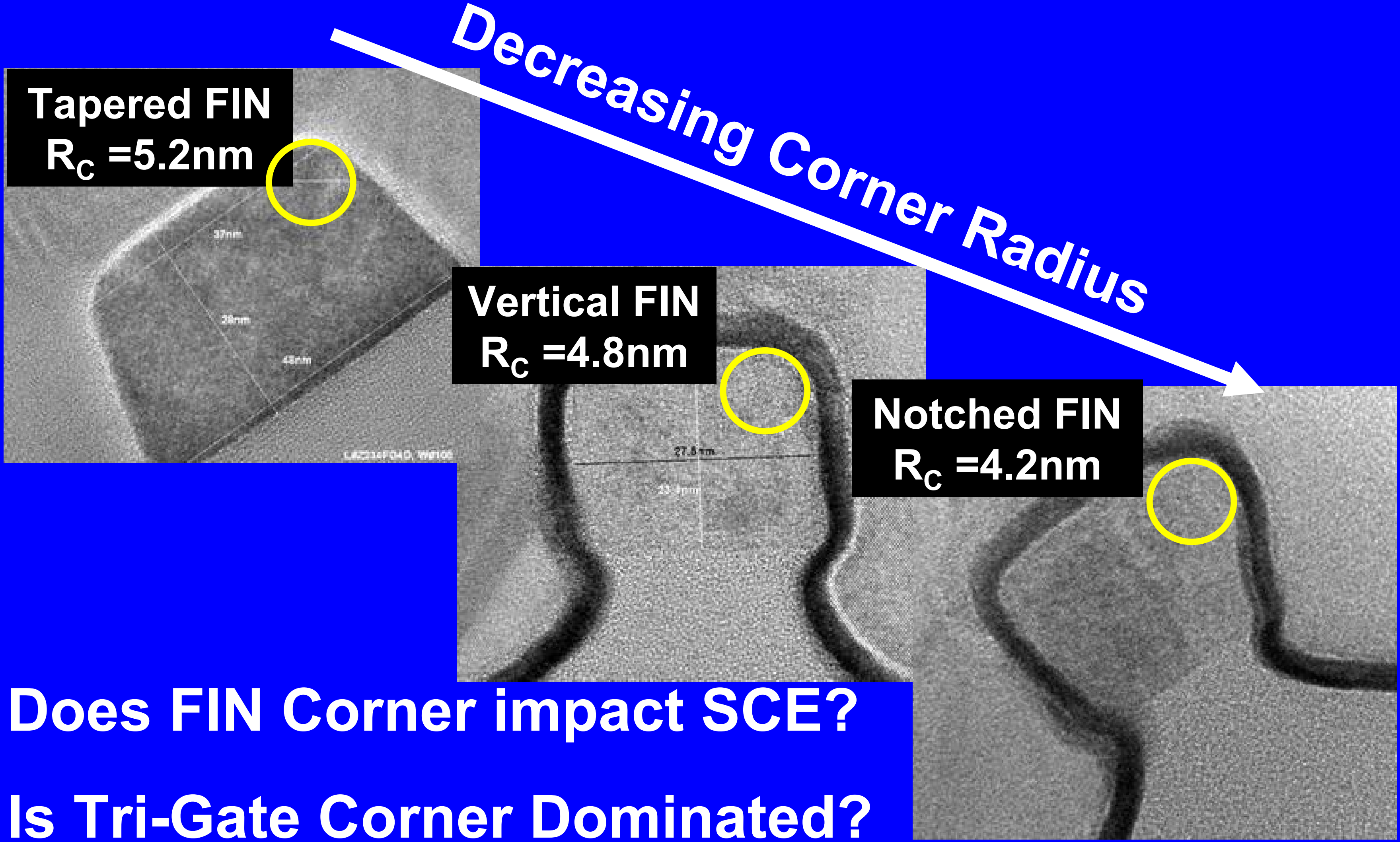
Equivalent Tri-Gate on Bulk and SOI





Trigate on Bulk-silicon and SOI substrates have similar short channel performance.

FIN Corner Rounding



Decreasing Corner Radius

Tapered FIN
R_C =5.2nm

Vertical FIN
R_C =4.8nm

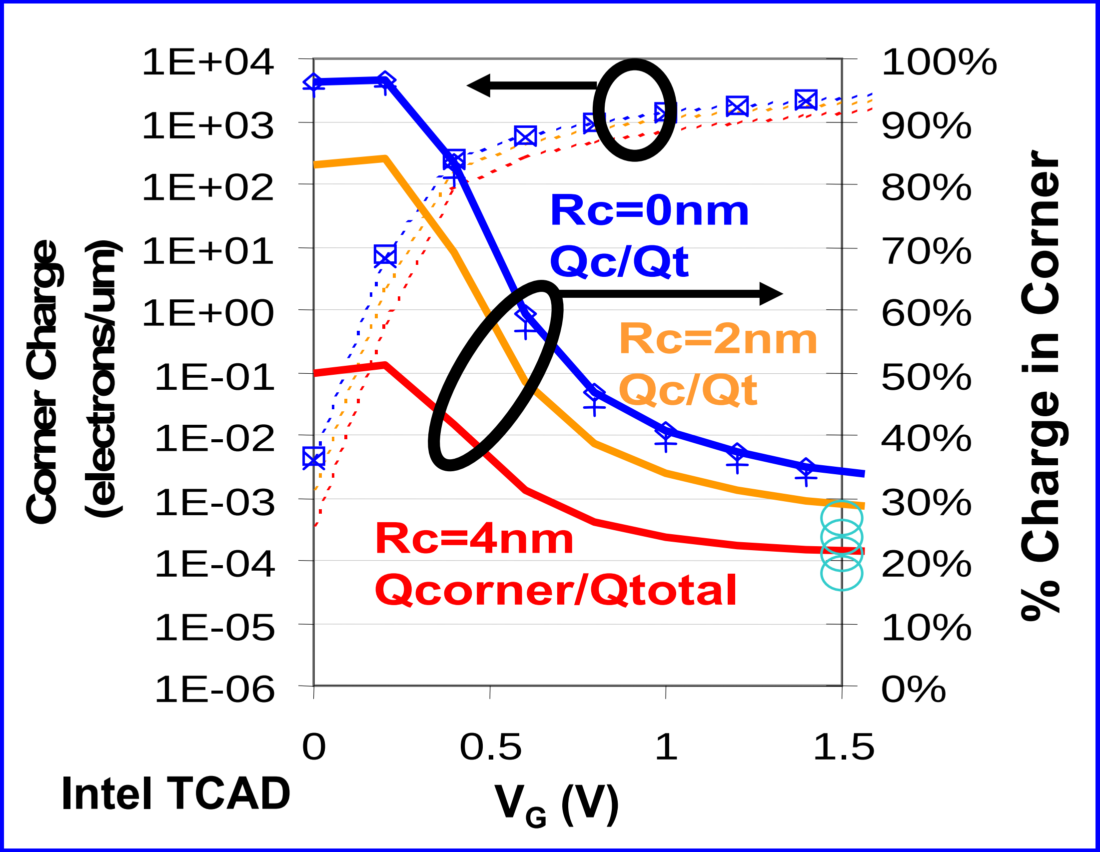
Notched FIN
R_C =4.2nm

Does FIN Corner impact SCE?

Is Tri-Gate Corner Dominated?

Tri-gate a Corner Device ?

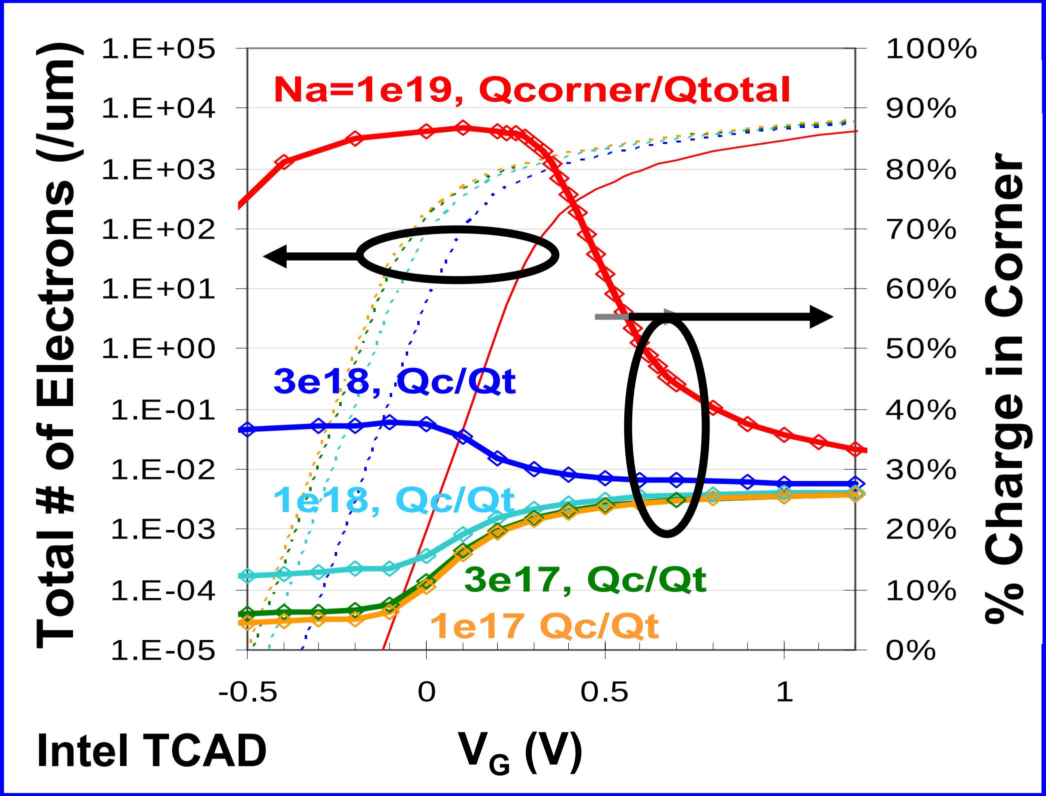
High FIN doping Na=1e19 cm^{-3}



Even for high FIN $N_A = 1 \times 10^{19}$ cm^{-3} an Rc ≥ 4nm reduces the corner transistor turn-on.

Tri-gate a Corner Device ?

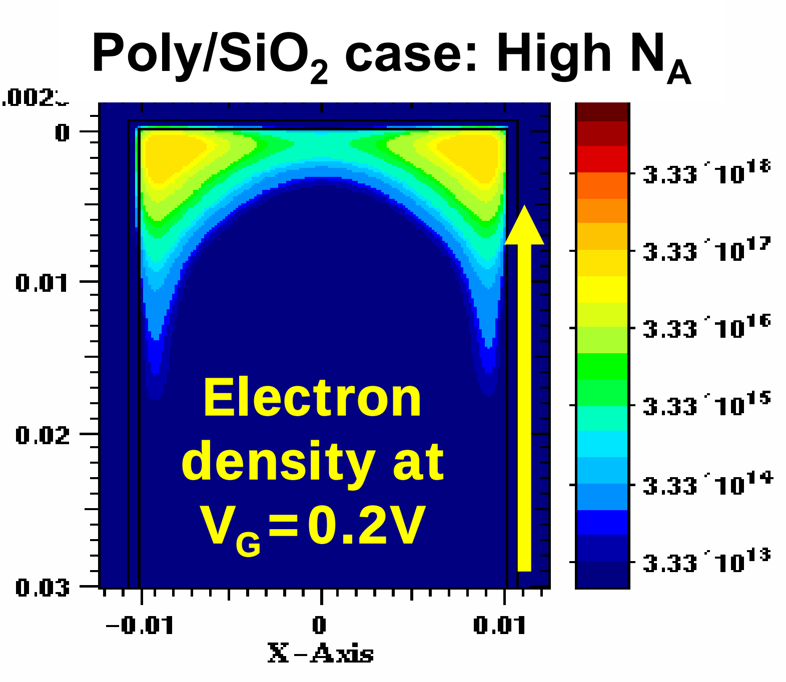
Perfect square corner (R_C=0nm)



High-k dielectrics & mid-gap metal gates enable lower FIN doping resulting in volume inversion and hence

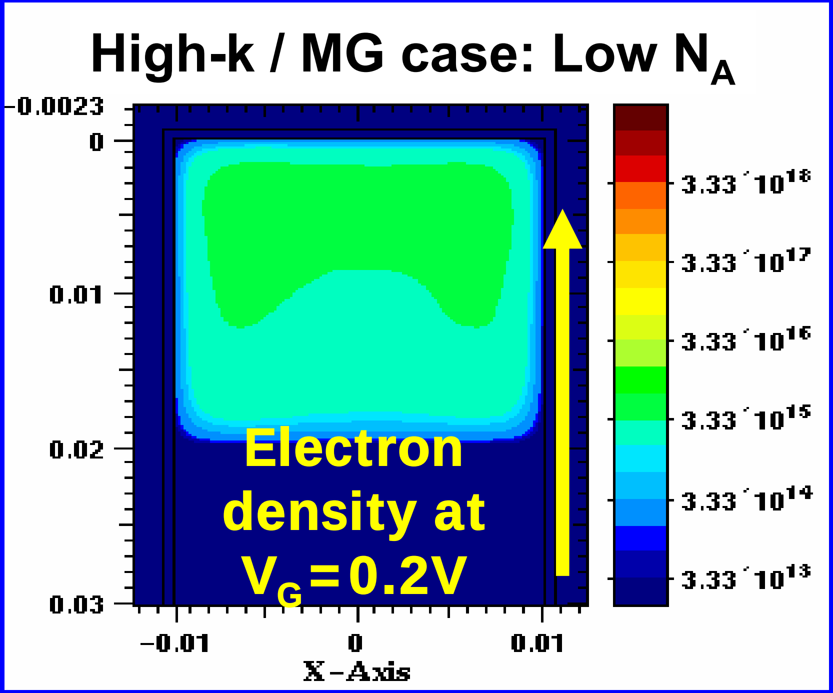
No corner effect

Corner Transistor Signature



Poly/SiO$_2$ case: High N_A

Electron density at V_G=0.2V

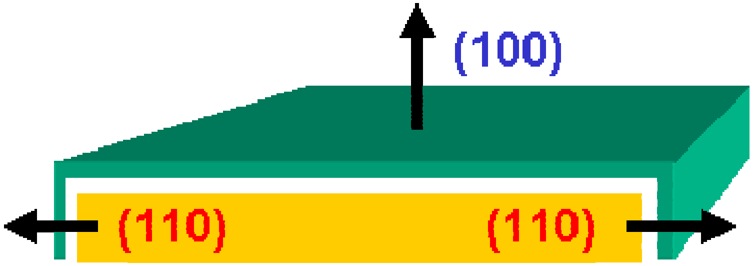


High-k / MG case: Low N_A

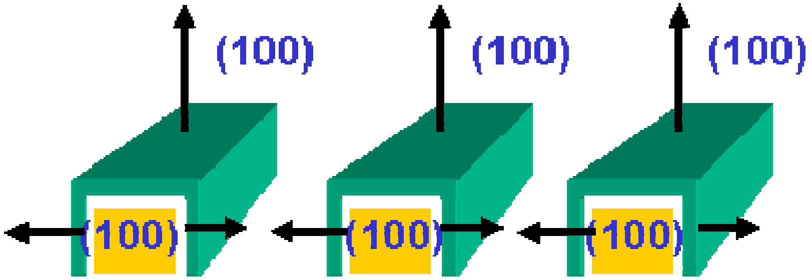
Electron density at V_G=0.2V

- Corner transistor is revealed at high body doping N_A
- The Hi-k/Metal Gate enables low body doping suppressing corner transistor turn-on.

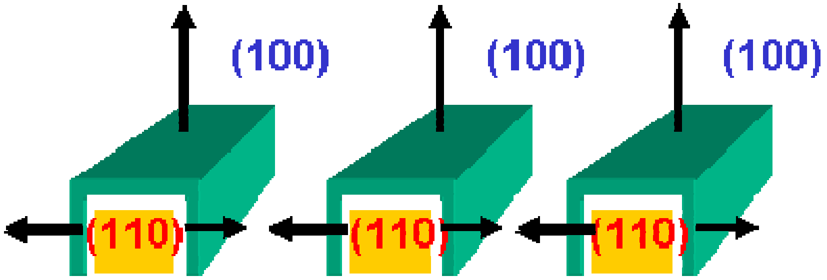
Tri-Gate Carrier Transport



Planar DST-like (long channel)

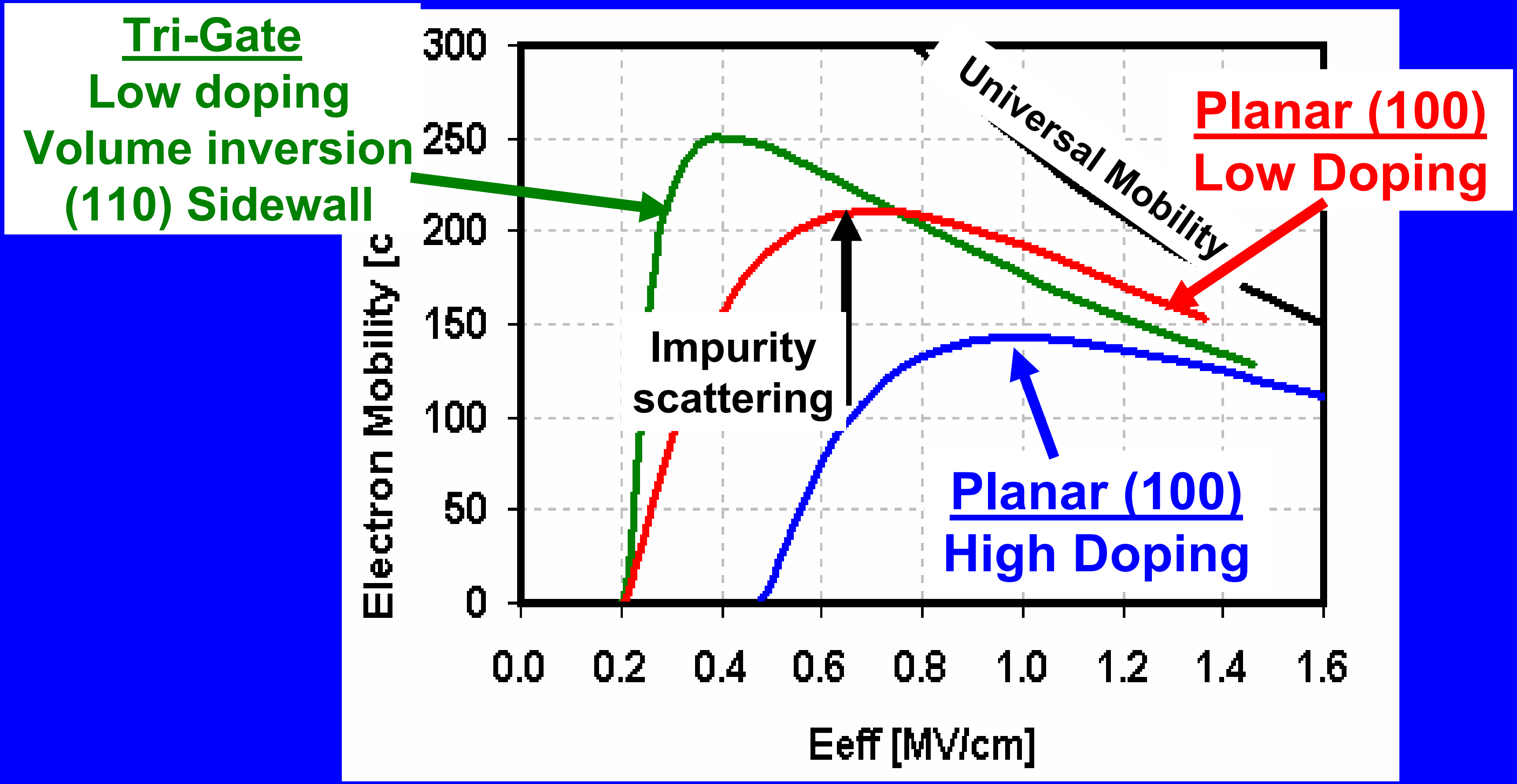


45° Rotated Trigate (long channel)



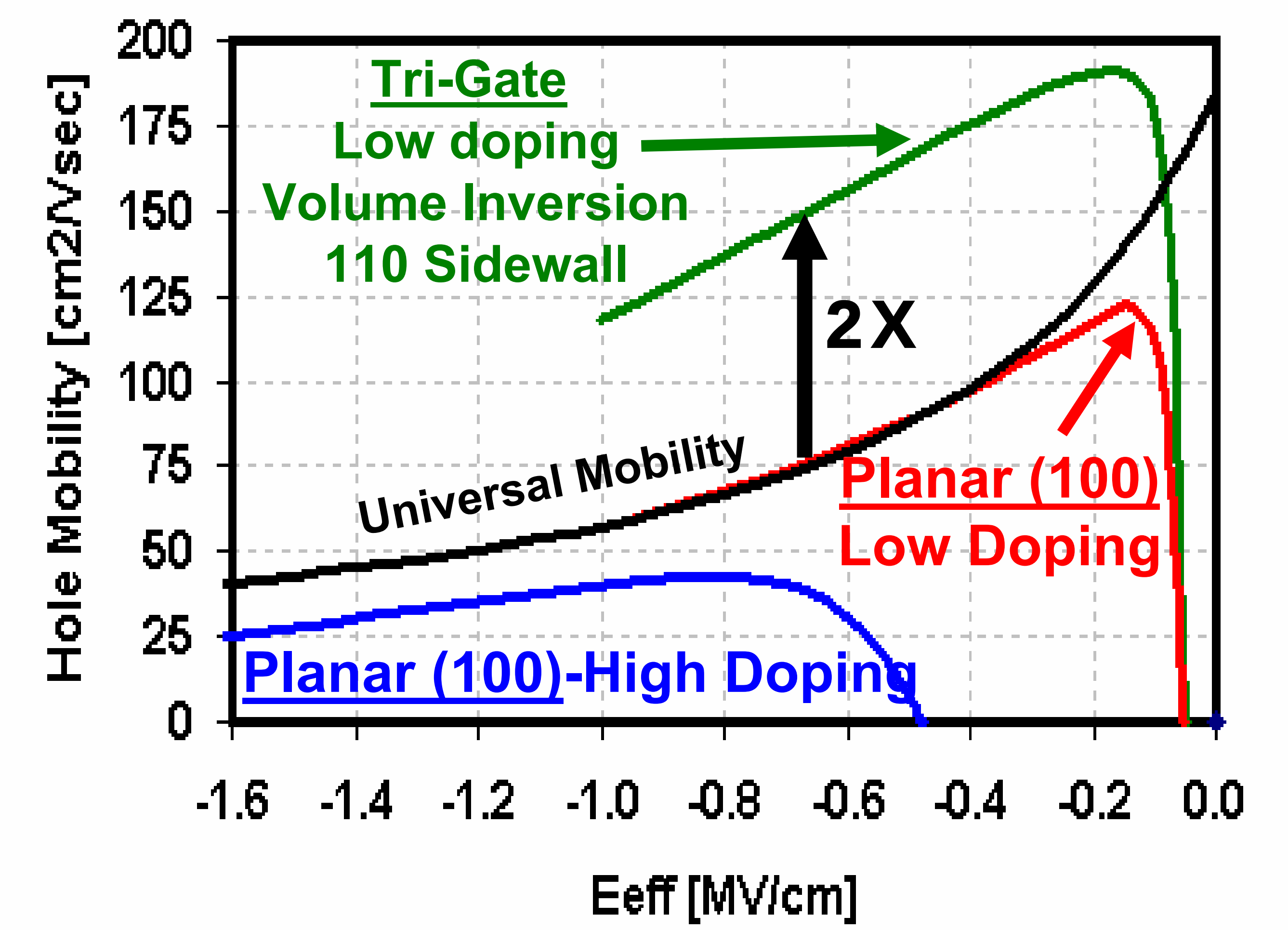
Normal (110) Trigate (long channel)

NMOS Tri-Gate Mobility (Long Channel)



- **40% long channel mobility improvement comes from low body doping in Tri-Gate at low to moderate vertical fields**
- **Minimal mobility degradation due to <110> sidewall and surface roughness scattering**

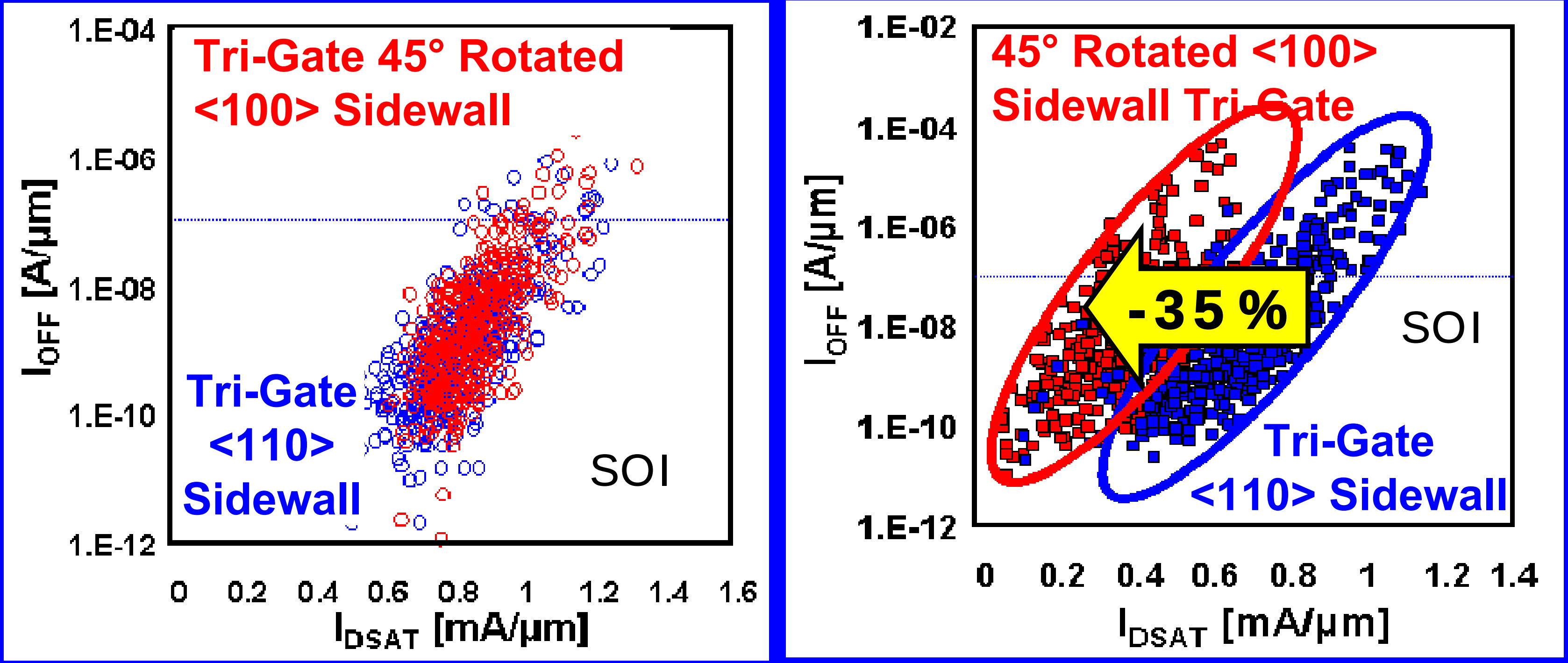
PMOS Tri-Gate Mobility (Long Channel)



Low doping and the <110> sidewall surface leads to over 2x increase in hole mobility

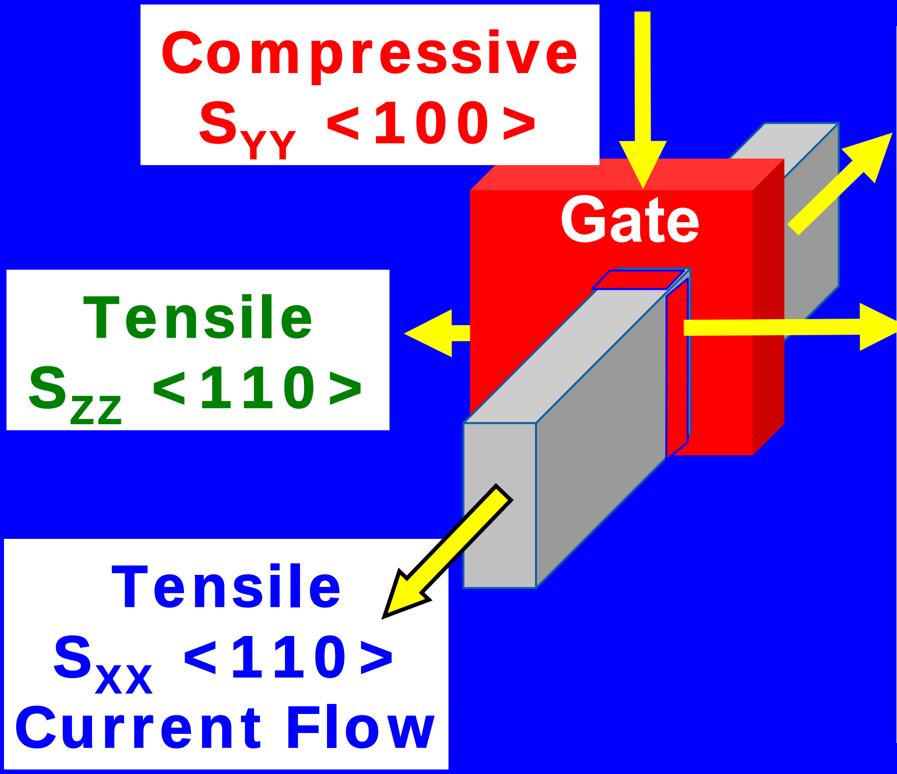
Tri-Gate Performance
(110) Sidewall vs. 45° Rotated (100)

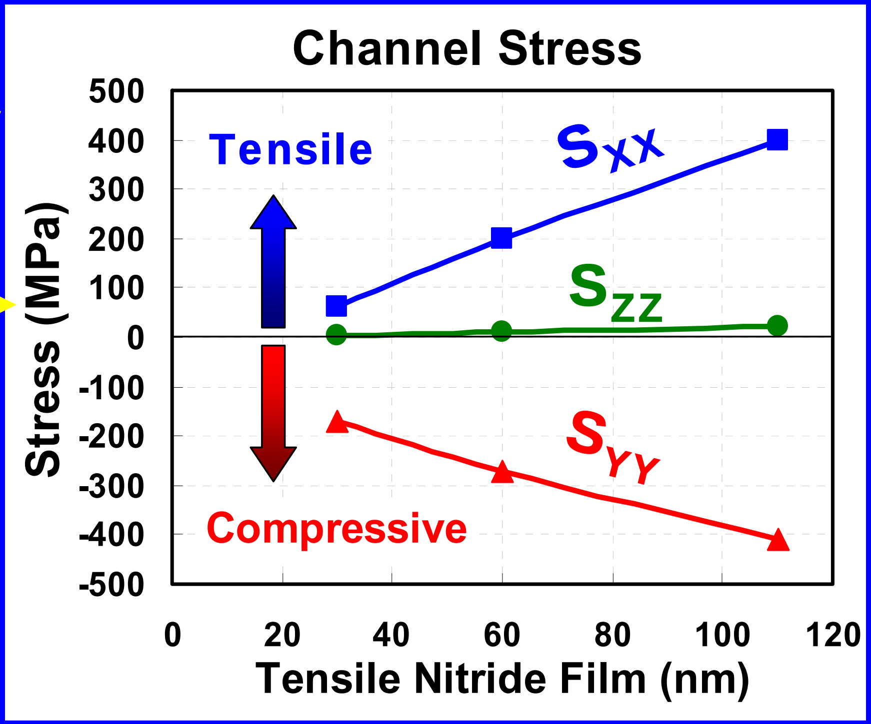
NMOS **PMOS**



Hybrid (45°- rotated) orientation substrates not needed for high performance CMOS Tri-Gates.

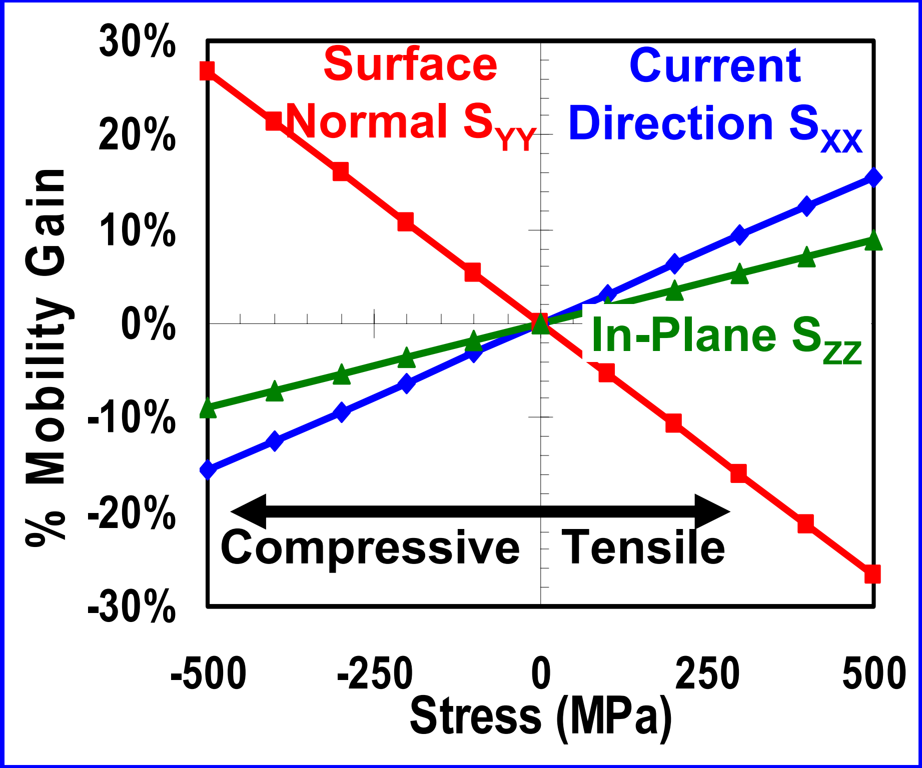
NMOS Tensile Nitride Film Stress





- S_{XX} & S_{YY} scale with nitride thickness, S_{ZZ} is invariant
- S_{XX} tensile, S_{YY} compressive, & S_{ZZ} slightly tensile

Tri-Gate NMOS Mobility vs. Strain

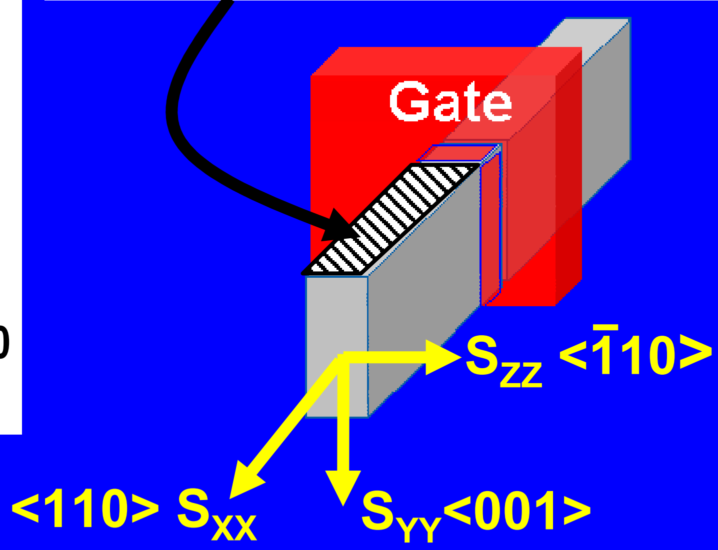


FIN Top Normal <001>

S_{XX}: Tensile →Current ✓

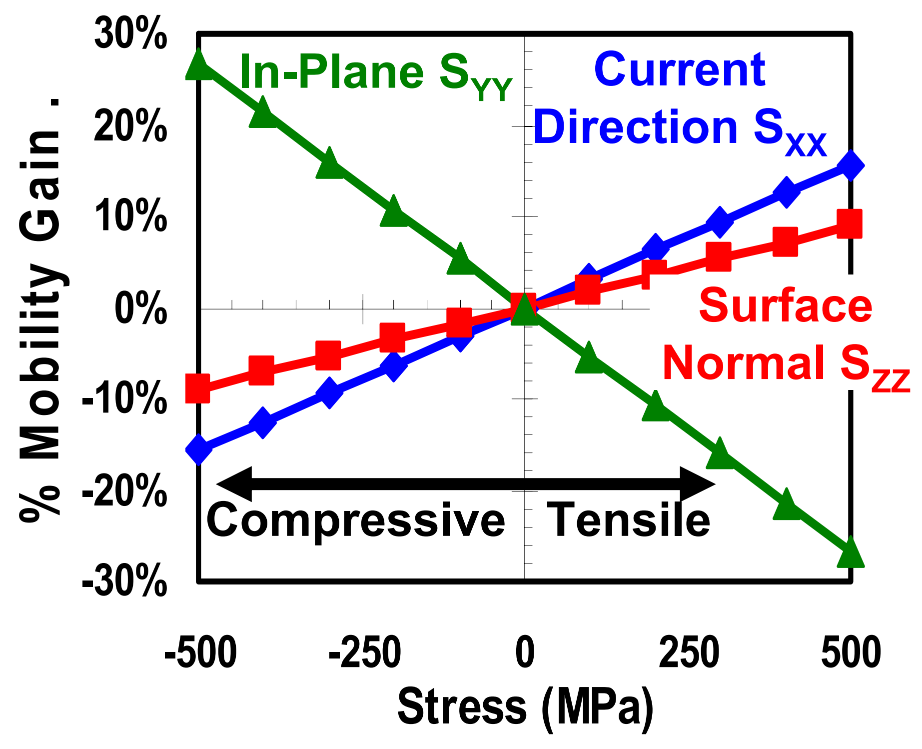
S_{YY}: Compr. →Normal ✓

S_{ZZ}: Tensile →In-Plane ✓



- All tensile film stresses improve NMOS Tri-Gate μ.
- Compressive S_{YY} stress has strongest impact on μ.

Tri-Gate NMOS Mobility vs. Strain

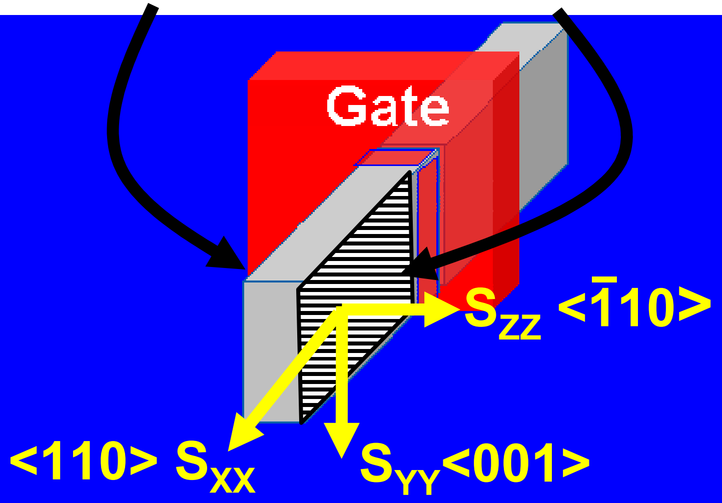


FIN Sidewall Norm. <110>

S_{XX}: Tensile → Current ✓

S_{YY}: Compr. → In-plane ✓

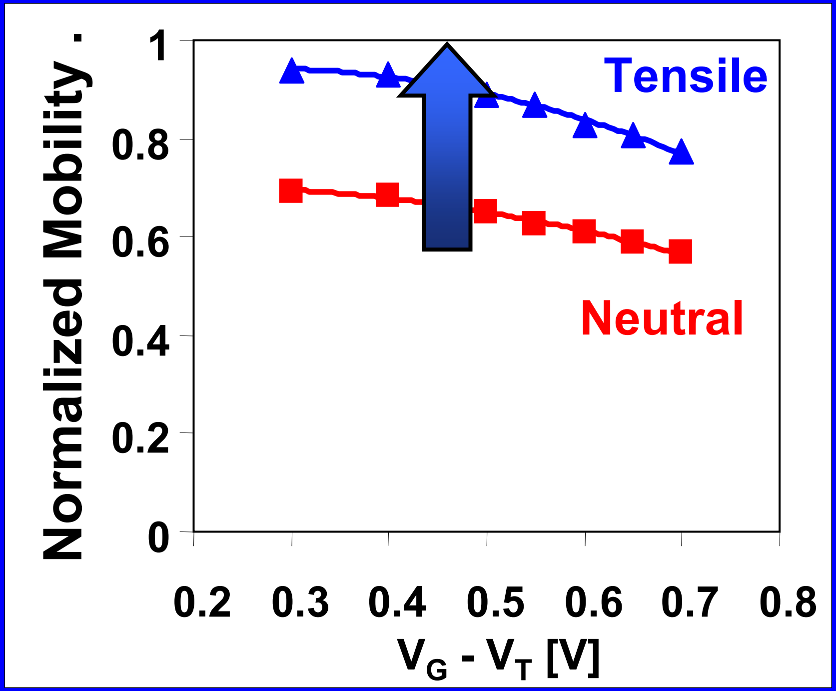
S_{ZZ}: Tensile → Normal ✓



- All tensile film stresses improve NMOS Tri-Gate μ.
- Compressive S_{YY} stress has strongest impact on μ.

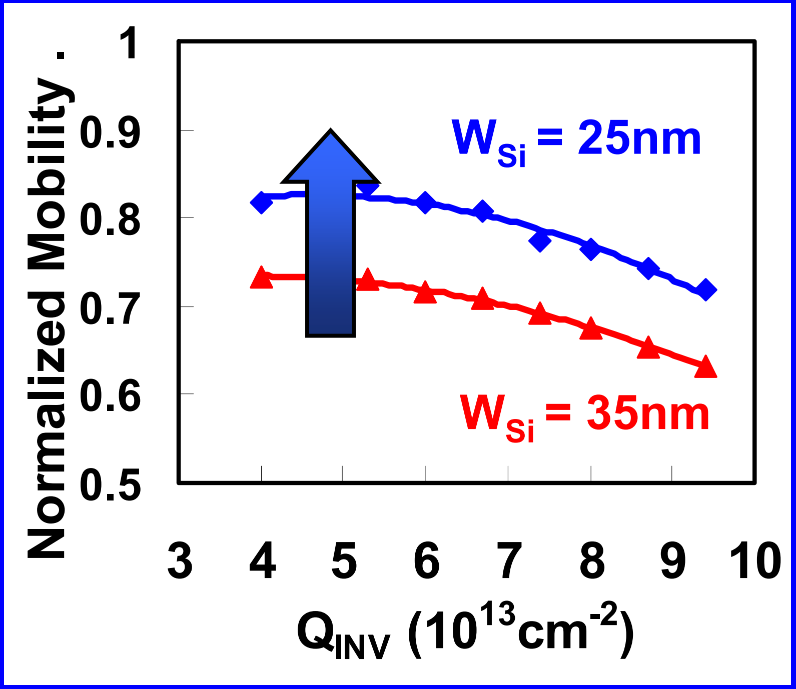
Short Channel Tri-Gate NMOS

Mobility vs. Film Stress



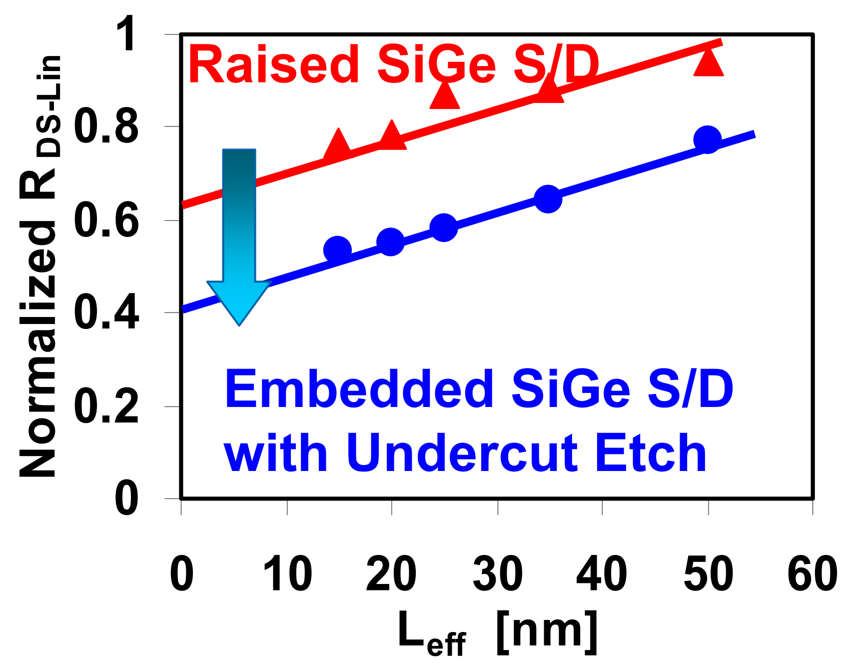
Tensile nitride film stress significantly enhances short channel electron μ

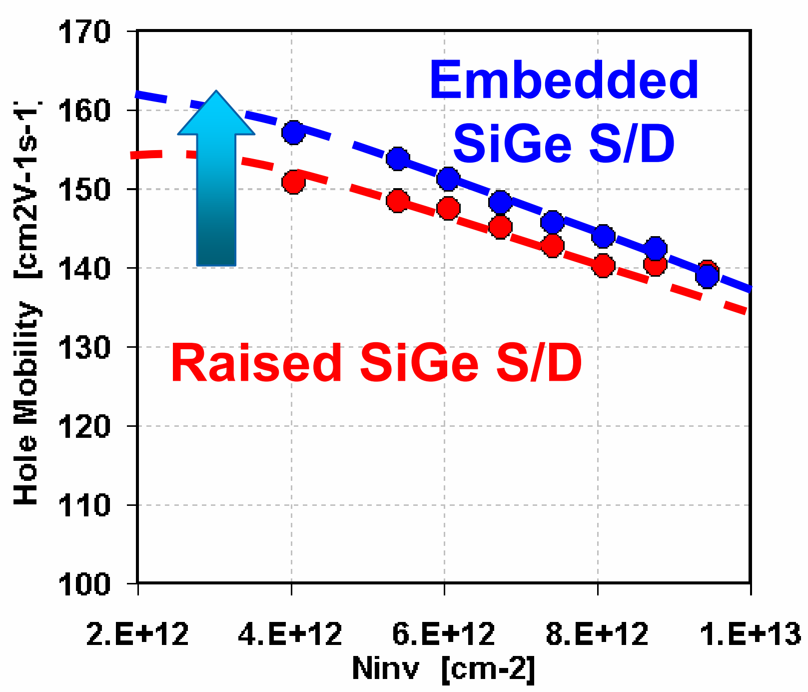
Mobility vs. W_{Si} (Tensile)



Tensile nitride film stress and electron μ increase as the FIN W_{Si} decreases

Short Channel Tri-Gate PMOS

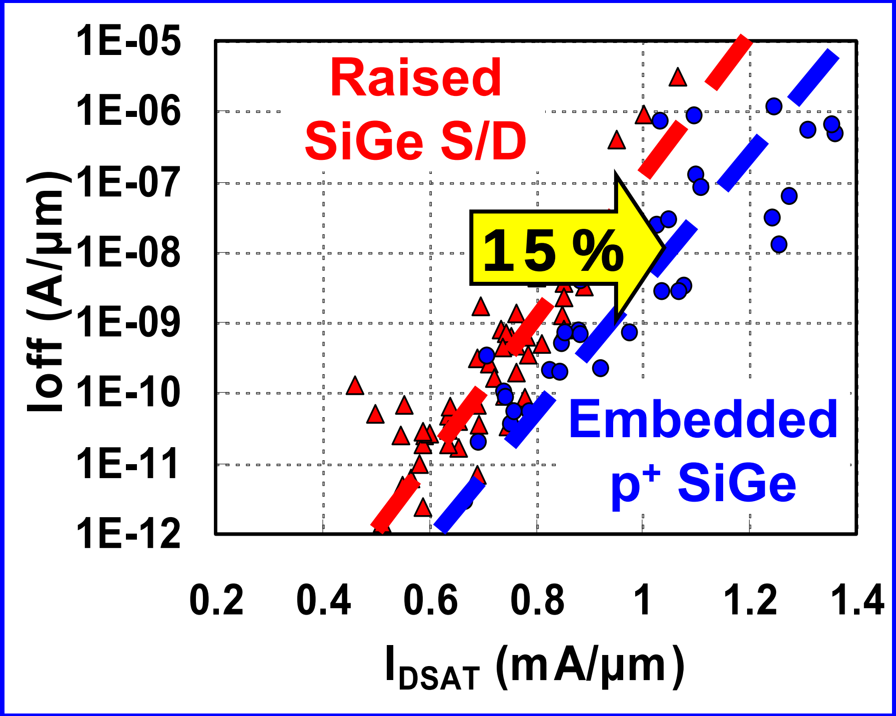


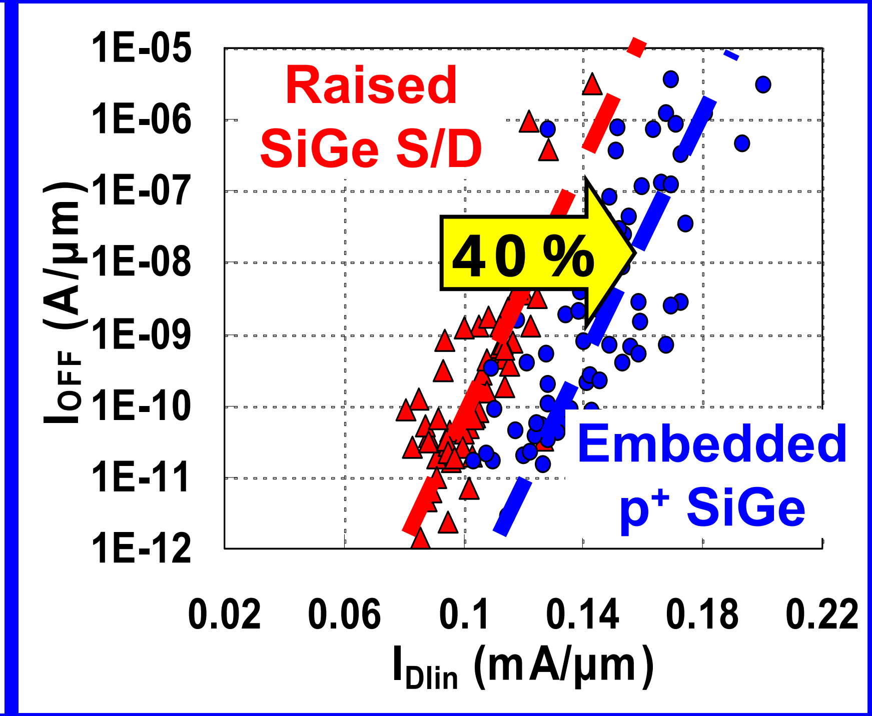


Embedding the p^+ SiGe S/D regions with under-cut etch provides 40% lower R_{DSLIN}

Uniaxial compressive strain is observed in short-channel Tri-Gate

Short Channel Tri-Gate PMOS

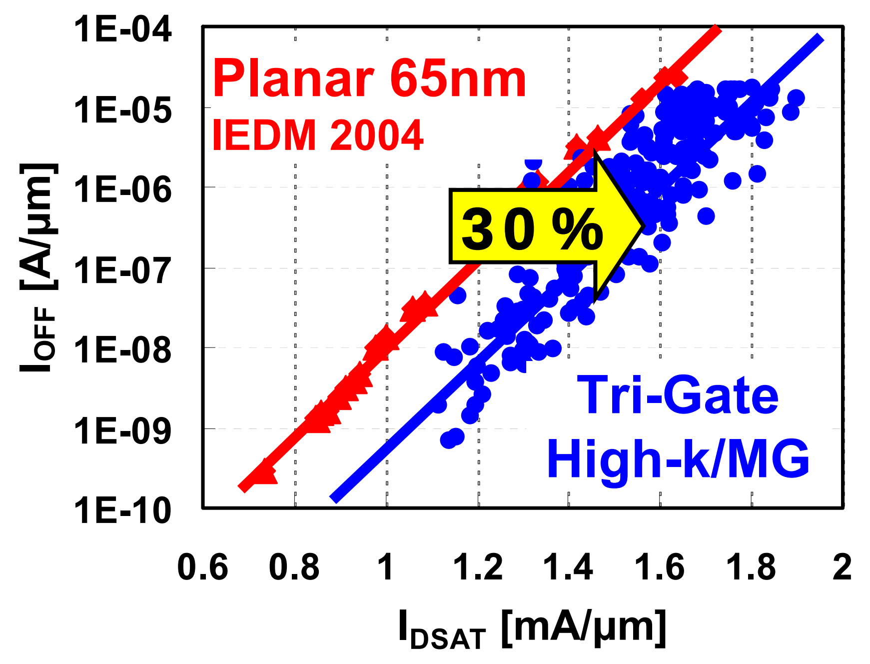




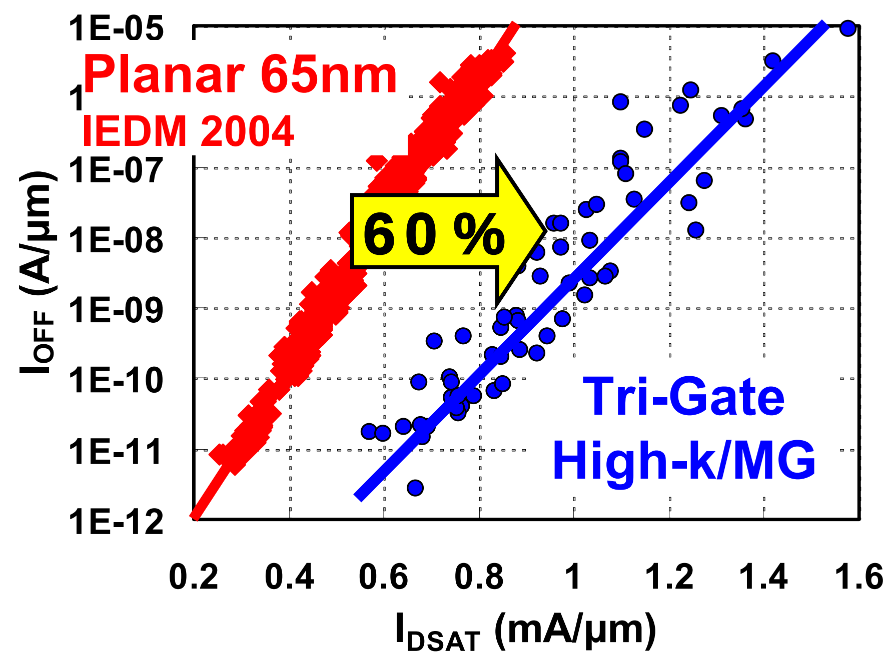
Embedding the p^+ SiGe S/D regions with an under-cut etch provides a 15% I_{DSAT} & 40% I_{DLIN} benefit.

Industry Leading Performance

NMOS



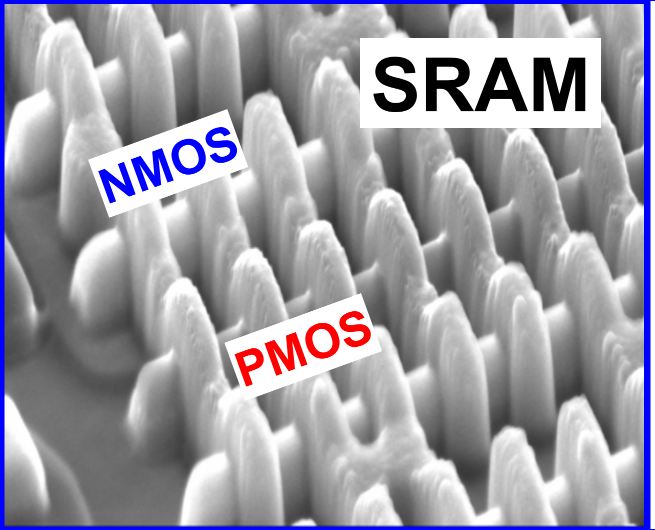
PMOS

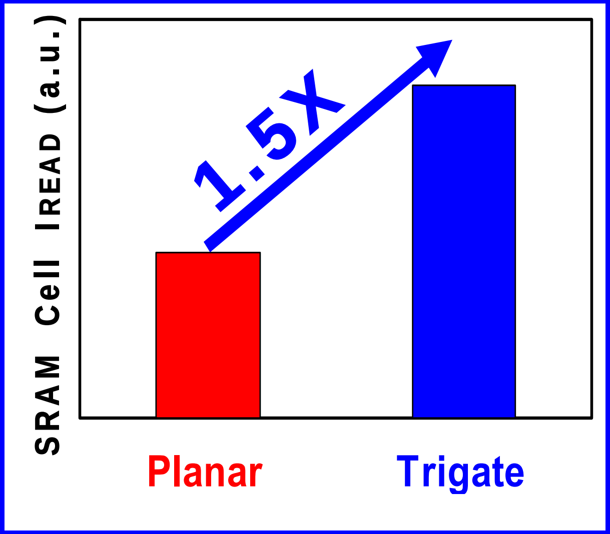


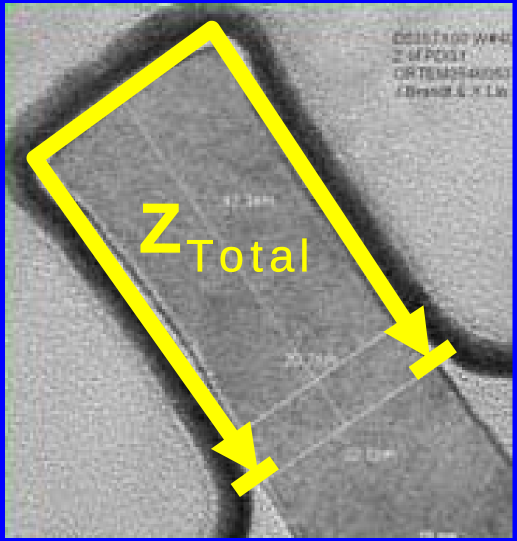
Integrated CMOS Tri-Gate with:

1. High-k dielectrics & metal gate
2. Strain engineering for NMOS & PMOS
3. Dual epitaxial raised source/drains

Integrated Tri-Gate CMOS







Demonstrated functional Tri-gate SRAM cells

For equivalent cell size Tri-Gate SRAM cell shows 1.5x higher cell I_{READ} due to higher $Z_T = 2 * H_{Si} + W_{Si}$

Conclusions

1. Highly scalable Tri-Gate architecture with excellent short channel effects and record performance.
2. Bulk-Si Tri-Gate demonstrates equivalent scaling and performance to SOI Tri-Gate.
3. High-k/Metal Gate, corner rounding and low doping eliminate any parasitic corner device turn-on.
4. Tri-Gate PMOS mobility shows 2x enhancement due to <110> sidewalls over <100> planar devices while NMOS is neutral.
5. Functional Tri-Gate SRAM cell demonstrated with 1.5X the cell read current due to the increase in Z_{Total} per cell footprint.