Enhancement and Depletion mode InSb Quantum Well Transistors for High Speed and Low Power Logic Applications

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Outline

- Motivation
- Materials
- Transistors
- Gate Dielectrics
- Benchmarking
- Opportunities and Challenges

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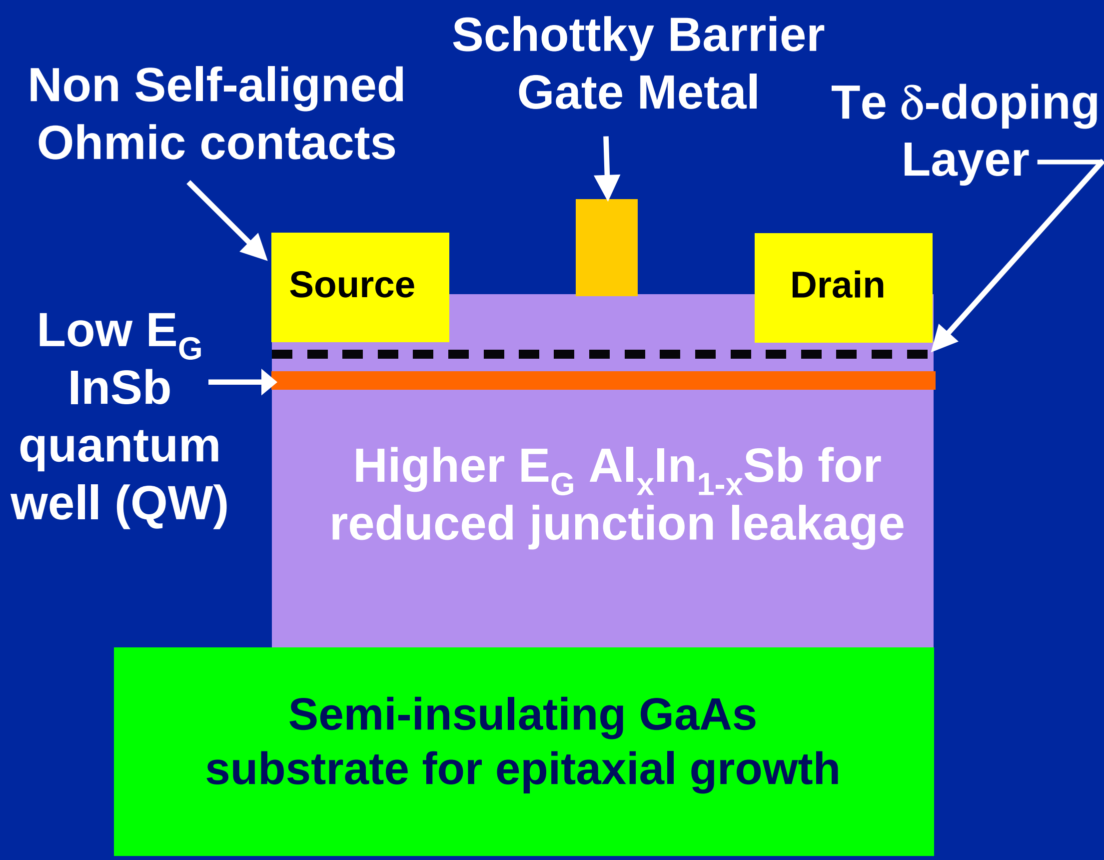
Channel Material Properties

	Si	GaAs	$In_{.53}Ga_{.47}As$	InAs	**InSb**
Electron Mobility ($cm^2V^{-1}s^{-1}$) @ n_s=1x10^{12}/cm^2	600	4,600	7,800	20,000	**30,000**
Electron Saturation Velocity (10^7 cm/s)	1.0	1.2	0.8	3.5	**5.0**
Ballistic Mean Free Path (nm)	28	80	106	194	**226**
Energy Band-gap (eV)	1.12	1.42	0.72	0.36	**0.18**

InSb has the highest room temperature mobility, but also the lowest energy band-gap

InSb Quantum Well Transistor



Layer	Material	Thickness (nm)
Top Barrier	$Al_xIn_{1-x}Sb$	15-45
Doping	Te	-
Spacer	$Al_xIn_{1-x}Sb$	5
Channel	InSb	15-20
Metamorphic Buffer	$Al_yIn_{1-y}Sb$	3,000
Substrate	GaAs	

- Junctions are formed in the higher band-gap barrier layers
- High speed carrier transport occurs in the low band-gap InSb quantum well (QW)

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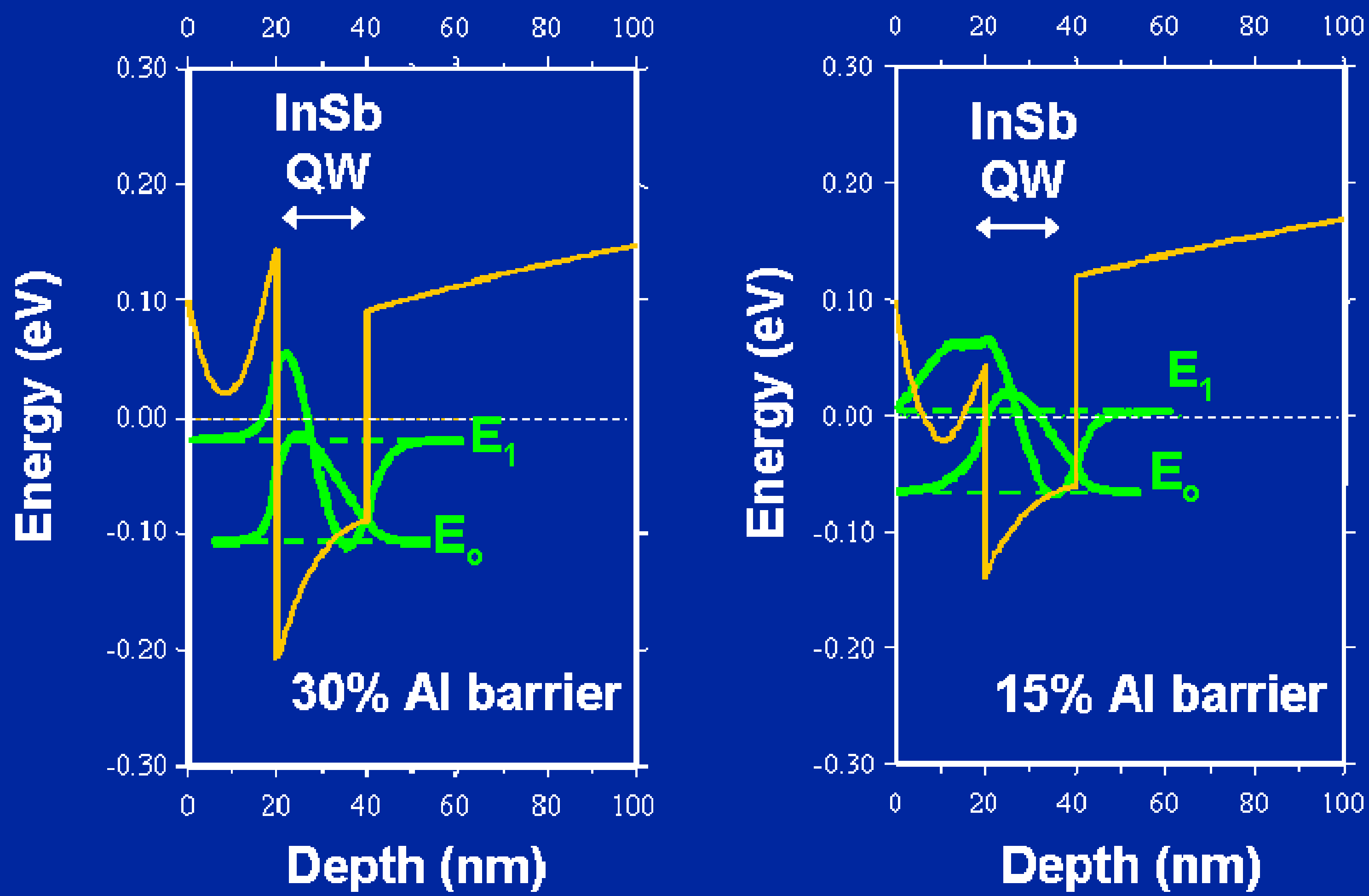
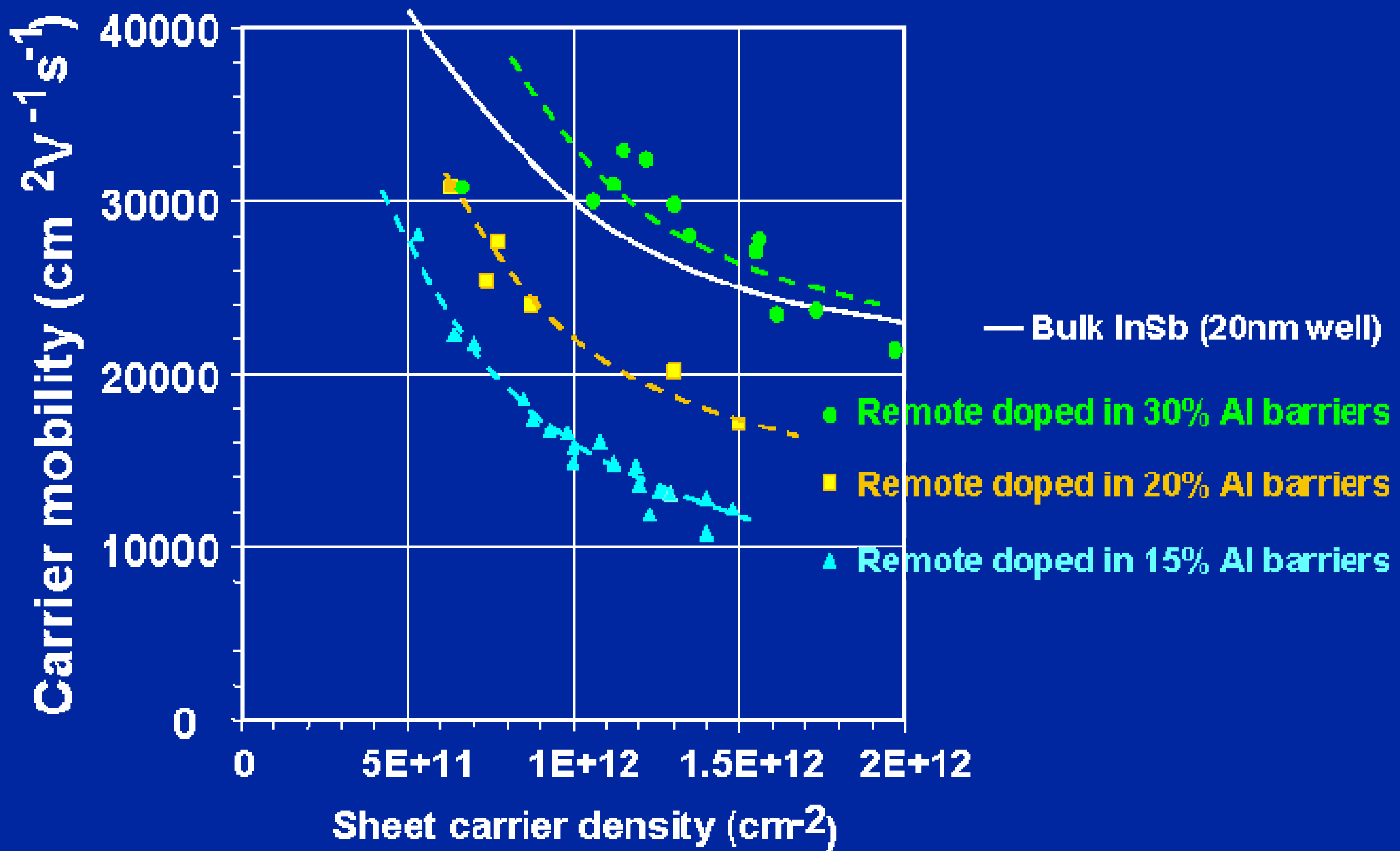
Carrier Confinement in InSb QW



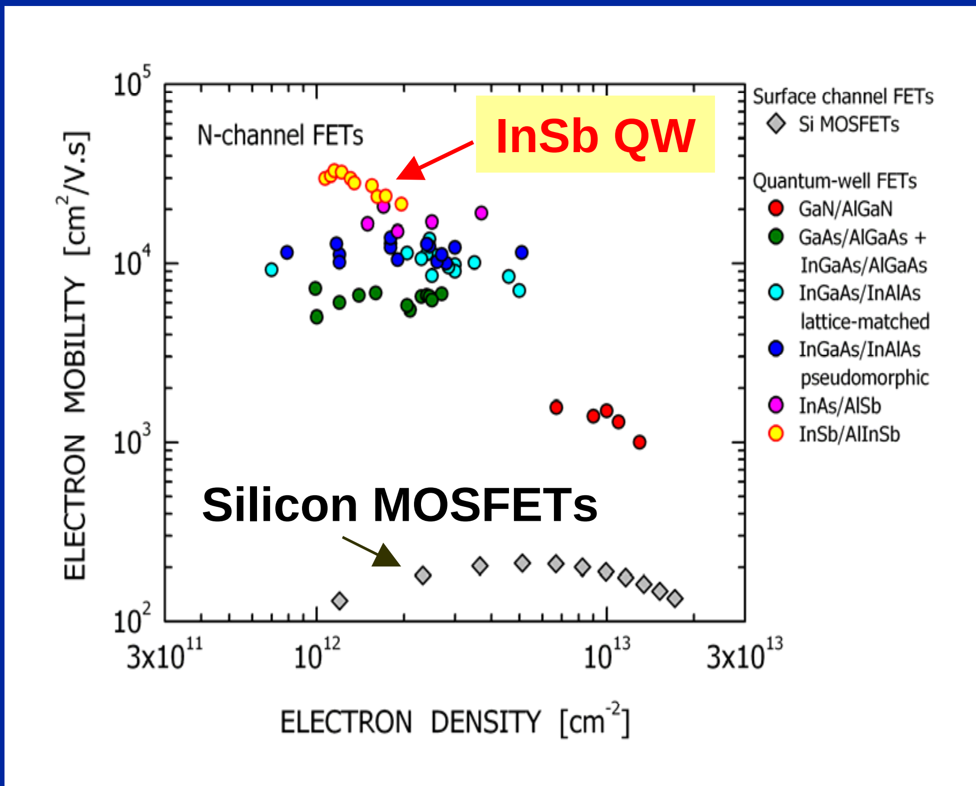
Band-gap engineering is utilized to confine electrons within the InSb QW at high carrier densities

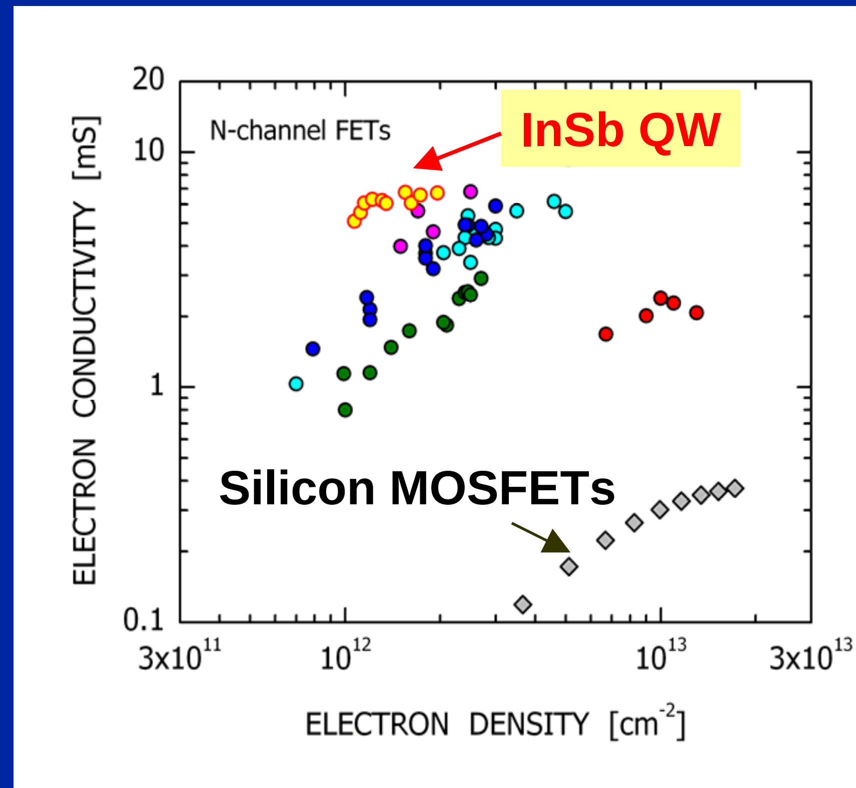
Hall Mobility of InSb QW



Room temperature InSb QW mobility over 30,000 $cm^2V^{-1}s^{-1}$ is achieved with 30% Al barrier at $n_s = 1.3\times10^{12}$ cm^{-2}

Mobility and Carrier Concentration





- **Highest conductivity and lower carrier density in InSb QW transistors (QWFET)**
  - **Attractive for gate capacitance dominated circuits**
  - **Less suitable for interconnect dominated circuits**

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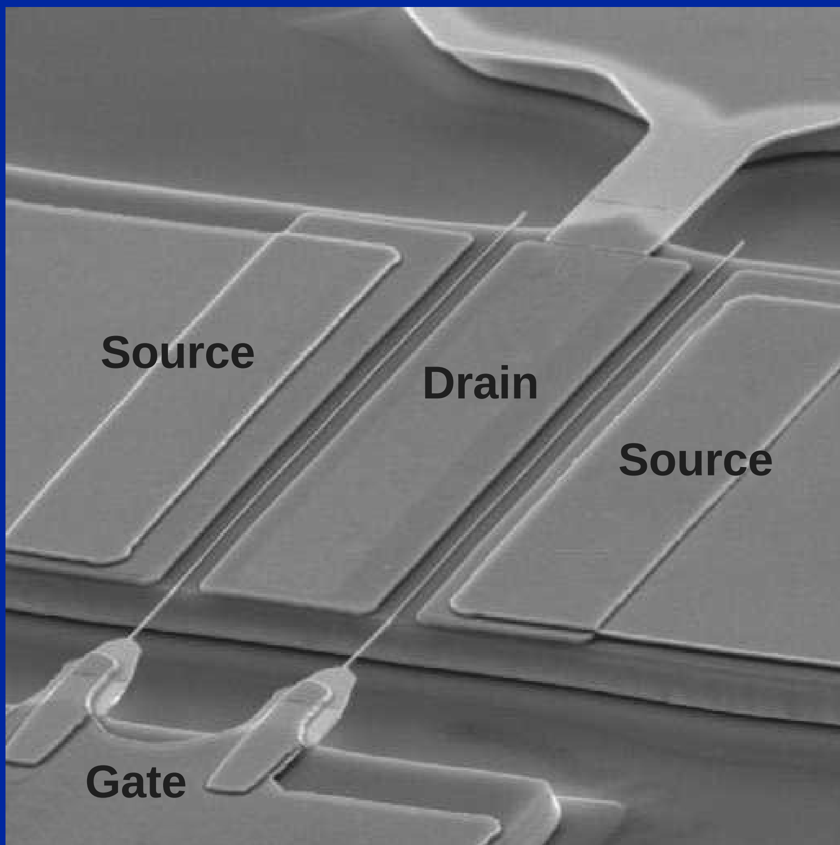
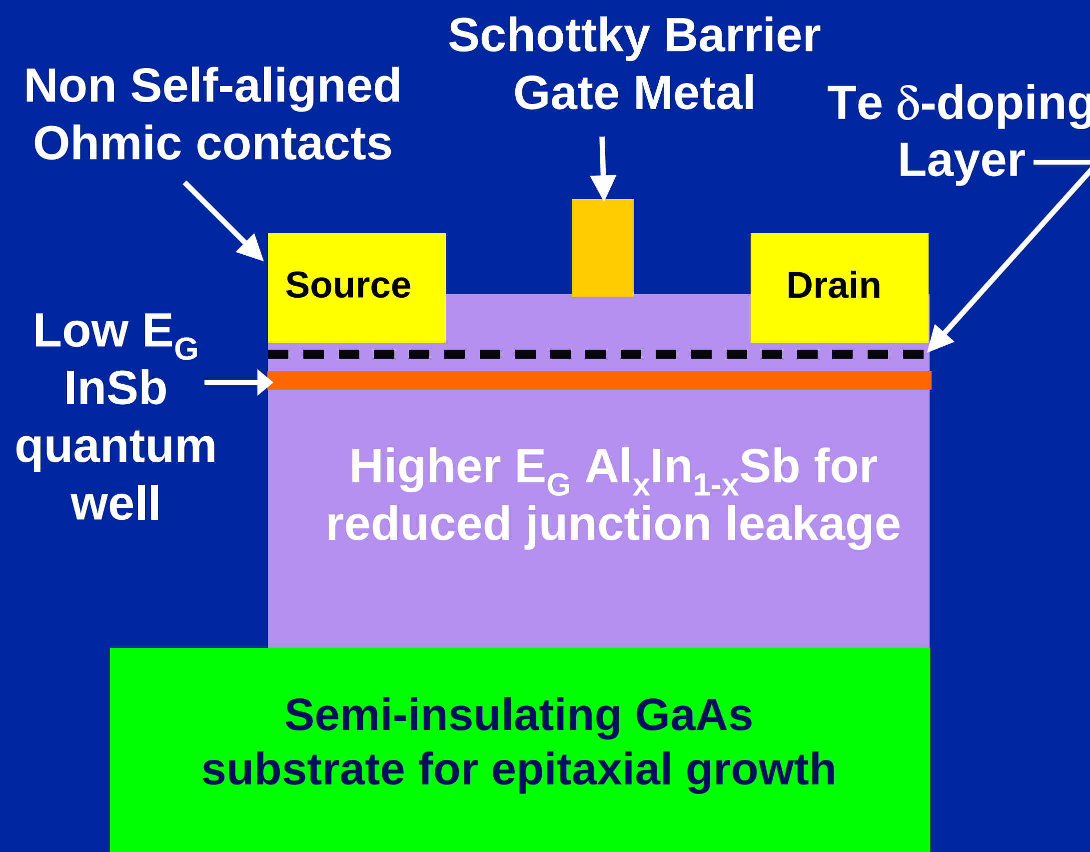
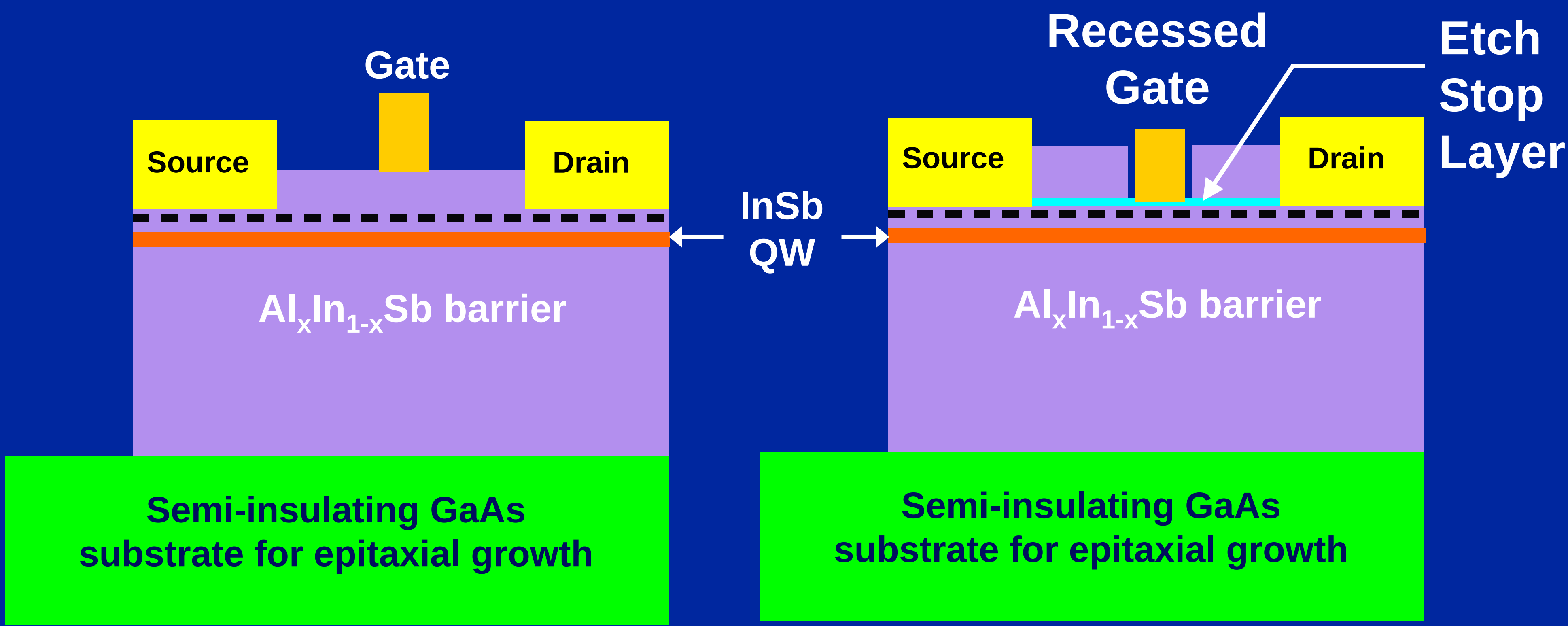
InSb QW Transistor Fabrication





A two gate finger InSb QW transistor (QWFET) is fabricated with gate air-bridge using mesa isolation

Depletion and Enhancement Mode

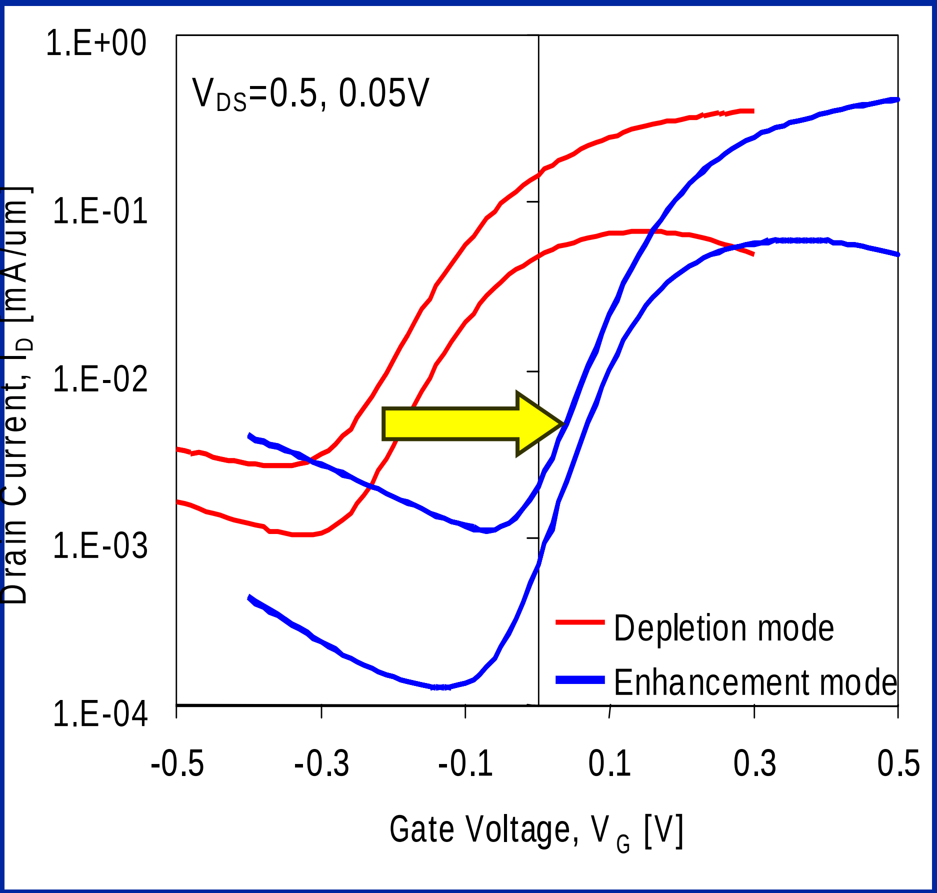


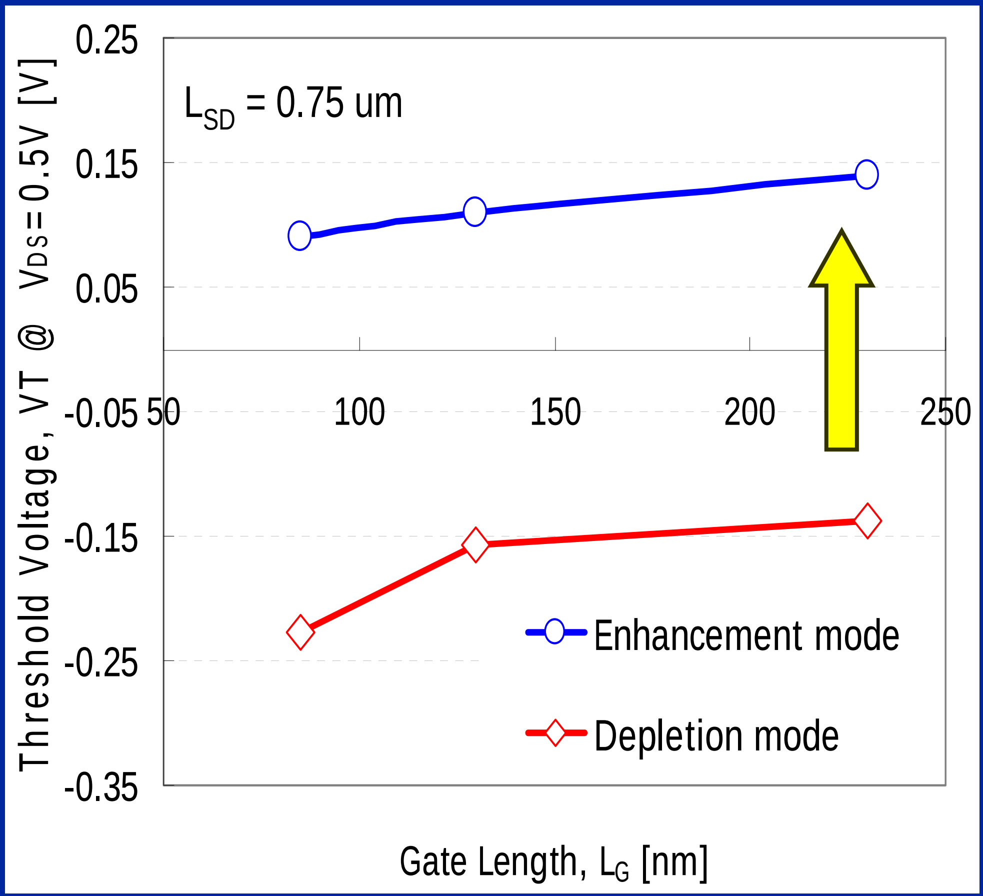
Depletion mode
(Normally ON)

Enhancement mode
(Normally OFF)

A novel gate recess process is used to fabricate enhancement mode InSb QWFETs

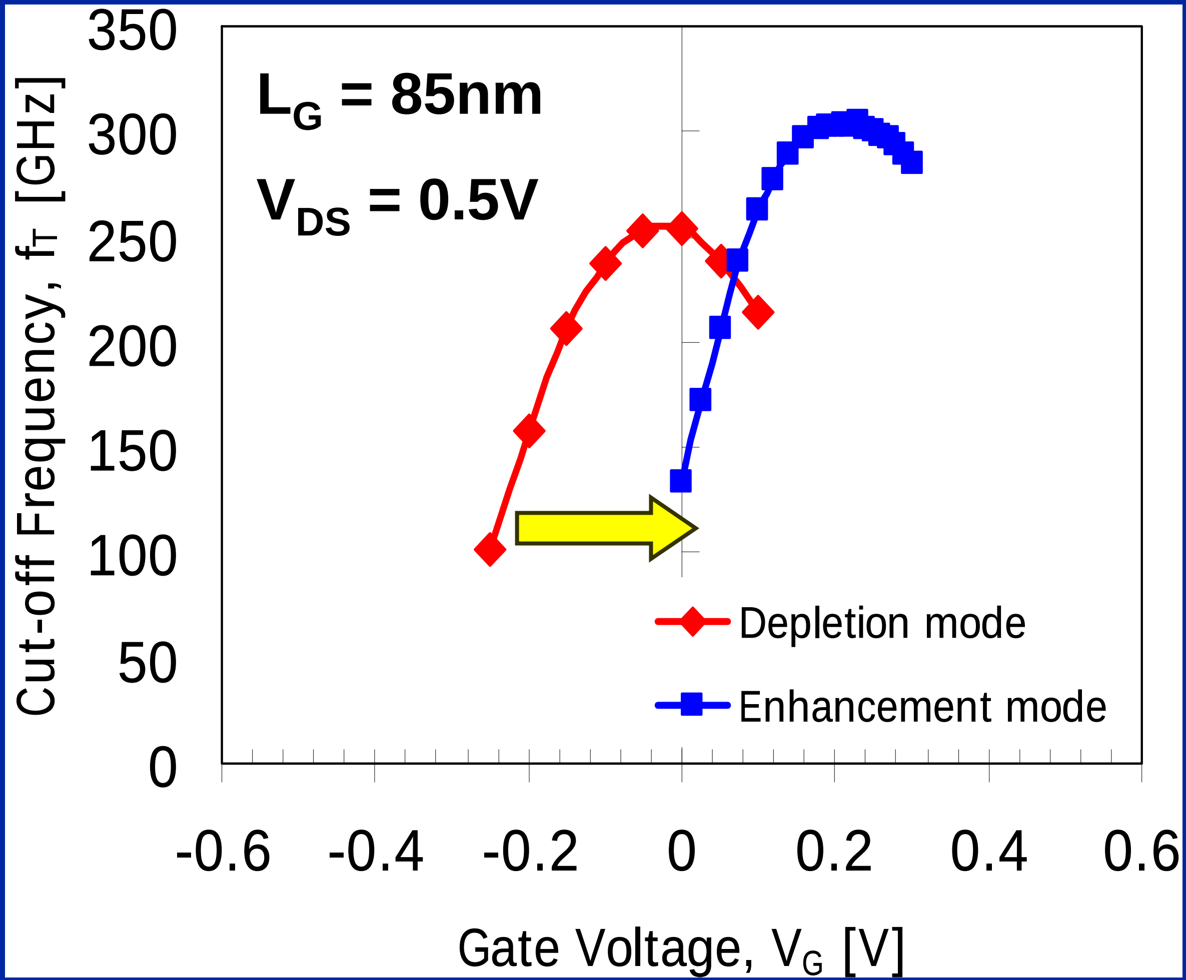
Depletion and Enhancement Mode





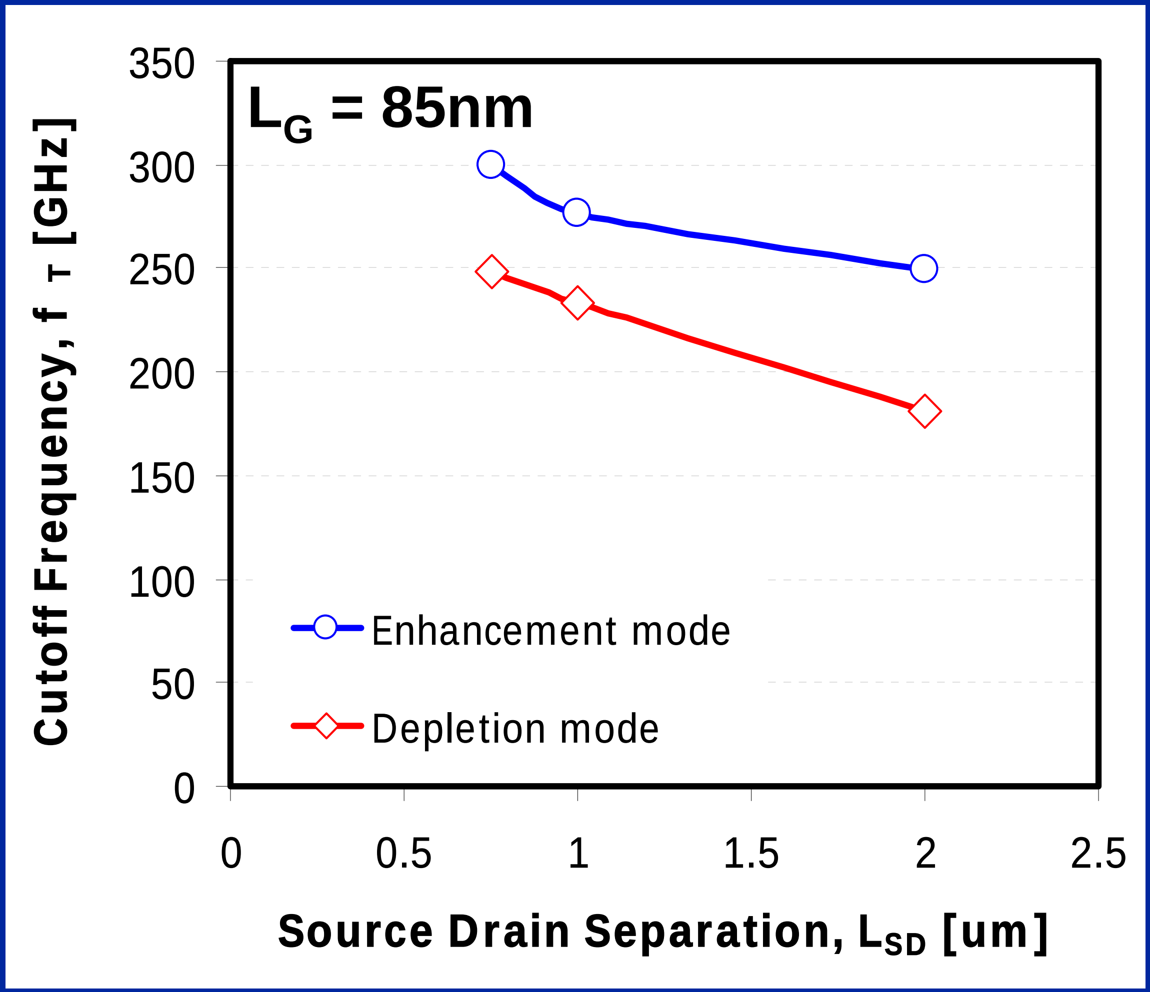
Gate recess is carefully optimized to set the threshold voltage of the InSb QWFETs

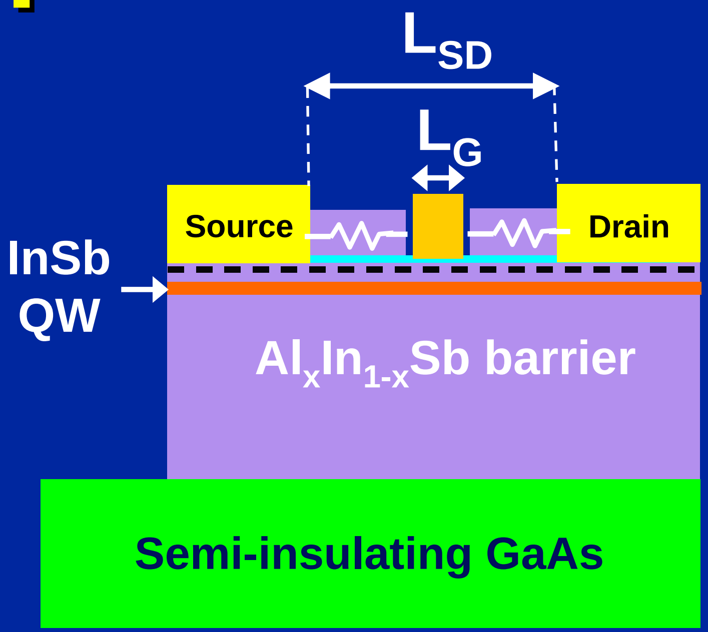
Depletion and Enhancement Mode

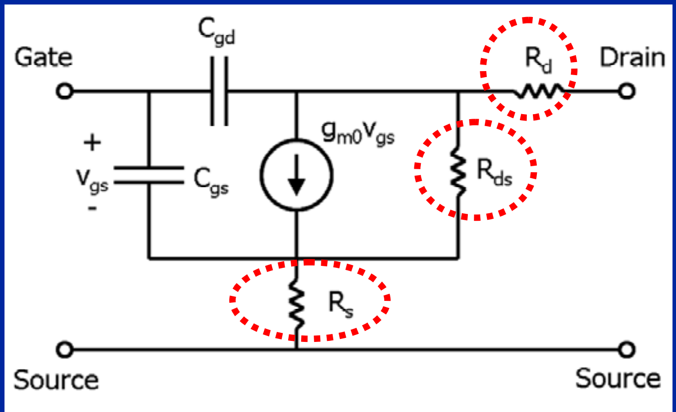


Enhancement mode InSb QWFETs achieve record intrinsic switching speed of 305 GHz

Source to Drain Separation



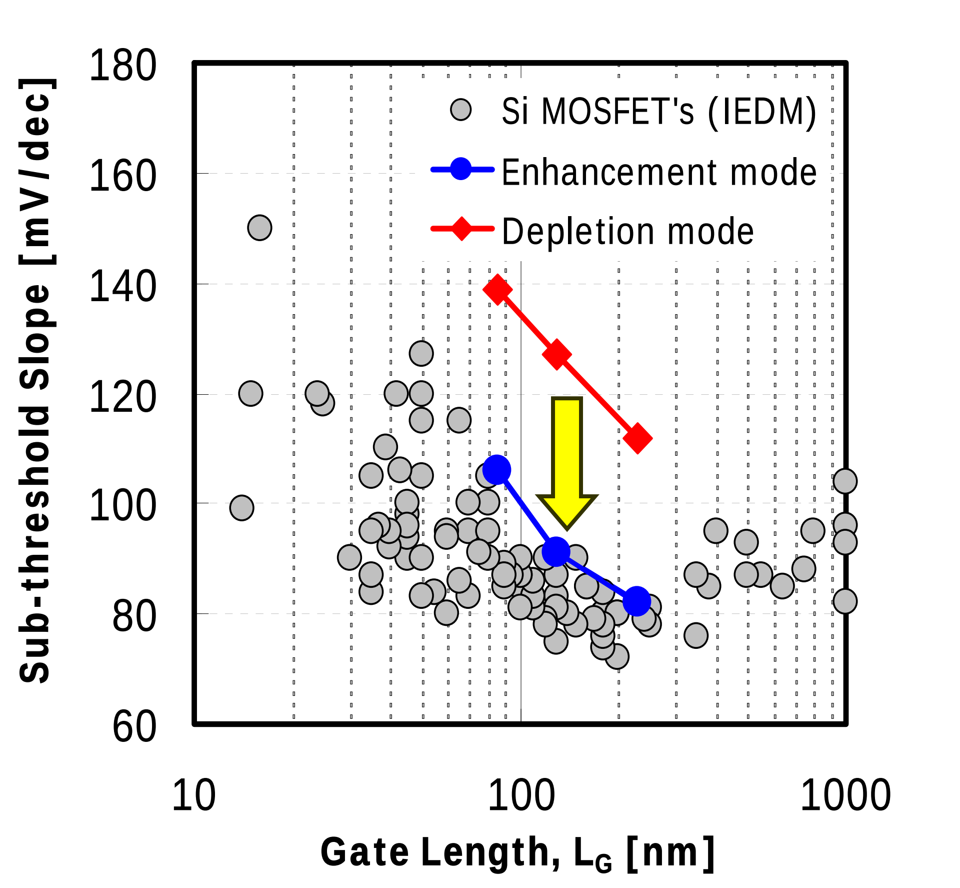


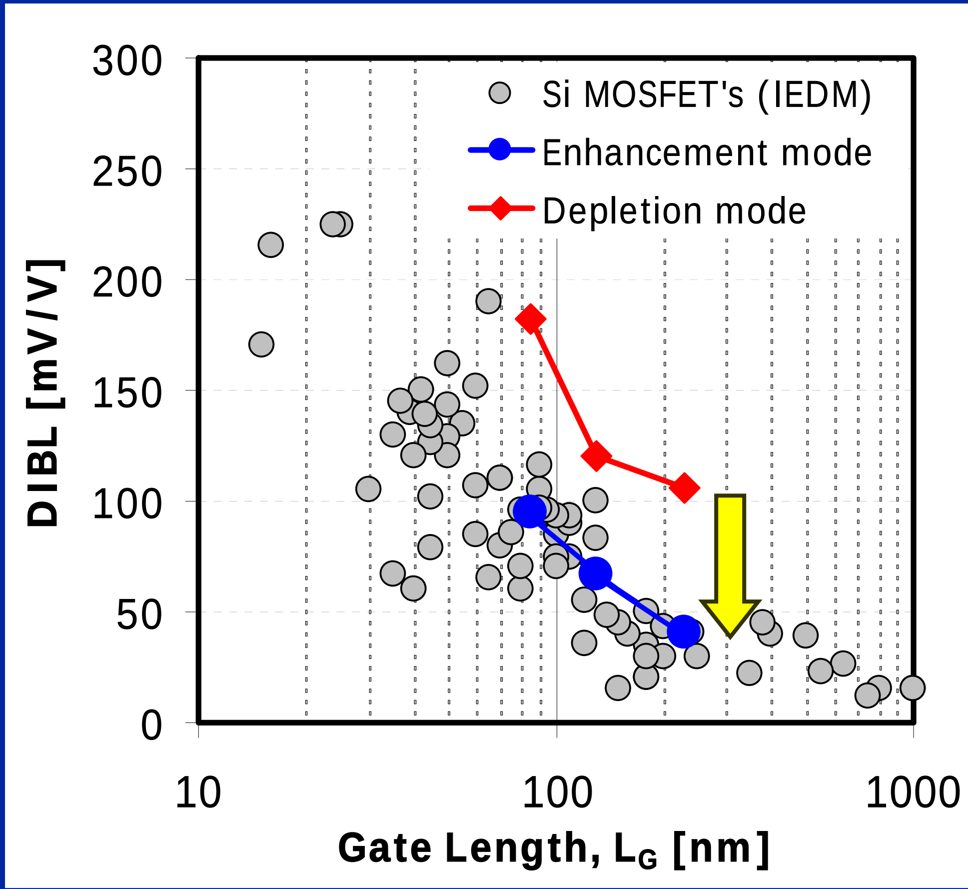


$$f_T = \frac{1}{2\pi} \frac{g_{m0}}{(C_{gs} + C_{gd})\left[1 + \frac{R_s + R_d}{R_{ds}}\right] + C_{gd} g_{m0} (R_s + R_d)}$$

Self aligned transistor architecture will further improve performance

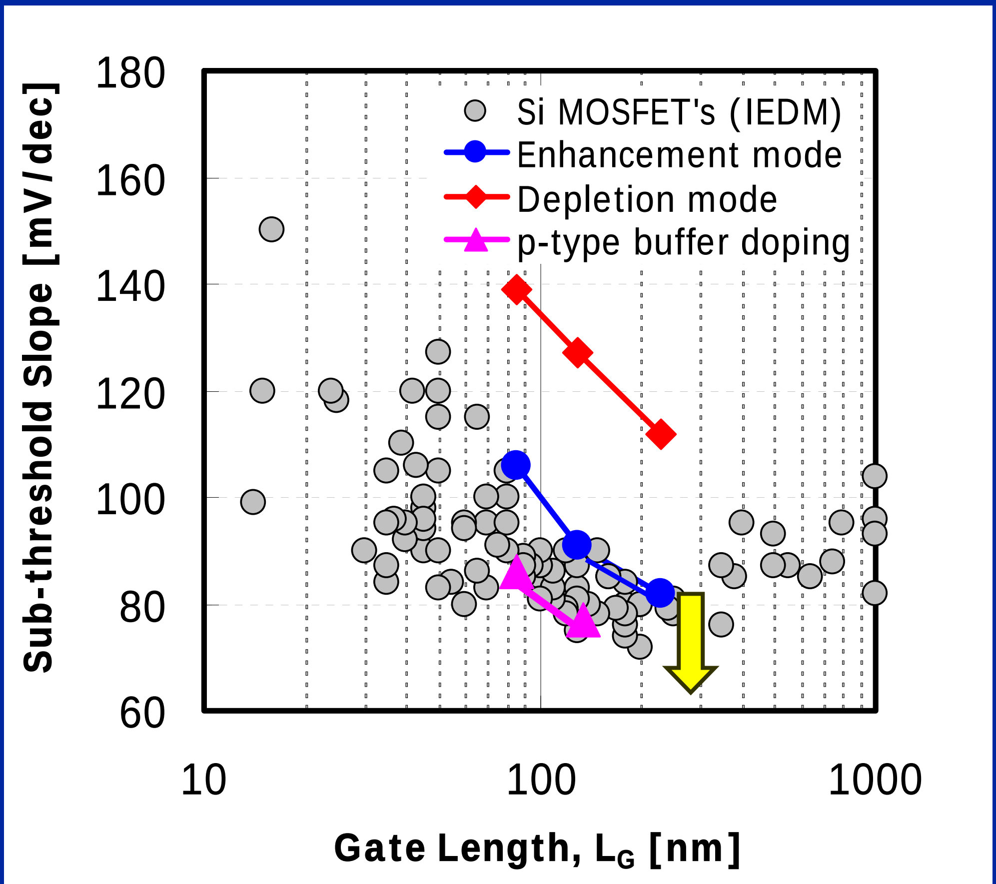
Scalability: Recessed Gate Effect

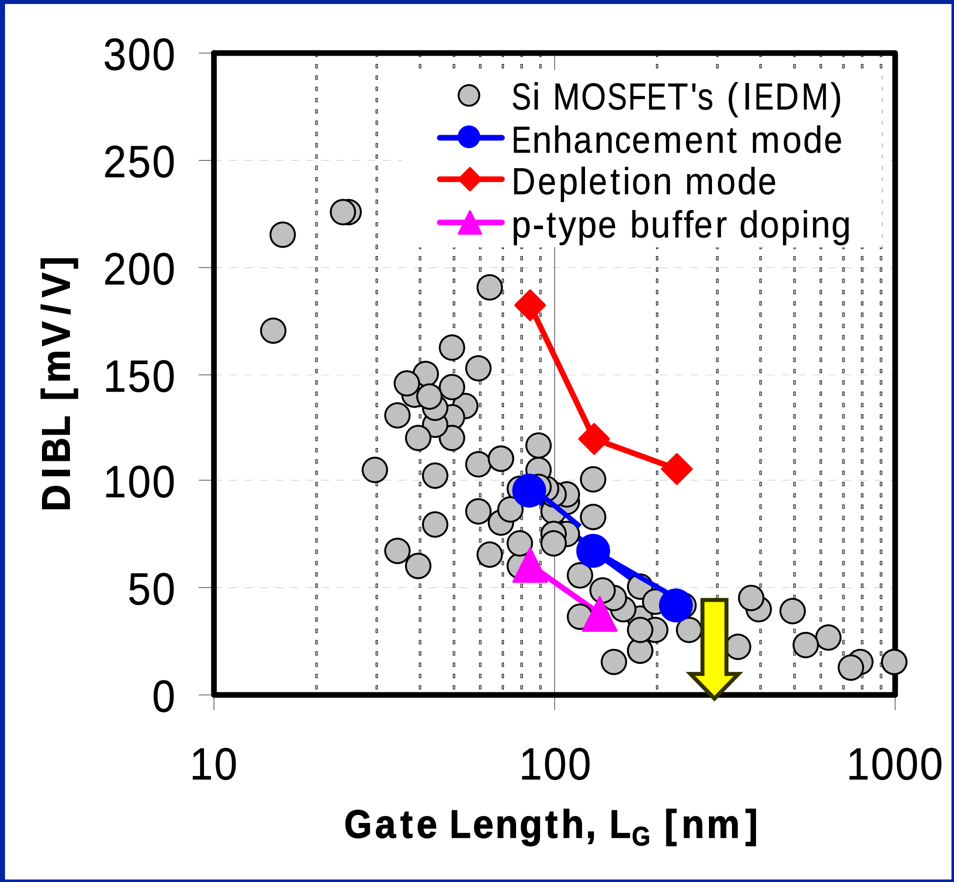




Recessed gate architecture improves the gate field to quantum well coupling, improving scalability

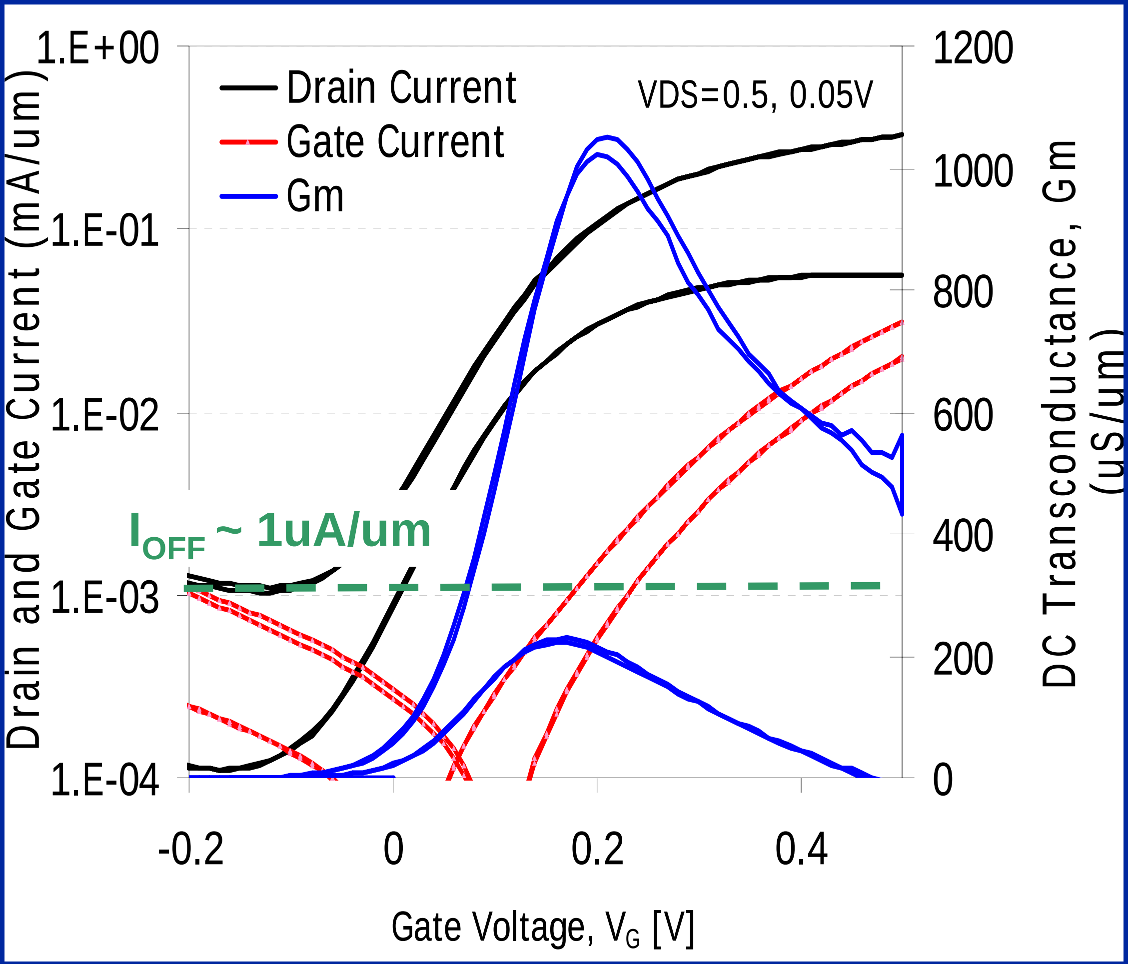
Scalability: Buffer Doping Effect

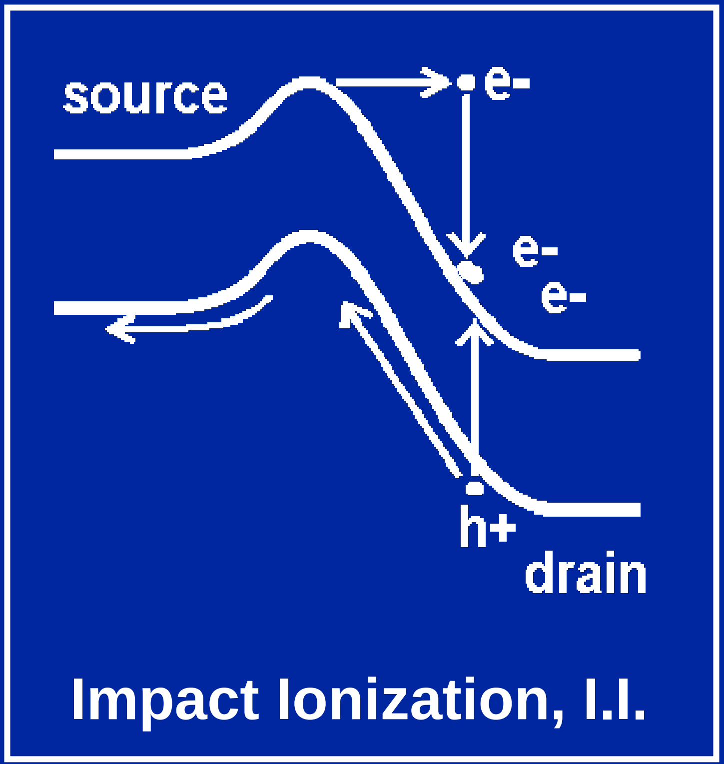




Scalability further improves by buffer dopant engineering

Off-State Leakage



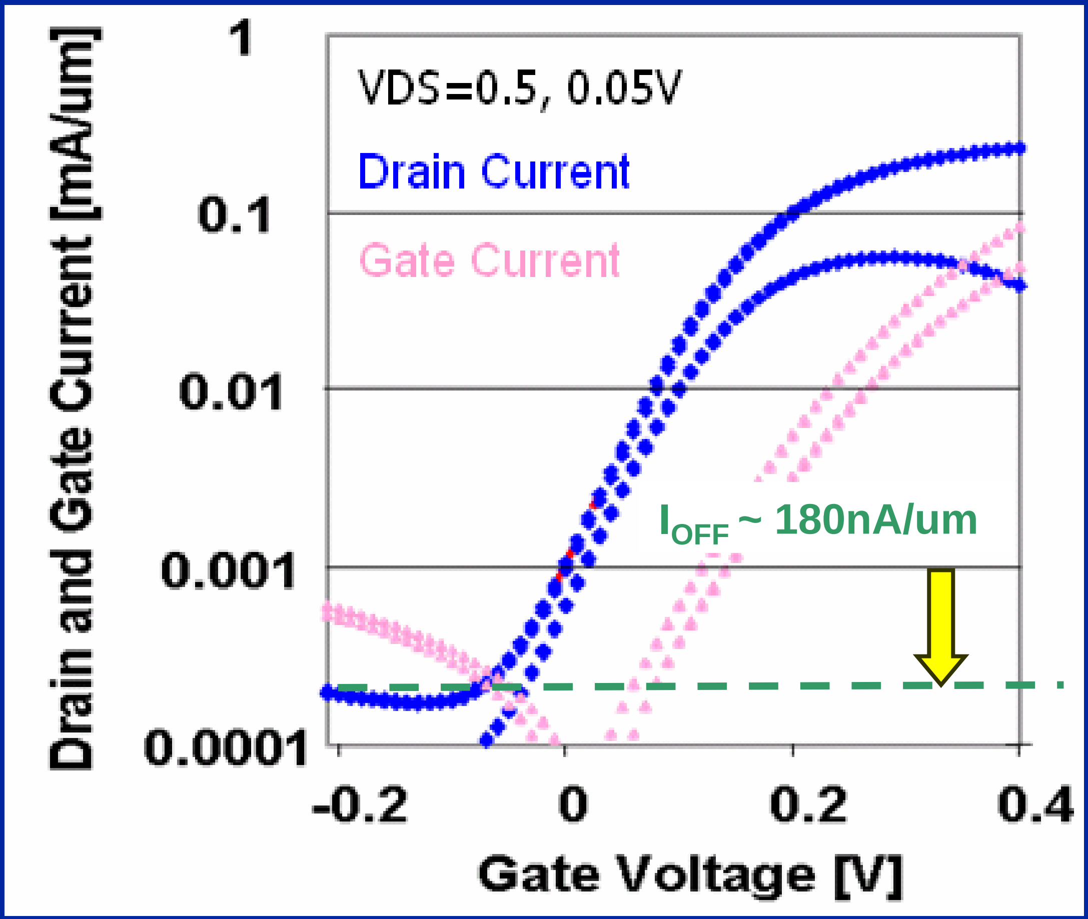


Off-state drain leakage current is from:

a) gate leakage through the M-S Schottky junction

b) impact ionization in the InSb QW

Off-State Leakage



I_{ON}-I_{OFF} ratio increases to 1000 over 0.5V V_G swing with a hole extraction contact

- Extraction of holes reduces I.I. which, in turn, reduces the drain side off-state leakage
- Gate leakage from forward biased M-S Schottky junction still an issue (need insulated gate)

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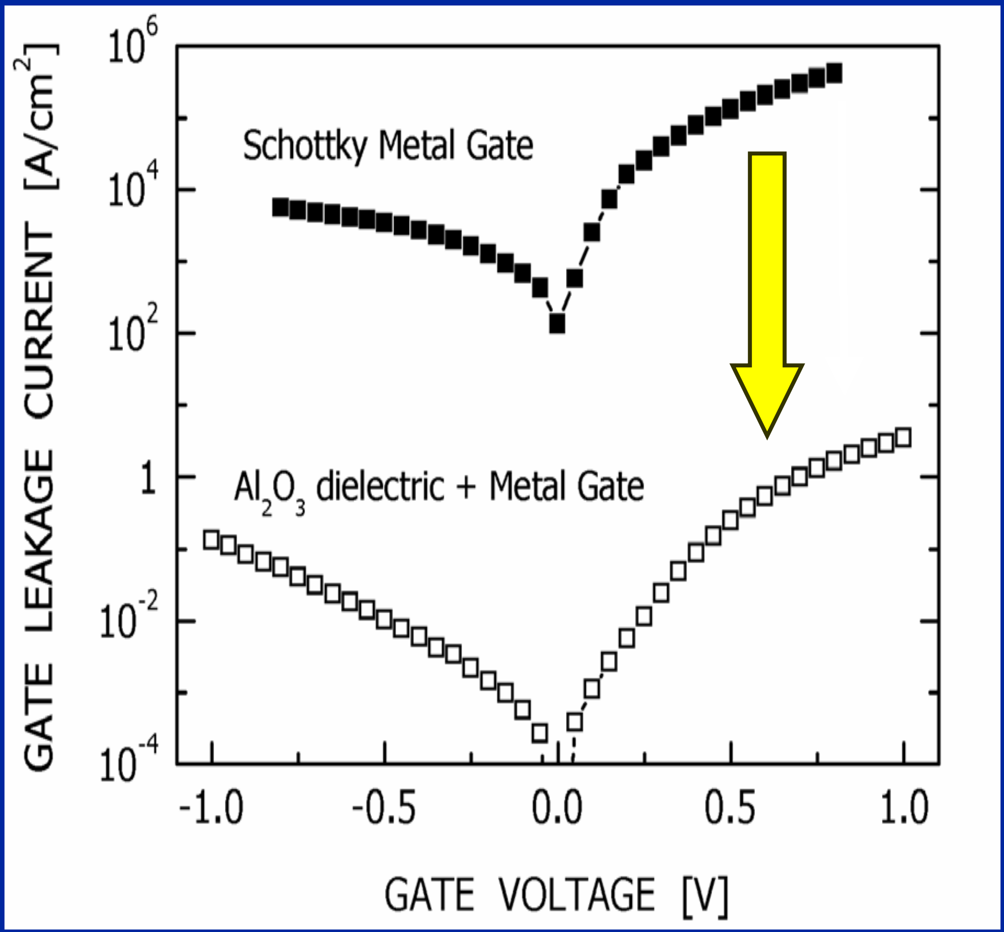
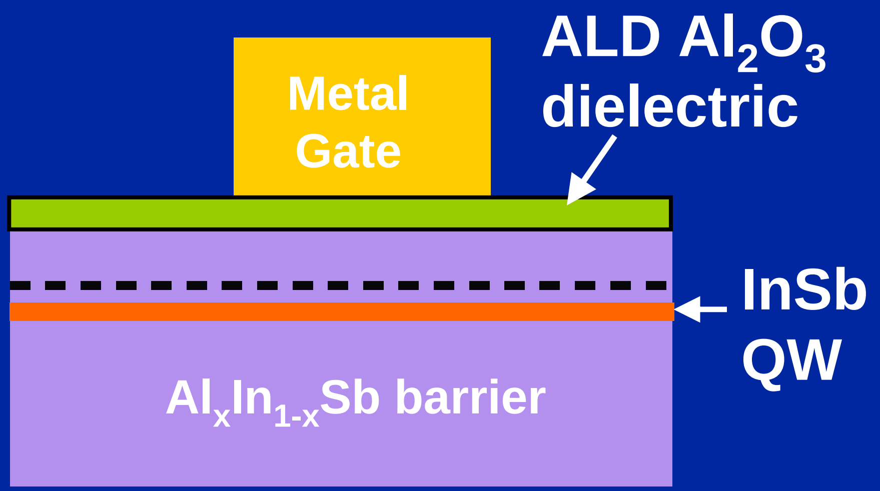
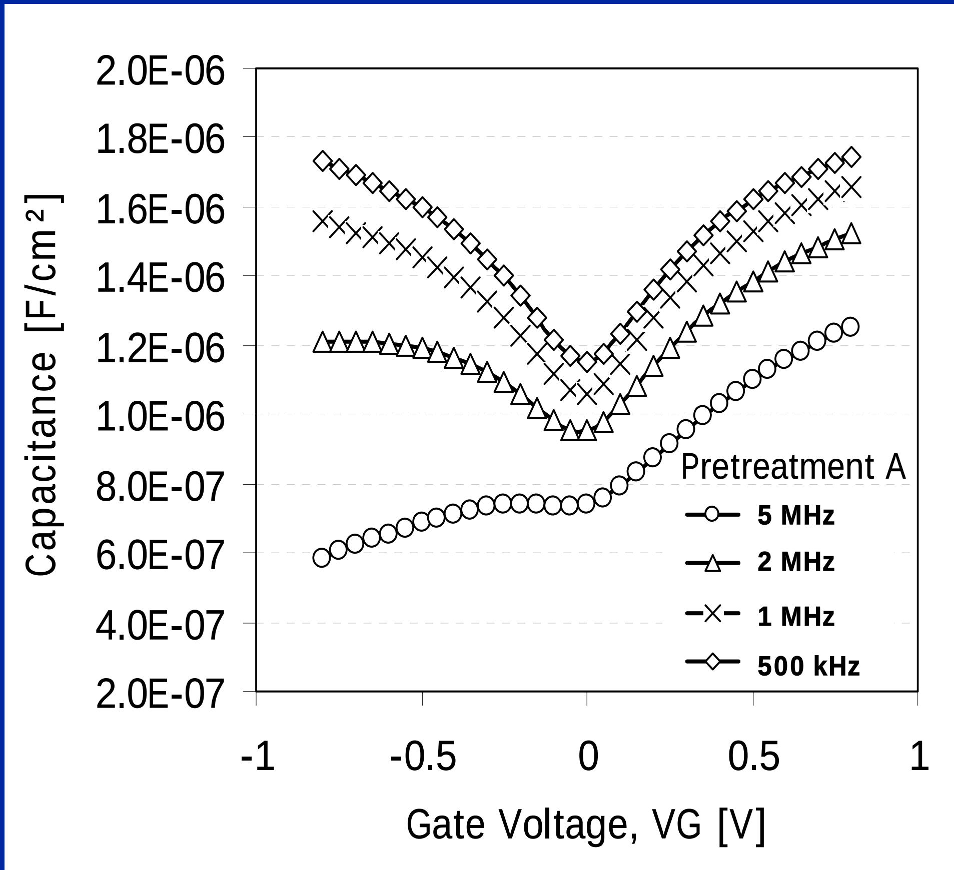
High-K Gate Dielectric



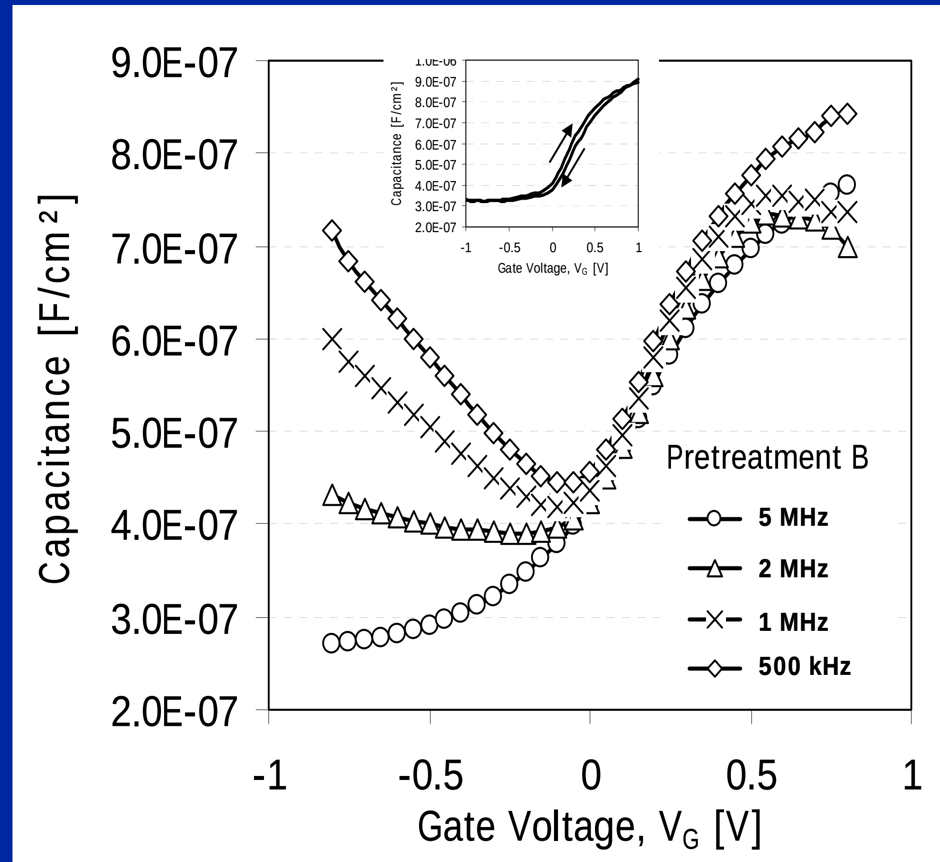


4 orders of magnitude reduction in gate leakage with ALD Al_2O_3 dielectric + metal gate on InSb(Al)

High-K Gate Dielectric



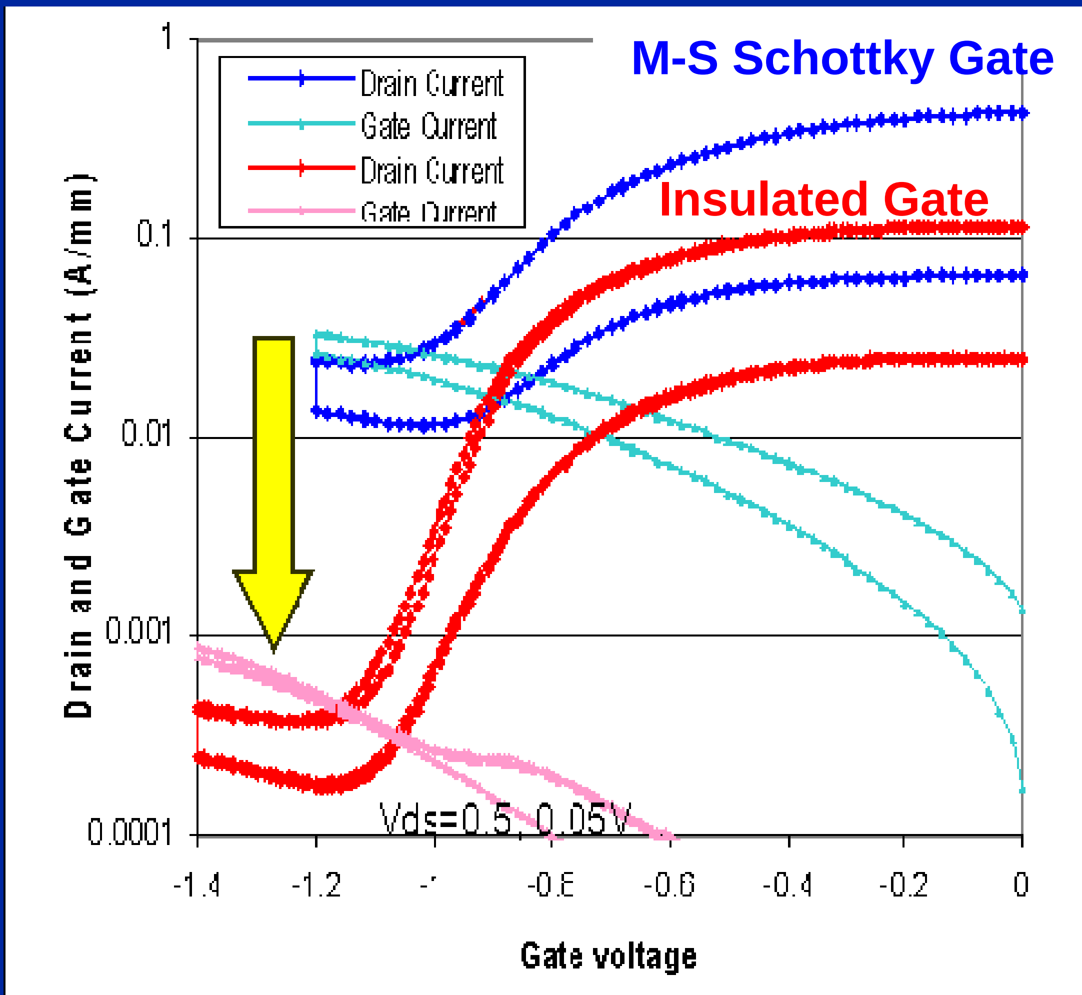
Oxidized Surface

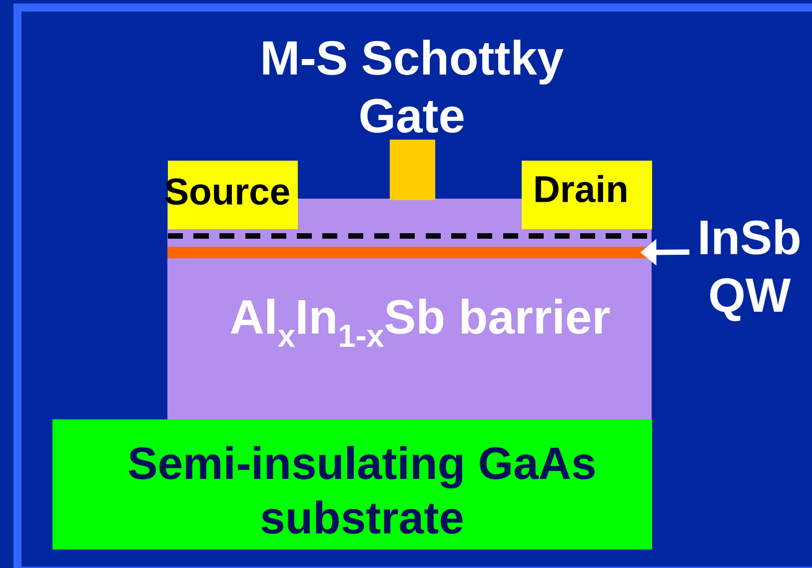


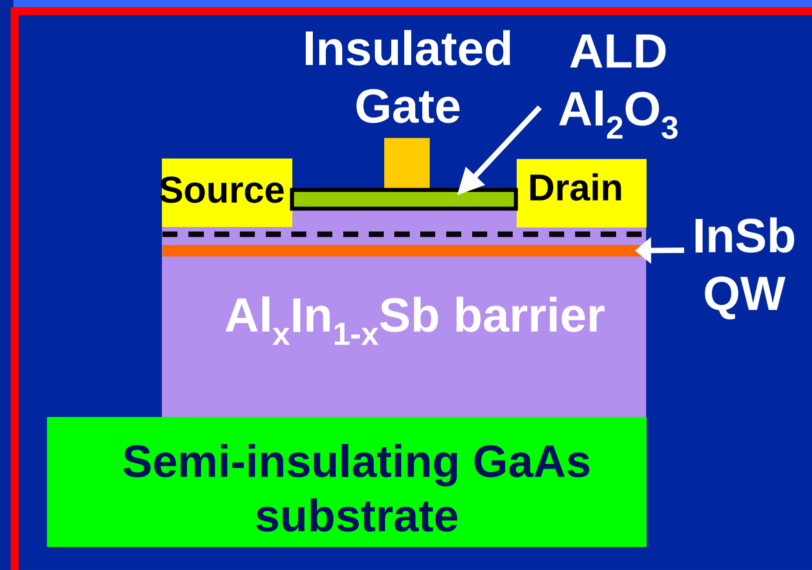
Less Oxidized Surface

The dielectric and semiconductor interface quality is strongly modulated by the surface pretreatment

High-K Gate Dielectric







Depletion mode InSb QWFETs with high-k gate dielectric show significant improvement in gate leakage and I_{ON}-I_{OFF} ratio

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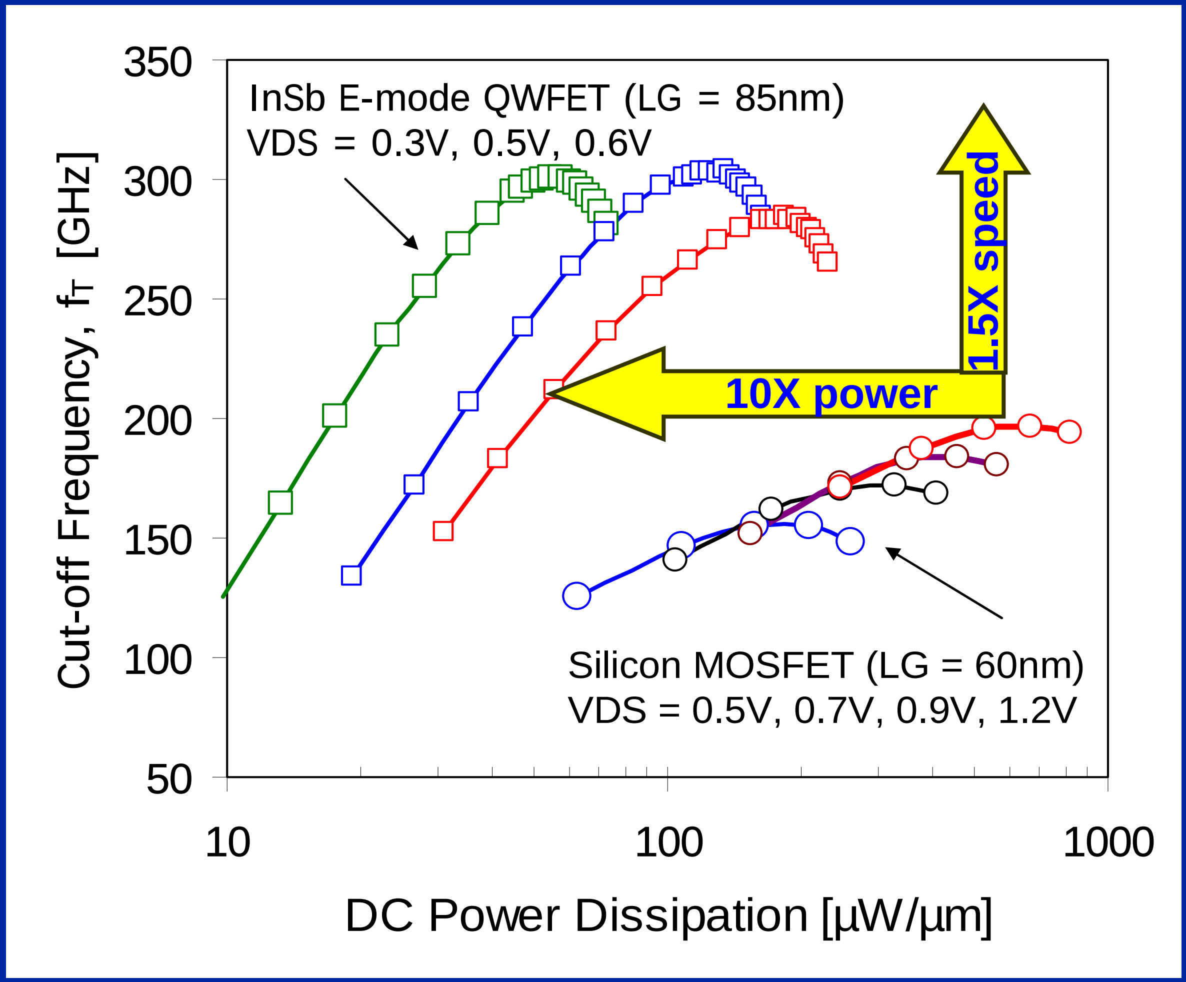
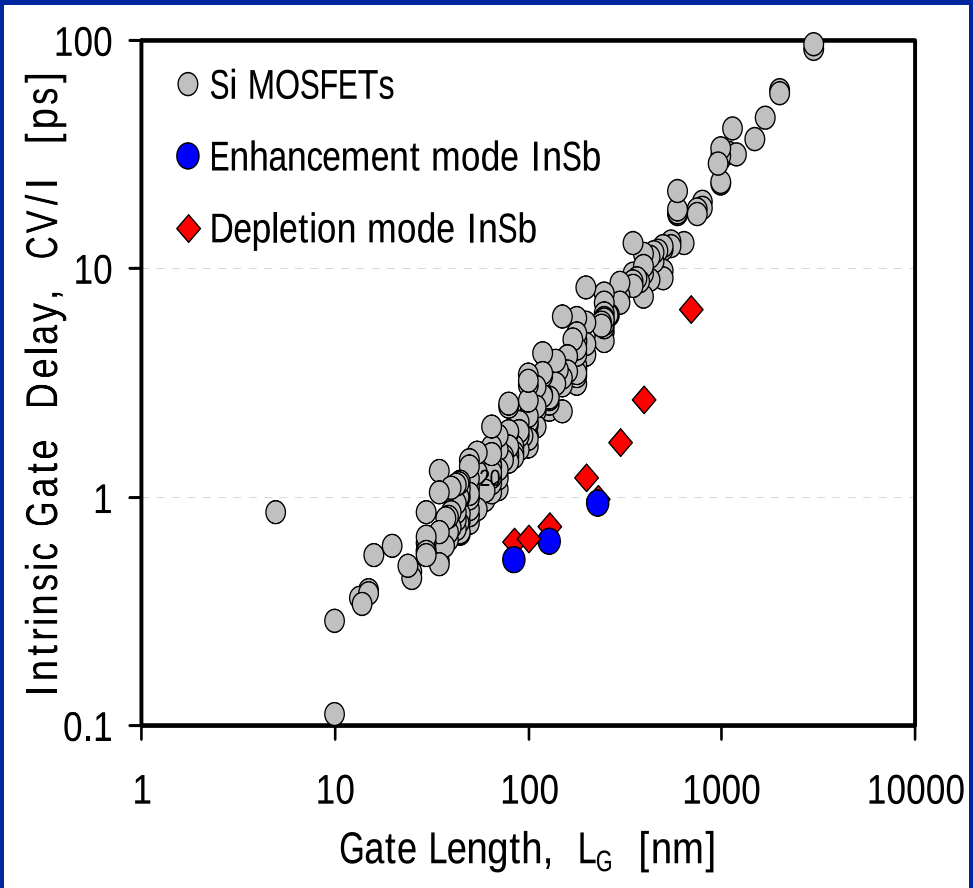
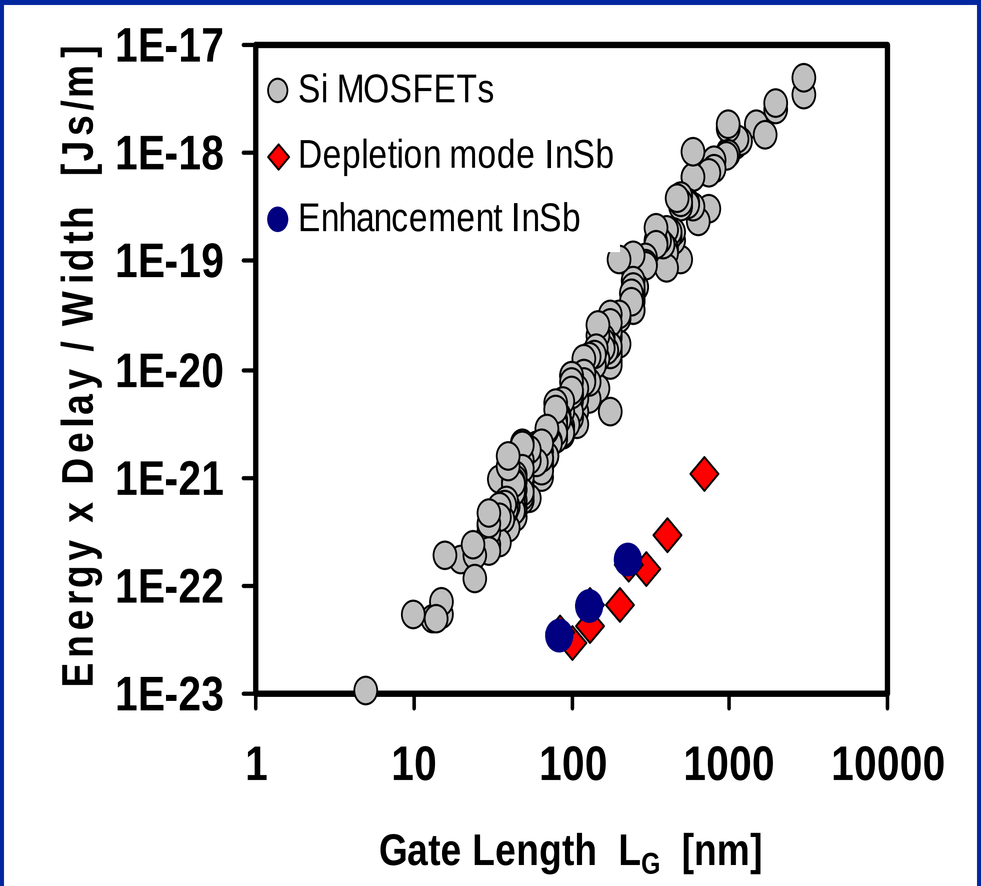
Speed Power Performance



InSb QWFETs show > 10x reduction in active power dissipation compared to Si MOSFETs

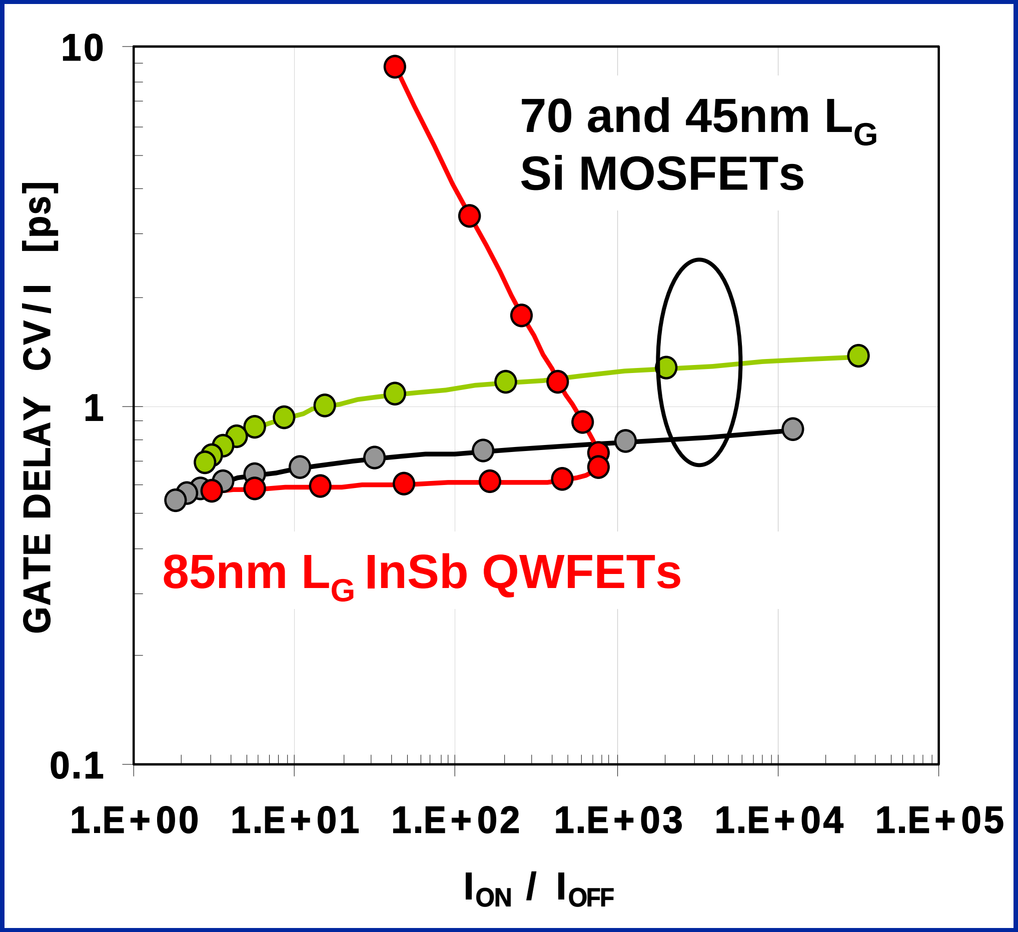
Benchmarking InSb QWFETs





InSb transistors show significant improvement in intrinisic gate delay and energy-delay product over Si MOSFETs at equivalent gate length

Benchmarking InSb QWFETs



The gate leakage through the M-S Schottky junction limits the dynamic I_{ON}-I_{OFF} range of InSb QWFETs

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Opportunities

- **85nm L_G depletion and enhancement mode InSb QWFETs have been demonstrated intrinsic switching speed of 300GHz at 0.5V V_{DS}**
- **Benchmarking shows InSb QWFETs can potentially provide**
  - 10X reduction in active power compared to Si MOSFETs from low Vcc operation
  - 50% higher intrinsic switching with speed at equivalent power

Grand Challenges

- High quality High-K dielectric demonstration
- Continued L_G scaling
- Self aligned architecture for density + performance
- Ultra-high hole mobility P-channel III-V for complementary logic
- III-V integration on Silicon substrate