

Line Defect Control to Maximize Yields

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Abstract

This paper discusses line defect control through the use of defect monitors in semiconductor manufacturing. Defect monitor development has focused on maximizing good die output through die yield improvement in a cost-efficient manner. Line defect monitors provide rapid feedback and shorten cycle times for problem resolution. For high-volume manufacturing, line defect control is employed to achieve rapid excursion response and more stable yields. Return on investment analysis optimizes the cost of defect metrology against die cost reduction achieved by higher die yields.

Introduction

A semiconductor factory must provide predictable output to meet its customer commitments. Predictable output is based on meeting the die yield, line yield, and wafer throughput time forecasts for the factory. Today's semiconductor manufacturing processes have over 150 process steps and several weeks of throughput times. Several weeks of output is at risk if the only metric to measure the quality/yields of the wafers is at final test. Line defect control is a method that uses inline defect monitors to measure defect/quality levels on product wafers at various sampling points throughout the manufacturing line [1,2]. Inline defect monitors give quantitative and qualitative information about the types of defects detected on the wafer surface. A response system based on the information collected by these defect monitors assures good line defect control.

Line Defect Control Method

Defect monitor development has focused on maximizing output through die yield improvement in a cost-efficient manner. Numerous manufacturing and die yield advantages from product wafer defect monitoring have been realized over traditional bare test wafer monitoring.

Line defect control is achieved by measuring and controlling defects on process equipment/tools and by inspecting and controlling defect levels on product wafers. Defect levels on process equipment are measured by running silicon test wa-

fers through the tool and then responding to shifts in defect levels measured on the test wafers. The traditional method of inspecting product wafers was to visually inspect wafers under a microscope. The visual inspection technique worked well for detecting relatively large and high-density visible defects. However, it was limited by the skill of the inspector and the limited die sampling area. As process technologies move to smaller geometries, the size of yield-limiting defects is scaled with the feature size. Similarly, the high capital cost of current semiconductor factories requires ever-lower defect densities for each generation of technology. The industry has responded with the use of automated defect inspection equipment for product wafers and parallel development of response systems, called product line monitors.

Defect detection is a critical component of defect reduction and control (1). The SIA Crosscut Technology Working Group [3] has formed its own sub-group to ensure that the roadmap for future defect detection capabilities is consistent with the future (higher) yield requirements forecasted by the industry. The two primary techniques for automated defect inspection are either optical based or laser detection based. In the optical inspection method, pixels in one die or cell are compared to adjacent cells, with differences counted as defects. This method is very good for catching small visible defects and even subtle pattern variations. As the sensitivity is increased, however, optical detection is limited by noise from subtle color variations and natural thin-film grain structure variation. In the laser defect detection method, defects are detected from reflected signal changes as the laser is rastered over a surface anomaly. The laser method is good at picking up defects on layers where the wafers are relatively planar; that is, when the defects are large relative to the pattern topography. Laser tools scan much larger areas per unit time than do optical tools. Both methods have their strengths, and they are used accordingly to provide the best visibility of different types of defects. Once the die are inspected, optical reviews are used to classify defect types. Defect

paretos, as shown in Figure 1, are constructed to understand the different types and levels of defects at each inspection location.

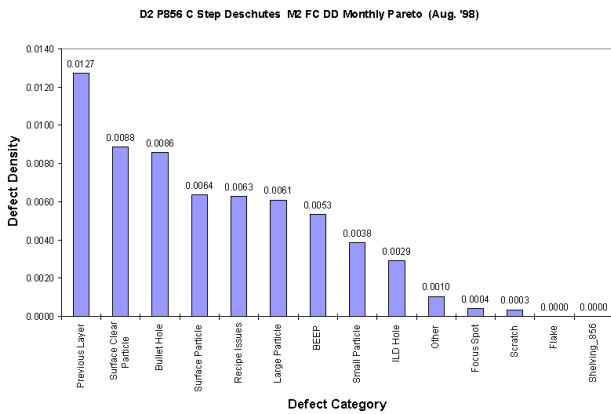


Figure 1: Defect classification pareto for a defect monitor

For line defect control, multiple product line monitors are inserted throughout the manufacturing process so there is continuous feedback on the stability of defect levels. Monitor locations are chosen based on multiple considerations including the excursion risks of preceding operations, the yield impact of the layer defect population, and the quality of the monitoring recipe.

Defect Control in Manufacturing

As with other commonly monitored parameters, statistical process control (SPC) is used to monitor defect trends and trigger responses, as shown in Figure 2. Automated factory floor response systems are initiated when defect limits violate statistically determined SPC control limits. These Out of Controls are the first line of defense against tool excursions.

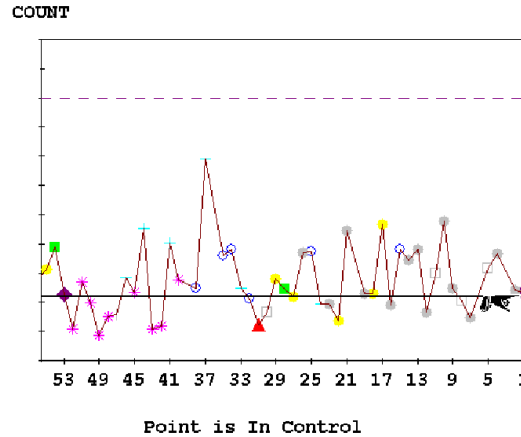


Figure 2: Defect monitor control chart

The response systems in a manufacturing line are critical to the effectiveness of the line defect monitors and to the workflow of the manufacturing line. If the manufacturing technicians (MT's) do not have a well defined response flow system, then either the response is inadequate or the workflow of the manufacturing line is interrupted while an engineer is called in to decide how to respond. The MT's must be trained to respond on a 24-hour basis.

Line defect control can be used to improve yields by adding stability to the line and by using the defect pareto data (Figure 1) to eliminate or reduce "killer" defects. Using SPC, line defect monitors can be used to detect defect excursions, and the rapid feedback minimizes material loss. Line monitors provide rapid feedback.

Cost/Cycle-Time Implications

Improved line defect control, and therefore yield control, can be achieved by increasing the number of defect monitors placed in the line. However, placement of defect monitors leads to additional cost and increases the cycle time of the process. The increase in manufacturing cost comes from the cost of capital (inspection tools) and labor in collecting and analyzing the data. The cycle time of the overall process increases due to the time taken to do the additional monitoring. For example, if a manufacturing cycle time is six weeks, and there are no line defect monitors in place, we could potentially have up to six weeks of material in jeopardy in a case where a die yield defect-related problem is detected at final test. However, if a monitor were placed in the middle of the manufacturing line, this would cut the amount of material in

jeopardy by half, assuming the line defect monitor could effectively catch the defect. Thus, the feedback loop for the line defect and yield control can be improved by strategically placing monitors throughout the line. Moreover, in an environment where we are willing to tolerate an output risk of up to one week of material, we should have five line defect monitors in the above six-week manufacturing cycle time example. Assuming a 0.5 day cycle time per monitor, placing five monitors would increase the manufacturing cycle time by 2.5 days and increase labor and capital cost. Figure 3 shows a conceptual cost relationship of product defect monitor frequency to die cost. The parabolic shape in Figure 3 is caused by high-defect metrology costs at short monitor distances on one end, and by low die yield, by potentially missing yield excursions due to large distances between monitors, on the other end. The lowest point in the curve is the optimum balance between die yield and monitor distance/frequency.

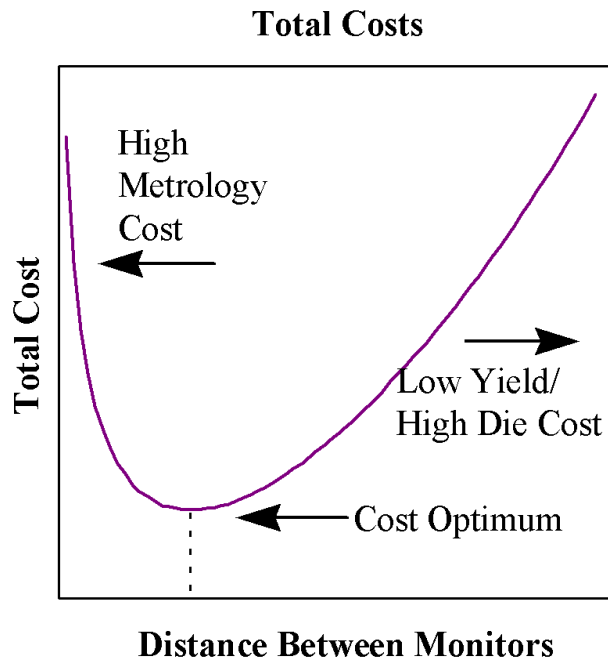


Figure 3: Cost relationship of the number and frequency of defect monitors in a manufacturing line

Future Trends

In the future, we hope to seamlessly integrate line defect inspection, data analysis, and response systems into the semiconductor manufacturing line. There are three significant trends for line defect control: more sophisticated automation to collect the defect description data, improved response to

line defect control data, and more emphasis on cost reduction. Automatic defect classification will enable us to significantly reduce the labor involved in collecting and summarizing the current defect data. Improved automation systems and algorithms are being put in place to allow a faster automatic response to “defects of interest.” For example, we envision a time when a defect source is known and there is an increase in defect levels from that source, there will be an automatic response signal sent to the suspect station or stations. The trend in cost reduction will force us to reduce the overall level of monitoring in a semiconductor process and make it more efficient.

Line defect control is now an essential part of the semiconductor manufacturing process to maximize die output. As we look forward, we should be able to improve the level of line control and reduce costs by increasing the sophistication of the tools, improving our response systems, and reducing the total number of monitoring points.

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Authors' Biographies

Sanjiv Mittal has been at Intel since 1984. He is currently the Fab Manager at Intel's D2 Development and Manufacturing Fab in Santa Clara. Prior to this position, he managed yield improvement and then the manufacturing departments. He has a Sc.D. from MIT and a M.S. from Purdue University both in materials science and engineering and a B.S. from the Indian Institute of Technology. His e-mail is sanjiv.mittal@intel.com.

Peter McNally has been with Intel's D2 development and manufacturing facility since 1993. He has served various yield improvement roles driving defect reduction, metrology systems, correlation tools, and yield analysis for Intel's .5 and .25 micron processor generations. His 15 previous years were spent at Hewlett Packard and National Semiconductor including an assignment with Sematech. His degrees include a M.S. from Stanford University and a B.S. from Cornell both in materials science and engineering. His e-mail is peter.mcnally@intel.com.