

Preface

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Editor

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Microprocessor packages are the external "suits" for the complex and intricate world of silicon chips. The working part of a microprocessor is a small piece of silicon no larger than a postage stamp encased in a sealed "package." The chip itself must be sealed away to prevent external contaminants, such as dust, from adversely affecting the silicon chip. The art and science of semiconductor packaging has advanced radically over the last decade as faster and more powerful microprocessors with millions of transistors stressed the state of the art in microprocessor packaging. Thermal-heat dissipation, signal interconnects, and higher densities have required many advances. Pin-grid arrays with hundreds of pins, multicavity modules, leadless chip carrier and quad flat packs are the many types of microprocessor packages today.

The seven papers here present an engaging discussion on Intel's microprocessor packaging technologies. They highlight the technical challenges faced by packaging developers now and in the future, and in a broad sense, ties them into the many challenges faced by the semiconductor industry to achieve the next level of performance. The first paper traces the evolution of Intel's microprocessor packaging technologies. Flip-Chip Pin Grid Array (FCPGA) used in Intel's high-performance microprocessors uses balls of solder and gold that are melted (or reflowed) to connect the silicon chip to the package. The second and fifth papers look at this packaging technology.

The third paper explains the technical complexity of interconnect design to achieve optimal electrical performance. This paper discusses the design analysis and synthesis techniques used to ensure optimal electrical design. The fourth paper presents the challenges faced in thermal design. Ensuring that packaging continues to meet high standards of reliability is a key to success and is discussed in the sixth paper. Finally, the seventh paper discusses the practical problem of managing the thermal environment during microprocessor testing.