

Preface

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Editor

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This Q2, 1999 issue of the Intel Technology Journal focuses on the Pentium® III processor. In late 1995, two factors influenced Intel's processor roadmap. The first one was the emerging importance of 3D capabilities for the volume PC market. These 3D capabilities were important for games and workstation software. Floating point computation is the heart of 3D geometry capabilities. With the introduction of the Pentium® Pro (P6) architecture, the floating point performance was good enough to make 3D really viable for PC's. The second influencing factor was the realization that there was an opportunity to strengthen Intel's processor roadmap for the late'98/early'99 timeframe with a P6 based proliferation. The question was how to do this while at the same time addressing the emerging importance of 3D.

In February 1996, the product definition team at Intel presented Intel's executive staff with a proposal for a single-instruction-multiple-data (SIMD) floating point model as an extension to IA-32 architecture. In other words, the "Katmai" processor, later to be externally named the Pentium III processor, was being proposed. The meeting was inconclusive. At that time, the Pentium® processor with MMX instructions had not been introduced and hence was unproven in the market. Here the executive staff were being asked essentially to "double down" their bets on MMX instructions and then on SIMD floating point extensions. Intel's executive staff gave the product team additional questions to answer and two weeks later, still in February 1996, they gave the OK for the "Katmai" processor project. During the later definition phase, the technology focus was refined beyond 3D to include other application areas such as audio, video, speech recognition and even server application performance. In February 1999, the Pentium III processor was introduced.

In this Q2, 1999 issue of the Intel Technology Journal, you will gain important insights into the features and capabilities of the Pentium III processor. The first and second papers describe the Streaming SIMD Extensions and the microarchitecture implementation challenges. The third paper discusses the processor serial number feature. The fourth and fifth papers cover tuning applications for Streaming SIMD Extensions and an optimized 3D architecture stack for performance. And, finally, in the fifth paper, programming methods for the Streaming SIMD Extensions are described.