Volume 12 Issue 3 Published October 2008 ISSN 1535-864X DOI: 10.1535/itj.1203.04

Intel® Technology Journal

The Original 45nm Intel Core™ Microarchitecture

Mobility Thin and Small Form-Factor Packaging for Intel® Processors Based on Original 45nm Intel Core™ Microarchitecture

Mobility Thin and Small Form-Factor Packaging for Intel® Processors Based on Original 45nm Intel Core™ Microarchitecture

Kyan Pedrami, Mobility Processor Design Team, Intel Corporation
Satish Prathaban, Mobility Platform Hardware Development Team, Intel Corporation

Index words: penryn, small form factor

Citations for this paper: Kyan Pedrami, Satish Prathaban "Original 45mn Intel® Core™2 Processor Performance" Intel Technoloy Journal. http://www.intel.com/technology/itj/2008/v12i3/4-paper/1-abstract.htm (October 2008)

ABSTRACT

The Intel 45nm processor, originally referred to by the codename Penryn, based on Intel Core™ microarchitecture, is the first processor that uses multicore-on-die design to maximize performance and minimize power consumption. This paper provides an overview of how the Penryn processor's mobility platform and package design teams delivered the Penryn silicon in smaller and thinner packages that enabled customers to design both smaller and thinner form-factor platforms. It also provides insight into the mechanical and electrical challenges of these families of thin, small, form-factor packages, challenges that were overcome without incurring significant performance degradation.

INTRODUCTION

The Intel® processor, originally referred to by the codename Penryn, is the first 45nm processor that is based on Intel Core™ microarchitecture that uses multicore-on-die design to maximize performance and minimize power consumption. It is also the first "all-green" Intel 45nm processor product that is lead and halide free. Historically, Intel mobility processors were packaged in a 35-mm × 35-mm substrate, in eight layers of package routing, with a z-height of 2.89 mm, on a socket, and with a pin pitch of 1.27 mm. This footprint and z-height were design targets for the Penryn mobility processor family. During the life cycle of the Penryn family of processors, two major packaging design requirements were introduced. First, a cost reduction target was identified for the Penryn family of processors. The team responded with innovative designs implementing both six- and four-layer packages, compared to the traditional eight-layer package. Second, a customer requirement was introduced for a smaller and thinner package option. The team was able to leverage the lower-layer-count proposal in order to achieve the new requirement profile. This new package design required a processor package z-height of less than 2 mm, with a footprint of 22mm × 22 mm, a pin pitch of 0.952 mm, and a pinmap, supporting the High Density Interconnect (HDI) board. The reduction of the package footprint size meant packing all the signals within the smaller package with negligible additional crosstalk. The challenges of such a design resides in processor power delivery, due to the lower number and placement of package capacitors in the available space constraints. In both cases, the design team was faced with the challenge of fitting a robust core power-delivery system, with negligible performance impact, into a package smaller than the traditional mobility packages.

The Penryn mobility processor with a 3-MB cache form-factor was the first processor in this family to be packaged into the lowest possible package stackup; and with a 6-MB cache, was the first mainstream Small Form Factor (SFF) mobility product to tape out a package in just nine weeks with pinmap redefinition and bottom-up package design. In this paper, we provide an overview of how the Penryn family of processors' mobility platform and package design teams delivered the Penryn silicon in smaller and thinner packages that enabled customers to design both smaller and thinner form-factor platforms. We provide insight into the mechanical and electrical challenges of these families of thin and SFF packages without incurring significant performance degradation. We also explain how design team members, located across multiple geographical

areas, synchronized their work for maximum productivity to achieve multiple package design breakthroughs in mobility package design.

OVERVIEW OF THE 3-MB PIN GRID ARRAY AND SMALL FORM FACTOR PACKAGES

In the context of mobility package design, the Pin Grid Array (PGA) package was traditionally designed first, and later on, the PGA design was converted directly to a Ball Grid Array (BGA) package by replacing the pins on the design with balls. Doing so enabled the back-end team to concentrate on one processor package form-factor validation and helped the package design team to focus on one design. As an additional benefit, investment in parts and validation tools to test two simultaneous designs was not necessary. The downside for the "one package design fits all" scenario was that the final implemented package contained all design requirements of both PGA and BGA packages combined, which results in very small cost optimization. Initially, this same package design strategy was planned for the Penryn mobility family of processors. This 35-mm × 35-mm socket has not been changed for three generations due to a backward compatibility requirement; however, in the case of the mobility processor, the pinmap was slightly modified to meet manufacturing and reliability requirements. This backward-compatibility feature meant the same 35-mm × 35-mm PGA package, socket, and pinmap could be used throughout multiple processor designs. This reuse helped in the verification of the new package on the old platform thus enabling customers to reuse their mechanical and thermal solutions from the previous platforms, an obvious reduction in design time and cost. Traditionally, the mobility processor packages were also designed with an eight-layer stackup with the top layer dedicated for Front Side Bus (FSB) routing. The original Penryn mobility processor package design stackup was eight layers. The four-package internal layers were used exclusively for processor and I O power delivery. The focus of the package design team when designing the Penryn family of processors' mobility package was to also optimize the package layer count, and if possible, optimize the package footprint.

With the introduction of the Penryn family of processors' cost-saving challenge, the team analyzed opportunities to reduce package cost. In 45nm design technology, it is feasible to reduce the overall number of package layers to six or even four, netting a significant cost reduction throughout the life of the product. For the 3-MB 35-mm × 35-mm package, the team pursued a four-layer PGA package design. The design practice of serial development of PGA and BGA designs was no longer followed, and packages were instead developed in parallel, making the two designs no longer dependent on one other. Although this approach now required validation of each form factor, this new approach facilitated the removal of BGA design elements from the PGA design. Coupled with the reduction in the number of layers, these innovations drove significant cost savings in the Penryn 3-MB processor's PGA package manufacturing cost. The design team was able to further leverage these advantages in response to a customer request for an SFF product. With the removal of PGA elements from the BGA package, the team was able to implement the design in a 22-mm × 22-mm footprint with a six-layer stackup. The socketless nature of the BGA package, coupled with fewer layers, enabled the overall z-height profile of the product to be reduced.

PACKAGE DESIGN—SMALL FORM FACTOR

In conjunction with a reduced number of layers in packages, many customers requested a reduced processor package size that could enable the design of a smaller platform form factor. We analyzed the external requirements and internal capabilities and concluded that package design size should be 22 mm × 22 mm for the Penryn BGA SFF package. Moreover, customers were also ready to use the HDI board, if the package size could be reduced. Taking advantage of the 22-mm × 22-mm package footprint, we chose a diagonal staggered pin pitch of 0.673 mm.

There were many roadblocks to clear during this phase of the design: solder joint reliability concerns and IO routing to support customers' Layer-1 and Layer-3 routing on platform.

Due to the solder joint reliability balls in the Penryn 22-mm × 22-mm package, the BGA package allowed only one column of signals for IO power delivery on the data side.

Another constraint was that the pin pitch of the package completely blocked the direct path for west-to-east power delivery. A novel method was introduced to feed the IO power from south to north by extending the pinmap down south, thereby allowing the power to enter from the south.

The pinmap was also adjusted so that it could support the HDI board. HDI is a type-4 board, with buried vias that help to reduce the package size. This is because the Plated Through Hole (PTH) does not extend up to the solder side, as via pad-to-pad spacing limits the pin pitch. In the HDI board design, motherboard Layers 1 and 3 are used

for signal routing. Most of the earlier platforms used eight layers, with Layers 3 and 6 being the routing layers, and Layers 7, 5, 2, and 4 being ground planes. In the Penryn family of processors' SFF HDI platform, one channel (odd bytes) of FSB was routed on the top layer (Layer 1) with Layer 2 as a reference (microstrip routing). The other channel (even bytes) was routed on Layer 3, with Layers 2 and 4 being ground reference planes. This method of routing enabled lower-layer board design but with the added cost of manafacturing HDI boards. This meant separate signal integrity (SI) analysis to validate both the microstrip and the stripline routing.

PLATFORM AND SUBSTRATE POWER-DELIVERY CHALLENGES AND IMPLEMENTATIONS

The standard voltage (SV) package of the Penryn family of processors is designed to enable the maximum core frequency. Frequency of operation is a function of the minimum voltage provided to the circuits in the processor; so the tighter the tolerance of the voltage at the processor, the higher the frequency that can be obtained at a given voltage.

In the PGA package, land-side capacitors act as the high-frequency decoupling solution for the package; however, due to BGA package construction, there is no cavity in which to place land-side capacitors. In both 35-mm^2 PGA 3-MB with four-layer stackup and 22-mm^2 BGA 6-MB or 3-MB with six-layer stackup packages, the surface layer has the FSB routed as the microstrip. Due to the space constraints and reduced package size, FSB lengths in the BGA package were not matched to PGA. The processor power delivery in both packages is from north to south. Unlike the PGA, in which the IO power delivery is from east to west, in the BGA, pin pitch does not allow the power feed from east or west, so the IO power delivery is from south to north.

Since the Penryn family of processors' 3-MB PGA processor had to follow the pinmap of the 35 mm × 35 mm package and the socket compatibility, the package design team concentrated only on reducing the layer count in the 3-MB Penryn family of processors.

After simulation and lab analysis on previous eight-layer stackup packages, the team determined that eight-layer packages were too robust for the Penryn family of processors' power-delivery requirements. First, two varieties of six-layer packages were evaluated. Due to BGA z-height requirements, the design required a thinner organic stiffener for package core material in the BGA compared to the PGA. In mobility packages, since the FSB was predominantly routed as microstrip on the outer top layer, only the power-delivery solution and signal-referencing layers needed to be resolved for packages with a reduced number of layers.

We realized from preproduction power-delivery analysis that removing two core layers from the original eight-layer package had minimal effect on processor performance; however, doing so substantially reduced package manufacturing costs.

Based on all preproduction findings, we decided to take a calculated risk and design the final Penryn family of processors' mobility SFF BGA package with optimized package layers, changing from the eight-layer original design to a six-layer package. This resulted in a huge savings in manufacturing costs, and moreover, as a result of fewer package layers, the total z-height was reduced, as per our customer's dictated request.

Preproduction, and post-package production data correlations, in conjunction with lab analysis of both Signal Integrity and power delivery of the Penryn family of processors' 6-MB PGA six-layer, showed that a four-layer package will be robust enough for the Penryn family of processors' 3-MB PGA mobility processor product.

In the PGA package, the decoupling capacitors are placed in the cavity directly below the die that provides the shortest path for processor discharge (Figure 1).

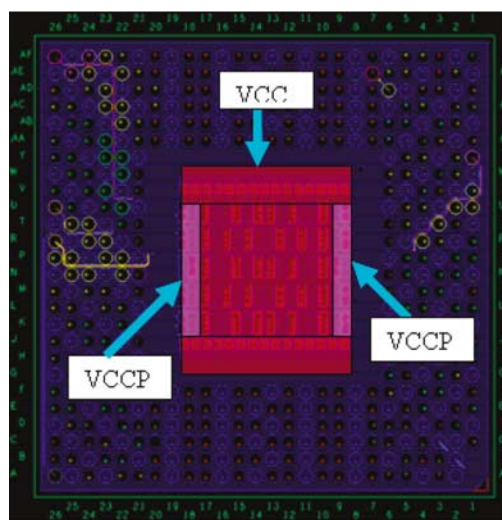

Figure 1: ***PGA land-side capacitor cavity.***

The load-line impedance is the target impedance for the power-delivery network from the voltage regulator to the processor voltage sensing points, and its impedance characteristic in the frequency domain can be extracted from the processor voltage sense points.

This characteristic can be divided into three major contributors: at low frequency (otherwise known as "third droop"), the voltage regulator and motherboard are the dominant contributors; at mid-frequency (otherwise known as "second droop"), the socket and package are the main contributors; and at high frequency (otherwise known as "first droop"), the processor itself is the main contributor.

We simulated the impedance profile for each of the package options and compared them with their previous-generation predecessor. At first droop the impedance was higher. We conducted many experiments on the previous packages by removing capacitors on the package and increasing the first droop impedance. The experiments showed that the impedance can be increased by a factor of 2 without impacting the frequency of operations.

The PGA decoupling solution uses 30 × 0306 and 30 × 0402 package land-side capacitors for the core power delivery. The board decoupling solution for core power delivery is 6 × 330 uF [ESR per capacitor = 9 mohms]. The mid-frequency capacitor on the board is either 12 × 0805 × 22 uF in the cavity region or 16 × 0805 × 22 uF on the bottom-side of the board. The IO FSB is on the east and the west of the processor with the data bus on the east and the address bus on the west of the die. The PGA package cavity could accommodate 5 × 0306 on either side for IO power delivery. Similarly, the decoupling solution for IO power delivery is a 6 × 0402 capacitor on the bottom-side of the board. Figures 2 and 3 show the location of the power-delivery capacitors on the PGA motherboard.

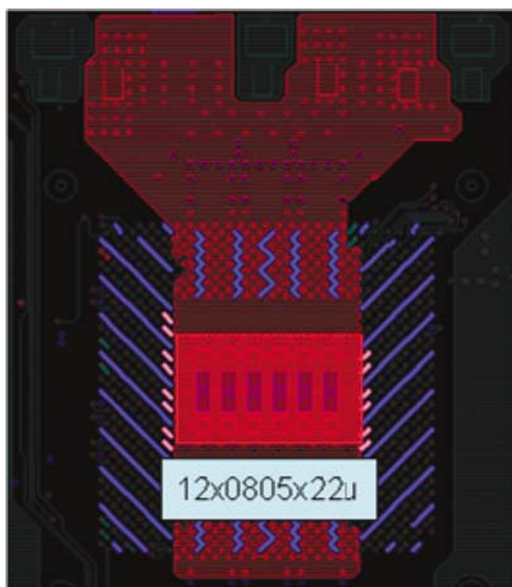

Figure 2: ***Motherboard top layer power delivery for PGA.***

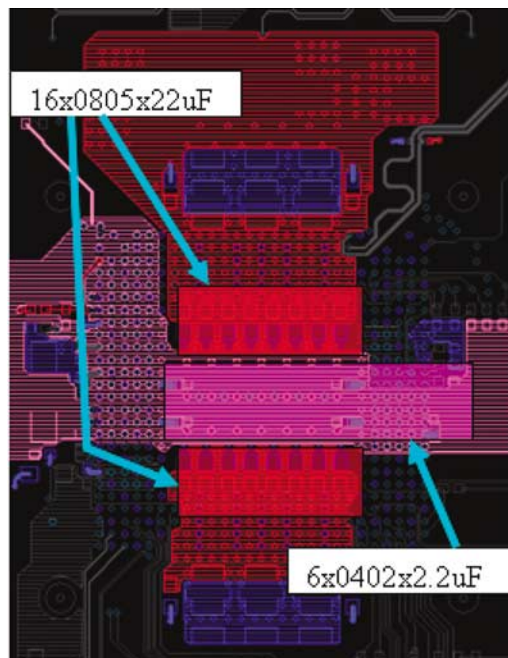

Figure 3: ***Motherboard bottom layer power delivery for PGA.***

The PGA package via pattern in the core area is chosen so that the loop inductance is low so as to reduce the first droop. The voltage regulator and motherboard load-line are kept at 2.1 mohms, the same as predecessor designs, for package backward and forward compatibility, so that customers can reuse their past designs.

The package power delivery for the SFF BGA package that lacks land-side capacitors consists of making the processor side capacitors accommodate both core and IO power delivery. The SFF BGA package contains 4 × 0402 capacitors on the north and 5 × 0402 capacitors on the south, providing the processor power-delivery solution for the package. The 4 × 0201 on the east and 4 × 0201 on the west provide the IO power-delivery solution for the package.

We designed the core power-delivery solution to meet a 4-mohm load-line with platform capacitors of 24 × 0603 × 10 uF and 24 × 0402 × 1 uF. The motherboard stackup is an eight-layer HDI stackup. We chose via patterns so as to reduce the loop inductance from the back-side capacitors of the board to the package. Our inability to put the land-side capacitors in the BGA with the pin pitch increases the loop inductance. The board IO power delivery required 6 × 0402 × 1 uF on the east and the west (see Figure 4).

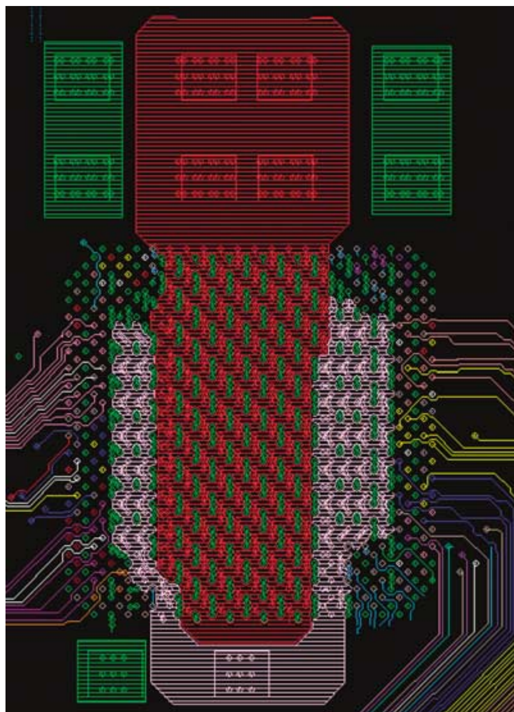

Figure 4: ***Platform power-delivery solution for the Penryn family of processors SFF BGA.***

In the end, the core power-delivery simulation results for both packages were closely correlated with the IFDIM [1] measurement in the validation cycle. Also, the simulation model was correlated to the Pico probe measurement on the package processor voltage sense points.

PACKAGE DESIGN TEAM'S CHALLENGE

The mobility package design team for the Penryn family of processors included only four team members: a design engineer, a requirement engineer, a platform power-delivery engineer, and a layout designer. This extremely small team faced the additional challenge of being geographically dispersed. Initially, team coordination was extremely challenging, especially since the dispersal of team members spanned multiple continents with all the inherent time differences. After aligning the work flow, this setup actually worked to the team's advantage and enabled the team to meet and beat multiple package design deliverables. For example, at the beginning of the typical cycle, team members located in the U.S. did what-if changes and analysis to the package design database. At the end of the U.S. workday, designers passed on the preliminary design database to the package layout team member in Malaysia. The Malaysian team member performed layout design rule cleanup and production-worthy implementation of changes and then, at the end of the Malaysia work day, passed on the design to the team member located in India. The Indian team member completed power-delivery network extraction, did the simulations from layout, and identified any processor performance impacts. In the event that processor IO FSB performance might be impacted, simulation models for stakeholders located in Israel were generated. Israeli stakeholders used layout-modeled data for FSB performance impact analysis, identified issues, and recommended solutions during their working hours. By the time US team members came back to work on their next business day, the team had already completed the extraction, simulation, and analysis of "yesterday's" work, thereby compressing the four-day wait time of co-located design teams into one twenty-four-hour work cycle. This work model was perfected and used by the package design team throughout multiple Penryn mobility processor package design flavors. It enabled the team to design more than seven mobility packages with less than typical staffing, and in one case, finished four weeks earlier than the originally agreed-upon package tapeout schedule.

CONCLUSION

By coordinating the roles and workflow of the geographically distributed team members, this small group was able to deliver the Penryn family of processors' 3-MB design implemented with the lowest possible package layer count and capacitors, returning significant cost savings over the life of the product. Likewise, the team was able to leverage this design strategy to tape out the first mainstream SFF mobility product in just nine weeks, despite the challenge of pinmap definition and bottom-up package design, thus enabling customers to design both smaller and thinner form-factor platforms.

ACKNOWLEDGEMENTS

We recognize Nicole Pedrami and Rob Milstrey for their contributions to the content and their review of this paper.

REFERENCES

[1] A. Waizman . "Integrated power supply frequency domain impedance meter (IFDIM)" In Proceedings of IEEE: 13th Topical Meeting on Electrical Performance of Electronic Packaging 2004, pp. 217–220.

AUTHORS' BIOGRAPHIES

Kyan Pedrami is a Staff Enginner in the Mobility Processor Design team and has been with Folsom Design Center since 1997. Before joining Intel, he worked at Digital Semiconductor in Maynard, MA. Kyan obtained his B.A. and M.A. degrees in Electrical Engineering from the Georgia Institute of Technology. His e-mail is kyan.pedrami at intel.com.

Satish Prathaban is a Senior Hardware Design Engineer in the Mobile Platform Hardware and Development team. He has an M-Tech degree from IISc-Bangalore. He started working at Intel India in 2003 in the area of motherboard and package power delivery. His e-mail is satish.prathaban at intel.com.

Any codenames featured in this document are used internally within Intel to identify products that are in development and not yet publicly announced for release. For ease of reference, some codenames have been used in this document for products that have already been released. Customers, licensees, and other third parties are not authorized by Intel to use codenames in advertising, promotion or marketing of any product or services and any such use of Intel's internal codenames is at the sole risk of the user.

BunnyPeople, Celeron, Celeron Inside, Centrino, Centrino logo, Core Inside, FlashFile, i960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel Core, Intel Inside, Intel Inside logo, Intel. Leap ahead., Intel. Leap ahead. logo, Intel NetBurst, Intel NetMerge, Intel NetStructure, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel Viiv, Intel vPro, Intel XScale, IPLink, Itanium, Itanium Inside, MCS, MMX, Oplus, OverDrive, PDCharm, Pentium, Pentium Inside, skoool, Sound Mark, The Journey Inside, VTune, Xeon, and Xeon Inside are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Intel's trademarks may be used publicly with permission only from Intel. Fair use of Intel's trademarks in advertising and promotion of Intel products requires proper acknowledgement.

*Other names and brands may be claimed as the property of others.

Microsoft, Windows, and the Windows logo are trademarks, or registered trademarks of Microsoft Corporation in the United States and/or other countries.

Bluetooth is a trademark owned by its proprietor and used by Intel Corporation under license.

Intel Corporation uses the Palm OS® Ready mark under license from Palm, Inc.

LEED - Leadership in Energy & Environmental Design (LEED®)

Copyright © 2008 Intel Corporation. All rights reserved.

Additional legal notices at: http://www.intel.com/sites/corporate/tradmarx.htm