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The Technical Challenges of Transitioning Intel[®] PRO/Wireless Solutions to a Half-Mini Card

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ABSTRACT

With the introduction of Intel's latest mobile platform, Montevina, which is based on the new Penryn Mobile family of processors, the Intel® Pro/Wireless 5300 and 5100 communication daughter boards, offered as part of the Intel Centrino® Mobile Technology platform, also underwent major changes to enable a smaller, more efficient platform solution. The 5300/5100 family of Wi-Fi wireless communications boards is now offered in a Half-Mini Card form factor. This paper describes some of the technical challenges faced when transitioning from a Full-Mini Card used in previous-generation wireless solutions to a half-size card while increasing the functionality on board. These challenges have directly affected the entire design from the core silicon all the way up to the complete product board, not to mention some of the challenges to address at the Peripheral Component Interconnect Special Interest Group (PCI-SIG), from a standardization point of view. Background information will be provided to better understand why this transition was driven in the platform.

In this paper, we will touch on the required Printed Circuit Board (PCB) technology, front-end integration, silicon floor planning, pinout definitions, and the thermal considerations necessary to enable this transition. Further, we will show how this new form factor differs from its predecessors in some key aspects, as wireless communication has progressed from generation to generation. The reader will gain a good understanding of some of the technological challenges driven by this form-factor change that will enable smaller, more condensed platform solutions.

INTRODUCTION

In this paper we give a brief overview of the technical challenges involved in transitioning the Intel® PRO/Wireless Wi-Fi solutions from a Full-Mini Card to a Half-Mini Card form factor. (We use the terms "Full-Mini Card" and "Mini Card" interchangeably.)

Over the past generations of Intel PRO/Wireless solutions, the team has been asked to continually increase functionality while decreasing board size. Figure 1 shows the evolution of form factors starting with the original Mini Peripheral Component Interconnect (PCI) form factor of choice at the launch of the first Intel Centrino® Mobile Technology (CMT) platforms back in 2004–2005. The Intel PRO/Wireless 2100/2200/2915 series were all implemented using this Mini PCI Card form factor. In 2006, a new smaller form factor and Host Interface were introduced into the platform—the Mini Card—with a high-speed PCI Express interface. The intent of this smaller form factor was to enable the incorporation of two Mini Cards in the available space of the older Mini PCI Card, thus enabling more functionality in the platform. The Intel PRO/Wireless 3945abg was Intel's first IEEE 802.11abg Wi-Fi solution using this new form factor, which was part of the Napa family of CMT platforms. As the IEEE 802.11 Wi-Fi standard evolved, a new higher throughput technology was introduced called IEEE 802.11n that enables a Multiple In Multiple Out (MIMO) communication scheme. One of the key features of this new scheme is higher data throughput. The Intel PRO/Wireless 4965 was Intel's first IEEE 802.11n Draft MIMO solution to the market. It has two transmitters and three receive chains for data rates

up to 300 Mbps, using the same Mini Card form factor: in previous-generation technologies, there was only a single transmitter and a single receive chain. This amounts to a functionality compaction factor of 2.5:1 and a data throughput improvement factor of 5:1. This new wireless solution was introduced into the market at the end of 2006 and continues to be provided on the Santa Rosa CMT platforms.

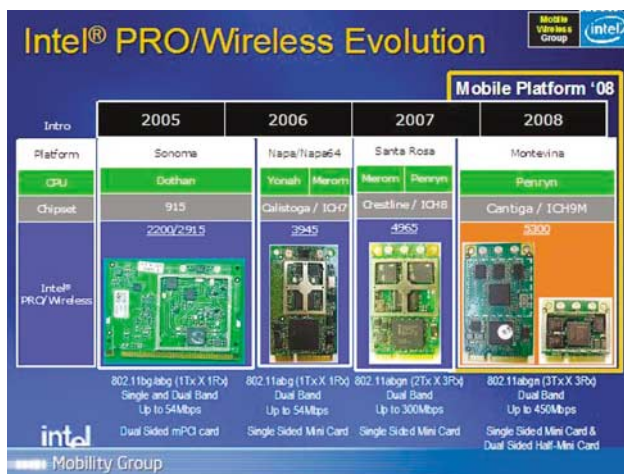


Figure 1: Intel® PRO/Wireless evolution.

However, the ‘ever hungry’ market demands more functionality in less space. This market demand drove the development of a new form factor called the Half-Mini Card. Again, the intent is to enable platform integrators to put more wireless content into the platform by placing two Half-Mini Cards in the space where they once put a single Full-Mini Card just one generation ago. With respect to performance, the intent is to also improve the throughput by a factor of 1.5:1 thereby reaching data throughputs of up to 450 Mbps.

In this paper, we describe some of the technical challenges and solutions the team faced while implementing this newer, smaller Half-Mini Card form factor while also increasing the functionality of the Wi-Fi system to a full three-transmitter and three-receiver 802.11n MIMO functionality. We discuss these issues in this paper:

- Half-Mini Card form factor standardization in the PCI-Special Interest Group (PCI-SIG)
- The Intel PRO/Wireless 5000 series of network adaptors
- Component and functionality partitioning
- Mechanical and physical requirements
- Printed Circuit Board (PCB) requirements

- Radio Frequency (RF) component sizes and challenges to meet regulatory emission certification requirements
- Thermal considerations and challenges

The team successfully met these challenges with the introduction of this latest family of Intel PRO/Wireless solutions 5300 and 5100 that are an integral part of the Montevina CMT platforms, by using the new Half-Mini Card form factor. These network adaptors will also be offered to customers in the older Full-Mini Card for the benefit of Original Equipment Manufacturers (OEMs) who continue to support the older, larger, single-sided form factor. This fact will also serve as a basis for comparison to better explain the challenges of converting the same product to the new, smaller Half-Mini Card form factor.

DEVELOPING THE PCI EXPRESS HALF-MINI CARD SPECIFICATION

With an increasing market pressure to integrate more and more wireless radio functionality into thinner and lighter notebook designs, the PCI-SIG in early 2004 was asked by some platform OEMs to consider space-saving alternatives to the PCI Express Mini Card specification that had been released only one year earlier and had yet to even have products developed based on it. Platform OEMs were heavily motivated by the need to figure out how to enable getting an increasing number of separate wireless radios into the already tightly-packed base of the notebook and by the need to establish a development roadmap toward a more space-efficient card format that wireless technology suppliers could eventually move to.

Starting in December 2005, the PCI-SIG Mini Working Group (WG) initiated the development of a specification for what would ultimately come to be known as the Half-Mini Card. The primary objective was to define a smaller variant of the PCI Express Mini Card, now to be known as the Full-Mini Card, which would enable notebook designs to accommodate an increased number of wireless cards while keeping the platform base volume associated with wireless applications at parity. The goal was to potentially get two smaller cards in the space of the one larger card while retaining interface and socket connector compatibility across the two card types. In this effort, the Mini WG, consisting of ten voting and seven observing member companies, succeeded in completing an acceptable specification in just over six months.

Figure 2 overlays color-highlighted card outlines aligned at a top-right origin to visually compare the decreasing planar size progression as the standardized card form factors shrank from the original Mini PCI Card (shown

in green) down through to the Full-Mini Card (blue) and toward the Half-Mini Card (red). It should be noted that no change to the z-height and assembly stack-up profile of the Mini Card was made going from the Full-Mini Card to the Half-Mini Card format. If solely based on the outline dimensions of the Half-Mini Card, the format appears to be slightly larger than half the size of the Full-Mini Card, 804 mm² versus 1528.5 mm², but the practical area for functional circuitry collectively across both top and bottom sides of the card is actually smaller than half, 1220 mm² versus 2670 mm², or about 45 percent of the useful area.

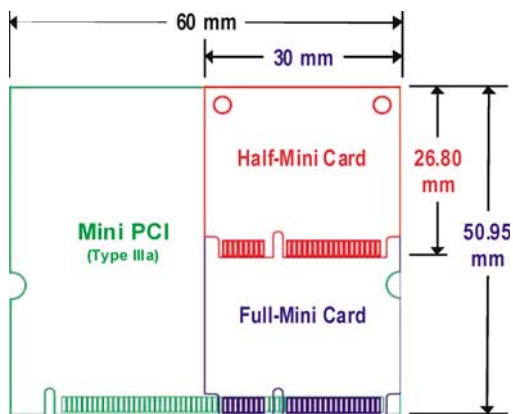


Figure 2: Comparing standardized card sizes.

The most critical factors in determining the size and shape specification of the smaller Mini Card included the area and volume reduction impact for circuit components, thermal density, and cooling impacts, and considerations for supporting a socket configuration that allowed for sharing between the larger and smaller cards.

Even as many wireless circuit technologies are progressing down a size-reduction roadmap, the proposed smaller Half-Mini Card format represented a challenge for both existing and emerging technologies. Initially proposed at being just less than half the size of the existing Mini Card, at one point there was even a proposal on the table for a smaller card on which the usable circuit area volume could have been reduced to as little as 37 percent. To help resolve the debate, each WG member company was asked to perform an independent feasibility review to determine if the smaller proposed sizes would be too constraining. Intel’s considerable internal review included analyses of six different wireless technologies (for LAN, WAN, PAN, and digital TV), both singularly and in some likely product combinations, and it took into account technology reduction trends over a period of many years. The result was that there was strong evidence that not all wireless applications would be relevant in the smaller card form factors. For a majority of the

specification development period, the WG settled on a target of 24.6 mm in length while keeping the card width the same as that of the Full-Mini Card. In the end, and after an even more extensive detailed review by Intel, the final dimension was increased to 26.8 mm to better accommodate a wider range of applications.

By its very nature, wireless technology can generate considerable thermal dissipation, this proving to be a key technical issue that an earlier concept to integrate wireless technology within notebook lids was unable to resolve. As a general rule, as the card format is reduced in size, the thermal density of a given application, when considered over its volume, is increased, and the cooling solution becomes more important. Unfortunately, reducing the size of a given radio technology doesn’t necessarily imply a reduction in thermal dissipation. However, as it turns out, the most common cooling issues with a radio solution are often localized to the area around the power amplifiers. With Half-Mini Card designs, the concentration of this dissipated heat doesn’t dramatically change. The WG chose to keep the thermal dissipation allowance the same between the two sizes of cards, but the notebook system designer must be cautioned that if two Half-Mini Cards are specifically placed within the platform to fill the previous space of a Full-Mini Card, then the cooling design for that space must take into account the potential doubling of the thermal dissipation.

Finally, the last major consideration was the potential re-configurability of a Mini Card socket, especially if the selection of Mini Card options that are to be offered for a given notebook platform design will include both standardized sizes. The primary factors in managing this include the orientation and placement of the socket connector(s) and the method used for holding the installed card in place (using the defined screw holes located at the corners of the card). Figure 3 illustrates how a socket can be configured for dual-use, given a second set of hold-down positions, with these hold-down points often being implemented as a boss and screw arrangement.

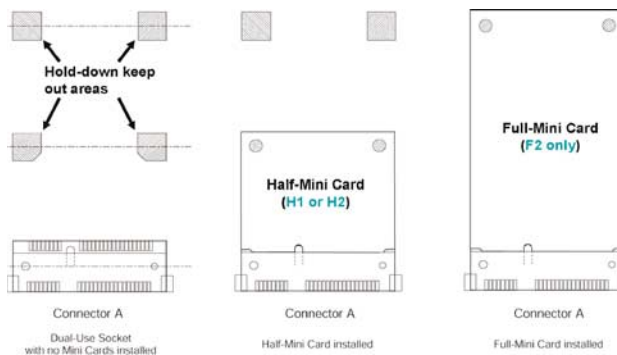


Figure 3: Dual-use socket concept.

In light of this dual-use configuration and another that specified a head-to-head configuration allowing for two opposing Half-Mini Card sockets that also support substituting a single Full-Mini Card, we defined options related to the bottom side keep-out areas of the Mini Cards to promote interoperability in multi-use sockets. In Table 1 we summarize the Mini Card and multi-use socket compatibility options that were defined. Notebook OEMs are allowed to also consider other configurations including just simply isolating and positioning individual sockets in convenient locations throughout the platform.

| ↓ Card Type ↓ | | Dual-use Socket | Dual Head-to-Head Sockets | |
|---------------|--|-----------------|---------------------------|----------|
| | | Socket A | Socket A | Socket B |
| F1 | Full-Mini Card ^a | No | No | No |
| F2 | Full-Mini Card with extra bottom-side keep-out areas | Yes | Yes | No |
| H1 | Half-Mini Card | Yes | Yes | No |
| H2 | Half-Mini Card with extra bottom-side keep-out areas | Yes | Yes | Yes |

^aSame as original Mini Card.

The remainder of the functional and performance specifications for both Full- and Half-Mini Cards is identical, including the support for both PCI Express and USB as the system I/O interfaces, the defined wireless-specific signaling features, and the available power-delivery pins. A recent unrelated change to the Mini Card specifications restructured the power supply interface to align on two voltage sources instead of three and to allocate more pins to power delivery as a means to reduce voltage drop across the interface. All of the changes that we discuss are normatively covered by Revision 1.2 (dated October 27, 2007) of the specification [1].

Intel's role in all of the Mini Card standardization efforts to date has been unique in that we are the only participating technology supplier delivering at both the notebook system chipset and the wireless communications levels. As such, Intel has been able to supply a broad range of technical expertise to review and guide the specification development activities. As the technical editor for PCI-SIG Mini WG, we have also been able to play a leadership role in establishing useful specification requirements across a diverse set of

industry participants including three major notebook OEMs, a number of wireless technology suppliers, and a number of connector suppliers.

INTEL® PRO/WIRELESS 5000

Wi-Fi solutions

The Intel PRO/Wireless series 5000 of network adaptors targets both premium and value-market segments. The premium device called 5300 is a full IEEE 802.11n MIMO three-transmit and three-receive (also known as 3 × 3) chains, dual band (2.4GHz and 5–6GHz) Wi-Fi solution. This enables the user to achieve up to 450 Mbps over the air data throughput, using standard communication protocols in both the Up Link (UL) and Down Link (DL) directions. This MIMO 3 × 3 scheme generally improves the data throughput vs. distance performance in a multi-path environment typical of indoor wireless connectivity, as expected in a premium device.

The value network adaptor device called 5100 is a scaled-down version of the 5300 premium network adaptor. It offers a MIMO 1 × 2 scheme (one transmit and two receive chains) and also supports dual band. This MIMO configuration offers a data throughput of up to 300 Mbps in the DL direction and up to 150 Mbps in the UP direction. This coincides with typical usage models in which we usually want to receive more than we actually want to send.

For the purposes of this paper, we concentrate on the Intel PRO/Wireless 5300 device, mainly because this was the more challenging of the two. However, our discussion is also applicable to the 5100 device in a more limited capacity.

In Figure 4 we show a general block diagram of the Intel PRO/Wireless 5300 Wi-Fi 3 × 3 solution. The main building blocks incorporated in the solution are these:

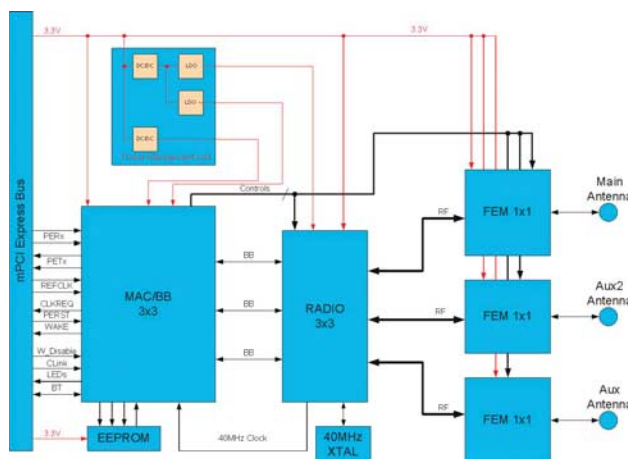


Figure 4: Intel PRO Wireless 5300 block diagram.

- The Media Access Controller and Base Band chip (also known as MAC/BB)
- The Radio Transceiver chip (also known as Radio)
- The Front End Module (FEM)
- The Power Management Unit (PMU)
- The EEPROM
- Xtal

The MAC BB chip serves as the Host Interface that is the main connection to the rest of the CMT platform. It is also directly connected to the Radio Transceiver. The Radio Transceiver contains three Radio Frequency (RF) chains, each containing transmit and receive circuitry that supports both unlicensed Wi-Fi communications bands of 2.4 GHz and 5–6 GHz. The Radio Transceiver in turn is connected to three front-end circuits that are used to amplify and filter the RF signals connected to the antenna ports. The PMU supplies all the necessary bias voltages used in the system that are not directly received from the platform power source. The EEPROM device is used to store some of the key board-specific information such as MAC Address, Regulatory Parameters, and Calibration Tables that are programmed into the device during production. The Xtal is connected to an internal Crystal Oscillator (XO) circuit that generates the required clock and signal reference in the system.

TECHNICAL CHALLENGES AND SOLUTIONS

Shrinking the full-mini card down to a half-mini card

The Intel PRO/Wireless 5300 family of network adaptors is targeted to be offered in two form-factor flavors: (1) the Full-Mini Card and (2) the Half-Mini Card. The Full-Mini Card solution was defined as a single-sided solution with all components on the top side of the PCB. The intent is to support OEM customers who want to make use of the space underneath the Mini Card. With the available room on the top side of the Mini Card, we typically subdivide it into two distinct sections: (1) the high frequency RF section including the Radio Transceiver chip and all the front-end components that reside under an EMI RFI shielded enclosure, and (2) the rest of the circuitry that is not as EMI/RFI sensitive and can sit on the board unshielded.

To meet the required functionality of the Intel PRO/Wireless 5300 Network Adaptor, almost all the available area of the Full-Mini Card is populated with hardware components. Therefore, it is fairly obvious

that in order to fit on the Half-Mini Card with the same hardware content that is half the board size, some of the components will need to reside on the bottom side of the Half-Mini Card board. We can look at this as if we are taking the Mini Card board and folding it on itself to create a board that is half the length but is now two sided and has components on the top and bottom of the board, as shown in Figure 5.

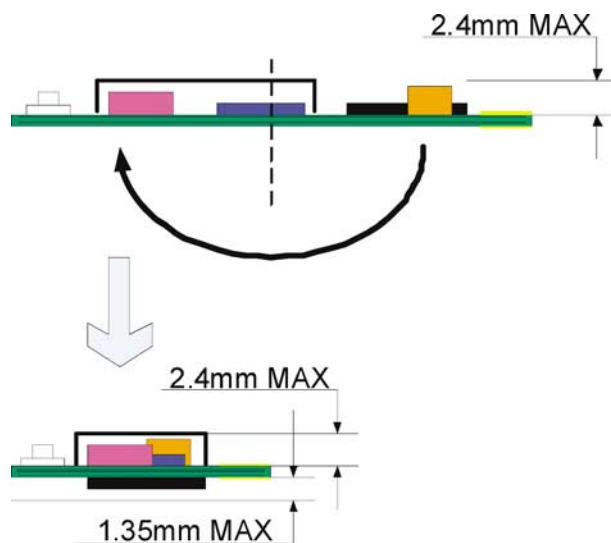


Figure 5: *Folding the single-sided Full-Mini Card to yield a dual-sided Half-Mini Card.*

The actual partitioning of what needs to reside on the top side and what can sit on the bottom side is mainly driven by the z-height limitations of the components and the z-height restriction per the Mini Card specification. The maximum z-height above the board is 2.40 mm, while the maximum z-height below the board is 1.35 mm. These restrictions remain the same for the Full-Mini Card and the Half-Mini Card even though we used only the top side for our previous-generation solutions. In our case of transitioning to the Half-Mini Card, the RF shielded portion is more suited to sit on the top side of the board, where the extra height is needed, driving almost all other low-profile components to the bottom.

However, based on the Half-Mini Card mechanical specification, the area on the top side that is available to be shielded is actually further limited in comparison to the Mini Card board. This is due mainly to the large mounting hole and antenna interface section at the end of the board that remain the same for both form factors. This section does not scale in size when the board is shortened to half the length. It is only shifted! So, effectively, we have less room for the RF section under the shield of a Half-Mini Card. Knowing this

fact a priori drove the development of highly integrated front-end modules to save space and enable all of the RF section, including the Radio Transceiver, to fit inside the shield of the Half-Mini Card board.

With the RF section on top, we are forced to push the rest of the components to the bottom side. This means that they need to comply with the low-profile requirements to ensure that the board complies with the z-height restrictions of the Mini Card specification. Several non-compliant components were identified; specifically the power inductors used in conjunction with the DC DC converters. This fact spurred a search for low-profile substitutes. However, the low-profile substitutes found were three times more expensive than the original part. The team was asked to find some way to place the original component on the top side as part of a cost-saving opportunity. Initially, a solution was proposed whereby the inductors reside on top outside the shielded area because it was feared that the switching noise generated in these inductors would somehow contaminate the RF signals. However, we found that the overhead of this type of solution took up too much of the precious board space needed for the RF section under the shield. We devised a simple Design of Experiment (DoE) whereby we designed a board with the power inductors inside the shielded enclosure. We tested the DoE and proved beyond a shadow of a doubt that noise contamination was not an issue. This became the Plan Of Record, and the original high z-height/lower-cost inductors are incorporated within the shielded enclosure area, leaving enough area for the RF components.

We still had more challenges to overcome, however, and these are described in the next sections.

REQUIRED PCB TECHNOLOGY

The PCB technology typically used for Mini Card designs is a lower-cost, standard through-hole via (THV) design, comparable to an industry-standard IPC Type 3 PCB. This was possible for two main reasons. The first is that there are no components on the bottom side of the Mini Card designs for the THVs to come in contact with. The second is that we were able to design the component packaging to not require any high-density interconnect (HDI) PCB technology. When we transitioned to a Half-Mini Card we were very limited on PCB area for components, so we had to utilize the bottom side of the PCB for components. The density of the components on both sides left us no room to place the THVs we had used on the Mini Card designs. This forced us to transition to HDI PCB technology. We needed a way to connect the I O between components without taking up the valuable

component real-estate on the outer layers with THVs. Rather than using THV technology to solve the real-estate issues, we used HDI PCB technology in the form of a microvia and buried via technology. Microvias are about half the diameter of the previous THV technology. We could also utilize them in component pads to eliminate any real-estate lost from I O connection and routing on the outer layers. This is comparable to the industry standard IPC Type 4 and Type II PCB [2,3]. The two types of PCB structures are featured in Figure 6, where the differences can be clearly seen.

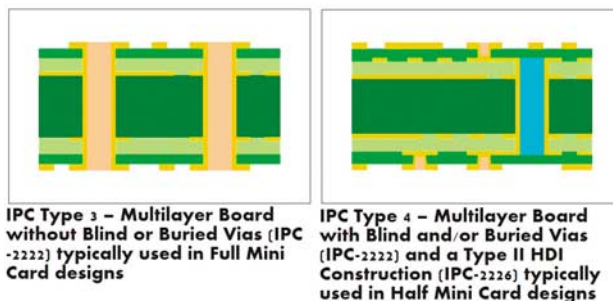


Figure 6: The PCB structure change between Full-Mini Card and Half-Mini Card.

Though the new Half-Mini Card PCB size was almost half the size of our previous Mini-Card designs, our overall PCB cost was increased by the PCB technology transition. The cost increase came from several areas. The layer count was increased: extra PCB processing time was required for the sequential lamination process for the microvia and buried vias. There was an increase in added drilling steps from one THV mechanical drill step to four drill steps, that is, two laser drills and two mechanical drills. All these changes to the processing of the PCB for Half-Mini Card outweighed the savings of the smaller PCB size. However, we did not change the component packaging technology to utilize the HDI PCB technology. We did this so that our Mini Card and Half-Mini Card design could use the same components. This made it more challenging for the component packaging development, but it kept our cost down for the Mini Card PCB version by not having to transition it to HDI PCB technology.

SILICON PARTITIONING AND CONNECTIVITY ON THE PCB

One of the key challenges the team faced was the fact that the same MAC BB chip would need to reside on either the top side of the Mini Card form factor or on the bottom side of the Half-Mini Card form factor. However, the pinout could be optimized with direct routing and connectivity for only one of the cases. This means that when the MAC BB is placed on either side

of the board, the pinout interface ordering is either in line or reversed in order. This reversal of pin alignment adds to the routing complexity and introduces adverse coupling and signal integrity effects due to trace crossovers not encountered in the case of direct routing. This is also true of the signals that go between the MAC BB chip and the Radio Transceiver chip for the same reasons. The dilemma we faced was which version should we optimize.

In the end, the PCB constraint and capabilities finally drove a decision with regard to the MAC BB pinout scheme:

- (a) PCB cost is a function of board size and board complexity. Since the Mini Card is the larger of the two boards, we can only reduce the complexity to maintain low cost. So a THV with a minimum number of layers is used for routing. This can be achieved only with direct point-to-point routing.
- (b) The Half-Mini Card solution requires component placement on both sides of the board, driving us to a more complex HDI PCB technology that can also support more complex component routing as needed.

Based on these reasons, the team decided to optimize the MAC BB pinout for the Full-Mini Card arrangement.

During the actual layout and routing of the MAC BB signals in the Half-Mini Card HDI PCB, many routing tricks were used to take advantage of the more complex board technology, including large indirect loop routing to circumvent and avoid other traces, layer play, and in some cases component rotations. These enabled us to route critical signals without any crossovers or adverse coupling effects. In this way, we avoided degraded signal integrity, something that is especially critical for the PCI Express Host Interface signals and all of the Analog Base Band signals. All of these are also differential pairs that require special care.

Front end module (FEM) definition and board placement

The Network Adaptor chipset transceiver needs to be complemented by an external set of RF front-end components that are located directly between the Radio Transceiver chip and the antenna connection. This includes a pair of Power Amplifier (PAs), a pair of Low Noise Amplifiers (LNAs), a Diplexer, a set of Baluns (BALanced UNbalanced transformers), and a pair of Transmit Receive Switches.

Due to the fact that the required front-end content is fairly large, and our network adaptor supports a MIMO 3×3 system that needs three such front ends, we needed three highly integrated FEMs. The FEM size definition was driven mainly by the limited space available under the shield of a Half-Mini Card board and the required RF content within. The FEM pinout was synchronized with the Radio Transceiver pinout for direct pin-to-pin routing.

What is noticeable about FEMs is the fact that in the Full-Mini Card configuration, all three FEMs can sit snugly side by side and connect directly to their respective antenna and Radio Transceiver interfaces. This can be seen by the many traces running on the top layer of the PCB. However, in the Half-Mini Card scenario, the FEM locations had to be moved and rotated to either side of the Radio Transceiver. This burden made it extremely difficult to route the RF traces on the top side, and many of the RF traces needed to be embedded into inner layers. Special care needed to be taken to maintain trace impedances without sacrificing performance, something that was accomplished through careful play with the trace widths and the layer stack-up of the PCB.

We defined the actual FEM sizes through an iterative process. First, the Computer Aided Design Manufacturing Engineering team at Intel examined the board area available under the shield, taking into consideration industry assembly design rules and the system connectivity requirements. The FEM estimated sizes were then presented to multiple FEM vendors for evaluation. The FEM vendors were also given the FEM content requirements in the form of a specification document. After trimming down the content to exclude a pair of Baluns, the vendors confirmed that they could 'fit' the necessary content to within the target size of 6x4mm. The removal of the pair of Baluns was also acceptable by the Radio Transceiver design team. Finally, the FEM pinout was also defined with the aid of the vendors, taking into consideration their implementation requirements and our RF interface requirements with the Radio Transceiver chip.

Thus, with careful iterative planning, we were able to fit all the RF content within the smaller shielded area of the Half-Mini Card.

Regulatory emissions concerns and challenges

Even with all our careful planning and design, there was no guarantee that we would meet all emission requirements. The transition to Half-Mini Card with dual-sided assembly added complexity to the PCB routing and required a change to the metallization layer stack-up. Both of these changes can introduce

new potential sources of unwanted emissions from the board, but they also can bring new opportunities to overcome emission and other performance issues.

Through a combination of good design practices and drawing on our previous RF experience with former generations of PRO/Wireless solutions, the hardware design team identified three main items that require special care during the board layout design. Careful attention was given to proper grounding and the use of microvias (uVias) and power traces. These practices have a huge impact on overall performance and on the ability of our product to meet regulatory certification that enables worldwide use.

1. Grounds (GND)

With the increased number of layers on the Half-Mini Card, we decided to also increase the number of ground layers in the PCB stack-up. This was done for several reasons:

- GND pour and routing is critical to ensure expected performance of RF components as tested and approved in a standalone environment. Poor grounding might cause limited performance of key radio components such as the FEM. It might adversely affect output power, EVM level (a standard signal quality factor measurement unit used in phase and amplitude modulation systems), and cause spurious and harmonic emissions.
- Multiple ground layers enabled us to easily support different impedances (100 ohms, 50 ohms) of RF strip-lines while maintaining reasonable line widths. Homogenous and uninterrupted ground planes must surround and follow all RF and analog signal lines.
- Power lines and traces can be accompanied by a good ground path plane. This can be further improved if wide traces are sandwiched between two ground layers. The capacitance to GND increases and thus enables the removal of discrete high-frequency capacitors from the board. This not only frees up precious board space but can also save cost.
- IR drop on GND planes is minimized by multiple GND layers.
- Isolation of noisy sensitive control lines can be improved by routing them in internal layers next to a GND layer thereby enabling an uninterrupted ground return path.

2. Use of microvias (uVias)

To enable good grounding as mentioned above as well as optimized signal routing with the shortest possible

lines, it is essential to make use of uVias. Unlike THVs, uVias have an added advantage because of their small size: they occupy less board area, and they can be located within component pads for additional board-area savings. In general, a greater number of uVias can be spread all over the board to provide shorter paths to GND. Because of their small size, they can also be placed strategically at trace ends and corners. This minimizes the generation of stub-like lines of GND and other traces that can act as unwanted antennas generating unwanted emissions from the board. When routing power lines and traces, multiple uVias are needed to reduce IR (voltage) drops along the trace. Again, because of the uVias' small size, many can be placed within wide DC traces.

3. Power lines

Power lines and traces should be made as wide as possible in order to minimize IR drops and make use of multiple uVias between layers, especially those with high current loading. The wide lines/traces routed between two GND layers will also provide some high-frequency capacitance and minimize the need for many small value capacitors on the board for RF decoupling.

By incorporating these relatively simple Best Known Methods into the Half-Mini Card layout design, we were able to overcome issues such as degraded EVM performance, unwanted harmonics, and spurious radiation from the board. In some cases, multiple variants of the board layouts were in parallel in order to overcome these issues. In one such case, by strategically placing two additional uVias along a power trace leading to the FEMs, we improved the EVM performance and were able to remove a discrete decoupling capacitor from the board.

Thermal considerations

The Half-Mini Card specification calls for the same power-handling capability as that of the Full-Mini Card. However, the shrinking of the form factor from Mini Card to Half-Mini Card also introduced a new issue in the form of thermal power density. Basically, we are trying to dissipate the same amount of power that was previously dissipated on a Full-Mini Card in half the volume. In other words, the power dissipation is more concentrated. We feared that this would cause the T_{junction} of the MAC BB and Radio Transceiver silicon die to increase beyond the maximum acceptable temperature levels required to maintain performance and reliability.

In order to ensure that we do not exceed the max T_{junction} of the die, we conducted a series of thermal simulations taking into account a typical notebook

environment with our Half-Mini Card mounted on the bottom of the notebook motherboard. These simulations incorporated multiple variables that included the following:

- Package type
- Relative location of the key power dissipaters on the board
- Number of metal layers in the PCB and metallization thicknesses
- Actual power dissipation in each key component

The fact that the MAC BB and Radio Transceiver chips were designed for Wire Bond (WB) connectivity opened up an opportunity to examine various types of packages and combinations. We examined package types such as Ball Grid Array (BGA), Quad-Flat-No Lead (QFN), and others. Of these types, the QFN-type package offers the best theoretical power-dissipation capability. It has a large die paddle in the middle of the package on which the die is mounted, and it serves as a direct thermal conduit to the board. However, it should be noted that the number of interfaces with a QFN-type package is limited to the number of pads along the perimeter of the package. A Dual-Row QFN package offers more pads: two rings of pads along the perimeter. However, it also drives a larger package to house the same-size die. We had to look carefully at the tradeoff between thermal behavior and the number of interfaces.

Another parameter that plays a role in the thermal behavior is that we now have a two-sided board and need to add more metal layers to the PCB to accommodate the necessary side-to-side isolation and the added routing complexity. This increase in the number of layers (increase is in pairs to maintain symmetry) has a significant positive effect on the thermal behavior, and the added metallization layers actually enable us to dissipate more heat from the components on the board.

The relative location of the components on the board is quite limited in our case. The requirement to have all RF components on the top side under the shield meant that all other main power-dissipating components needed to reside on the bottom. This includes the MAC BB chip and the PMU. In light of the fact that there isn't a lot of room for the components to move around, only a few options need to be examined. The EEPROM has insignificant power dissipation; therefore, it could reside anywhere without really influencing the thermal behavior. Due to the space constrictions, however, it was placed on the bottom side.

The actual power-dissipation numbers selected to be used for the thermal simulation were a challenge in themselves. Under normal operating conditions, the system works in a dynamic mode based on the actual communication protocol. This means that the Network Adaptor sometimes transmits, sometimes receives, and sometimes is idle. The combination of these will yield a different average thermal behavior for different modes of communication. The worst-case scenario was identified as a MIMO 3×3 Transmit mode, which can occur for a duty cycle of greater than 97 percent when User Datagram Protocol (UDP) is used for high-throughput data communication. In this case, all the transmit chains are active and working almost all the time. The power amplifiers in the FEM are large power consumers. However, when in MIMO 3×3 mode, we are actually able to reduce the transmit power level of each FEM to a third of the maximum transmit level, approximately 5 dB lower, and this yields a collective transmit power of all three chains that will maintain the same total radiated power. This also means that each FEM will dissipate less power in this mode.

With all the various options described above, multiple simulations were conducted to examine the Tjunction of the chipset components. An example of such a simulation environment is shown in Figure 7. The result of this examination basically drove the following design guidelines:

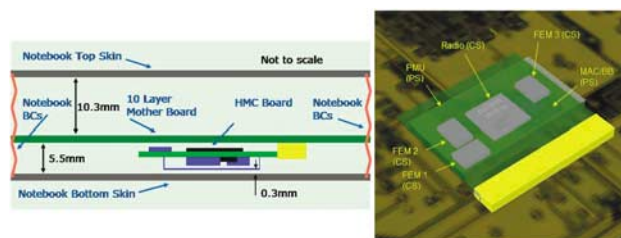


Figure 7: Thermal simulation in a notebook environment.

- Use QFN packages.
- Increase the number of PCB layers.
- Reduce the individual Tx power on each chain when working in MIMO modes.

Using these guidelines, the Intel PRO/Wireless 5300 Network Adaptor was designed and tested. Actual results correlate with the simulations and show that Tjunction does not exceed maximum Tjunction for the silicon when mounted on a Half-Mini Card. We also carried out the simulations and tests on the Full-Mini Card. The Full-Mini Card has the huge advantage of having a much larger PCB to dissipate the heat

generated by the components, enabling the implementation of a solution with a reduced number of PCB layers. The simulations clearly show that there are no issues whatsoever with the regular Mini Card product skew from a thermal point of view.

ACTUAL IMPLEMENTATION OF INTEL PRO/WIRELESS 5300

The saying “a picture is worth a thousand words” is certainly applicable in this case. Figure 8 shows the actual implementations of the same Intel PRO/Wireless 5300 Network Adaptor Mini Card and Half-Mini Card. It clearly shows how the component partitioning was done keeping the RF shielded components on the top side (component side) and putting low-profile components on the bottom side (print side). The shield size reduction and tight fit of all the RF components under the shielded area shows the necessity to integrate the FEMs. It can also be seen that the tall power inductors (bottom right-hand corner inside the shielded area) are on the top side to enable the lower-cost option. Looking at the MAC BB chip, it is clear that the direct and simplistic routing to the Radio Transceiver chip and to the Host Interface gold fingers connections are maintained in the Full-Mini Card version to enable lower-cost PCB technology. However, this direct and simplistic routing cannot be maintained in the Half-Mini Card version of the board. Nonetheless, the devices were successfully routed using more complex routing in multiple inner layers.

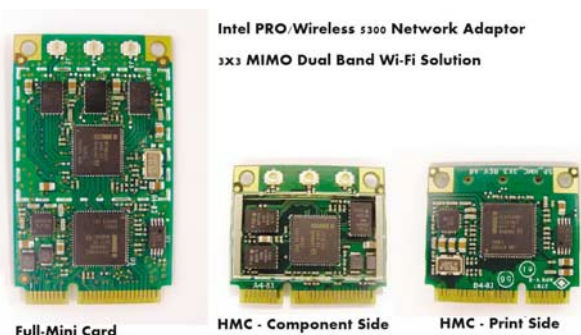


Figure 8: Intel® PRO Wireless 5300 network adaptor Full-Mini Card and Half-Mini Card implementations.

CONCLUSION

The trend to make things smaller with more functionality continues to be a key driving force for Intel PRO/Wireless solutions. As shown in this paper, the technology challenges of moving to a half Mini Card form factor have been met and or exceeded.

This quantum leap, when compared with the Wi-Fi solution offered in the original CMT platforms of 2004, has significantly changed the platform content and capability. The new board area, which is less than one quarter of the original board size and greater than six times in functionality (two times the bands supported and three times the number of transmit and receive chains), proves that such silicon and board challenges can be met.

This shrinkage of the Intel PRO/Wireless 5000 Wi-Fi 802.11n solution down to a Half-Mini Card form factor while increasing functionality has enabled our OEM customers to incorporate multiple add-in cards and increase wireless functionalities inside their latest Montevina CMT platforms. The OEMs can now offer higher-performing and smaller platform solutions compared with the previous-generation Santa Rosa CMT platforms.

Undoubtedly, the Half-Mini Card will become the industry standard form factor going forward. We expect the competition to also align with this trend. Although it is unclear how much our competitors will be able to integrate their solutions into this new form factor, Intel has taken it upon itself to be amongst the first to drive and adopt this new form factor standard from concept to product. The introduction of the 5300 series of Intel PRO/Wireless solutions, which is a full Dual-Band 3×3 MIMO IEEE 802.11n solution using this new Half-Mini Card form factor as part of the Montevina CMT platforms, is a testament to the Intel “Leap Ahead” corporate motto.

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Glossary

| | |
|----------------|--|
| MC | Mini Card, also referred to as Full-Mini Card |
| HMC | Half-Mini Card |
| CMT | Centrino™ Mobile Technology |
| WLAN | Wireless Local Area Network |
| MAC/BB | Media Access Controller/Base Band |
| MIMO | Multiple In Multiple Out |
| Mbps | megabits per second |
| PCI SIG | Peripheral Component Interconnect Special Interest Group |
| PCB | Printed Circuit Board |
| CS | Component Side (usually referred to as the top) |
| PS | Print Side (usually referred to as the bottom) |
| BGA | Ball Grid Array |
| QFN | Quad, Flat, No-lead |
| WB | Wire Bond |
| HDI | High Density Interconnect |
| THV | Through Hole Via |
| UVia | Microvia |
| RF | Radio Frequency |
| RFIC | Radio Frequency Integrated Circuit |
| FEM | Front End Module |
| PA | Power Amplifier |
| LNA | Low Noise Amplifier |
| PMU | Power Management Unit |
| DC/DC | Direct Current to Direct Current |
| EEPROM | Electrically Erasable Programmable Read Only Memory |
| IPC | Printed Circuit Standard body |
| EMI/RFI | Electro Magnetic Interference/Radio Frequency Interference |
| IR | Current x Resistance (voltage) |
| GND | Ground |
| EVM | Error Vector Magnitude |
| UL | Up Link |
| DL | Down Link |
| I/O | Input/Output |
| DB | decibel (a relative unit of measure) |
| T _j | Temperature @ die junction |
| WG | Work Group |
| BTO | Built To Order |
| LCD | Liquid Crystal Display |
| DoE | Design of Experiment |
| OEM | Original Equipment Manufacturer |
| USB | Universal Serial Bus |
| Xtal | Crystal |
| UDP | User Datagram Protocol |

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