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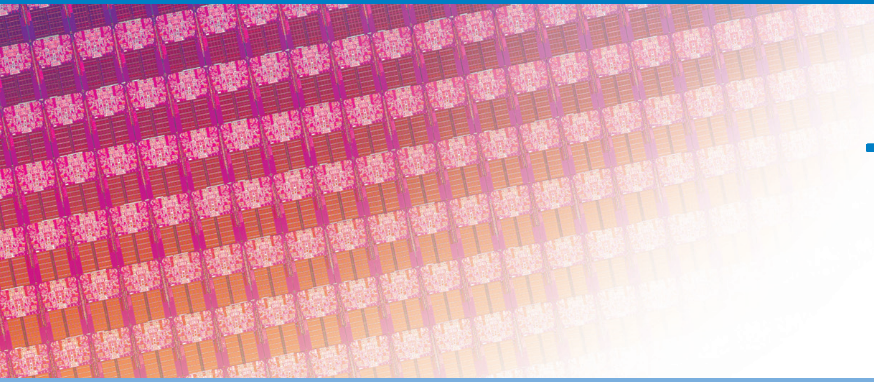

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Intel's 45nm CMOS Technology

Flip-Chip Packaging Technology for Enabling 45nm Products

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Index words: lead-free, flip chip, 45nm, packaging, form factor management

ABSTRACT

Intel's packaging team has been working on developing completely Pb-free packages that can be utilized in a variety of products and market segments including the newly emerging mobile Internet devices. These technologies have been introduced into high-volume manufacturing to enable packaging of 45nm silicon devices in 2007. In order to hit this milestone, a significant number of engineering challenges had to be overcome to select and integrate the new assembly materials into the complex interconnect structure of Intel's 45nm process technology. The new solder alloys for first-level interconnect resulted in significantly higher stress on the silicon, and the Intel team reengineered many aspects of the assembly materials and process technology to resolve the crucial problem and deliver this innovative technology. The change to lead-free (Pb-free) solder alloys necessitated the development of alternate flux materials to clean off the more tenacious tin oxides from the solder surface. The new flux material had to be stable at high process temperatures as well as cleanable following the chip attach process to allow strong adhesion between the underfill, the bump metallurgy, and the die passivation. The new Pb-free, first-level interconnect architecture is superior to the older materials in many aspects, including higher current-carrying capability, and it is more reliable and environmentally friendly, being 100% Pb-free. The development of the high-k 45nm devices also enables Intel to introduce high-performance microprocessors with very low power consumption. These devices enable development of fully functional personal-computer-like features in a hand-held device. However, in order to successfully integrate a 45nm silicon chip in a hand-held device, significant reduction in the form factor of the flip-chip package was essential. In order to achieve this goal, significant technology challenges were overcome through the introduction of new underfill material and process technologies. Further reduction in the z-height required die-thinning and introduction of thinner substrates. In this paper key technical challenges associated with Pb-free interconnect and form-factor reduction are discussed.

INTRODUCTION

Intel's 45nm technology portfolio includes the Penryn family of processors, which build on the success of the revolutionary core microarchitecture as well as the family of devices, based on Intel® Centrino® Atom™ processor technology, targeted for mobile Internet device applications. The Penryn family of processors features new dual-core desktop processors, quad-core desktop processors, quad-core server processors, and dual-core mobile processors. These new 45nm processors include features to improve performance at any given frequency:

they have up to 50% larger L2 caches and expanded power-management capabilities for new levels of energy efficiency [1]. The Intel® Atom™ processors have been developed from the ground up with the aim of minimizing the power consumption and yet enabling a high-performance fully functional chip for the mobile Internet device segment [2].

The introduction of 45nm products also marks the move to 100% Pb-free packages to meet Intel's environmental performance goals. Lead has been used generously in the past as the primary component of the metal alloy (a mixture of tin and lead) used to electrically connect the silicon processor to the motherboard via an organic package. The interconnect hierarchy is shown in Figure 1.

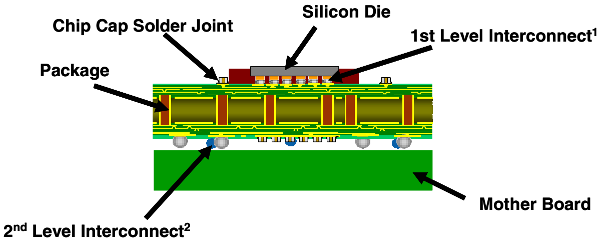

Figure 1: Schematic of a flip-chip ball grid array (FCBGA) pack

Due to the harmful impact of lead on the environment, however, Intel's engineers engineered a solution to get every last milligram of lead out of the package. The entire First-Level Interconnect (FLI) architecture was reengineered to be 100% Pb-free in a phased approach. In the first phase, Cu bumps were incorporated as part of the 65nm process technology CPUs [3] in place of the more compliant high *Pb*-bumps on the silicon die. This was followed by tin-silver-copper (SAC) solder in place of eutectic *Pb-Sn,* as part of the 45nm technology. The new architecture not only meets the stringent quality and reliability requirements of Intel products but also significantly improves bump cracking, bump electromigration, and solder fatigue performance, all of which are crucial to enabling reliable, high-performance microprocessors. Both *Cu*-bumps and SAC solder on the substrate are much stiffer than their leaded counterparts and impart significantly higher thermomechanical stress on the mechanically-weak, low-dielectric constant materials on the silicon die [4]. The use of a higher number of low-*k*-based metal layers in the 45nm products for improved interconnect performance further exacerbates the stress-management challenge. These challenges were resolved with an optimization of far back-end architecture, design, materials, and processes in both fab and assembly.

The move towards producing thin and light laptops and the need for improving the processing power in smart phones and mobile Internet devices has led to increased focus on the development of small form-factor, flip-chip package technologies that can accommodate full function, high I/O CPUs. In these market segments, the focus is on reducing the overall form factor of the package. This reduction in space is essential to enable system-level reduction in the motherboard size used in hand-held, mobile Internet device applications [2]. The drive towards smaller form factors places tremendous pressure on minimizing the area occupied by the flip-chip package and requires significant re-engineering of the flip-chip packaging technology.

In this paper we focus on the novel materials and processes that were developed in order to overcome these challenges to achieve 100% Pb-free interconnect as well as a significant reduction in the form factor for flip-chip packages.

FIRST-LEVEL LEAD-FREE INTERCONNECT

The 45nm process incorporates high-K+metal gate (HiK+MG) transistors for the first time along with third-generation strained silicon, nine copper interconnect layers, 193nm dry patterning, and 100% Pb-free packaging. A complete overview of the 45nm silicon process technology is given in [5]. The die far back-end architecture makes use of a very thick metal 9 (TM9) layer and a polymer dielectric, as shown in Figure 2. The integration of Pb-free solder with the novel TM9 architecture that employed a new dielectric/passivation material posed new challenges for material compatibility and M9 stack reliability, in addition to low-*k* dielectric material cracking/delamination. These issues were fully resolved through an iterative optimization of the metal interconnect, package design, materials, and processes within the fab and assembly.

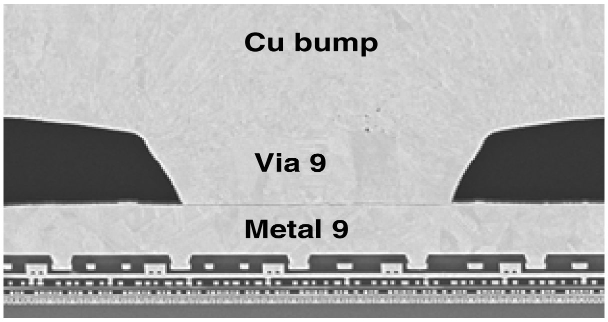

Figure 2: SEM depicting the M9 and V9 layers: M9/V9 is significantly thicker than all the other die metal layers

Challenges of First-level, Lead-free Interconnect

Compared to their leaded counterparts, tin-rich, Pb-free solder materials possess physical, metallurgical, and mechanical properties that pose significant challenges to flip-chip assembly and reliability. Their higher melting point (~30°C higher than SnPb) leads to an increase in the thermal expansion mismatch between silicon die and organic packaging and induces higher stress in the FLI solder joint compared to previous generations. The intrinsically higher mechanical stiffness of Pb-free solder and dramatically reduced mechanical strength of low-k dielectric materials of the silicon backend structures led to significant assembly challenges such as die Interlayer Dielectrics (ILD) cracking and occasional solder joint interfacial delamination (Figure 3). The inferior wettabililty of the Pb-free solder results in a reduced solder wicking with die copper column during chip attachment (Figure 4), and it considerably increases sensitivity to assembly-interaction-related failures, such as solder joint interconnect opens and non-wets, which require more stringent solder bump dimensional control. To achieve a healthy assembly yield for our Pb-free SAC process, tolerances, and sensitivities several new manufacturing process parameters had to be thoroughly studied, e.g., bump height variation and bump-level defects. Solder joint voiding is also of concern, as the outgassing of soldering flux residues becomes retarded due to higher surface tension and is accelerated by the ease of the tin oxide formation of the liquid solder.

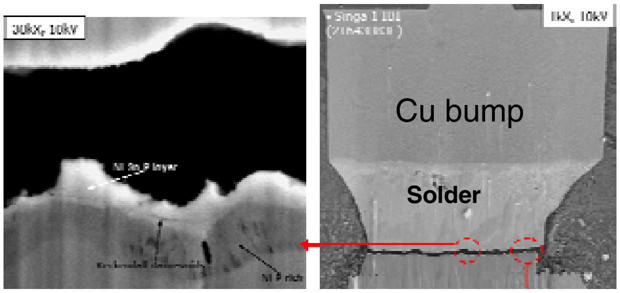

Figure 3: Solder joint delamination along solder/surface finish interface

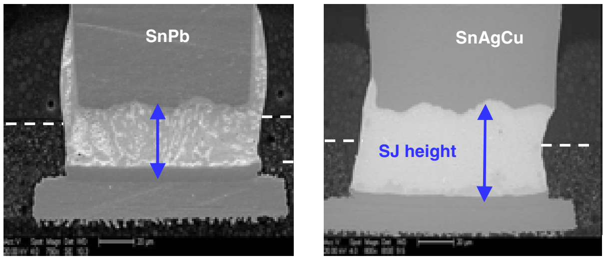

Figure 4: Reduced wettability of *SnAgCu* with die *Cu*-bump leads to a reduced solder joint collapse

The use of existing chip-attach fluxes developed for leaded solder alloys can cause significant defects, such as solder voids and interfacial nonwets, in the Pb-free FLI joints, due to the higher thermodynamic stability of the oxides in Pb-free solders. Furthermore, the need for higher peak temperature and Time Above Liquidus (TAL) for Pb-free solder can cause significantly higher flux residue to remain on the packages. Both these factors necessitated the development of a new flux that needed to be highly active in order to remove the thermodynamically stable tin oxides and improve wettability of solder to *Cu*. These new fluxes also had to have significantly reduced outgassing at reflow peak temperature and the TAL in order to reduce FLI voiding and in order to leave a residue that was easily cleanable by the hot water during the deflux process. In addition, the new flux formulations had to be compatible with the substrate solder resist material and the new die passivation material, have sufficient tackiness to prevent die misalignment and substrate solder bridging, and be capable of being printed or sprayed on the substrate.

The chip-attach process for flip-chip packaging follows these main steps: flux application, chip placement, reflow of chip joints, and cleaning of flux residue. Intel has been printing the flux in CPU packaging for many years. This process involves printing flux through an aperture opening in a stencil on the substrate bump area. This flux application process has worked very well for high-volume applications up to this point, but it has reached its limit for larger die sizes and multiple dies on a package. Using a flux printing process for larger and multiple dies can lead to scraping of substrate bumps that could potentially cause reliability problems such as non-wets, limited performance because of decreased maximum current-carrying capacity (referred to as IMAX), and reduced yield.

An out-of-the-box approach was pursued to enable a spray flux application process (SPRINT) by using a print flux material that was designed to be highly viscous at room temperature so it does not flow.

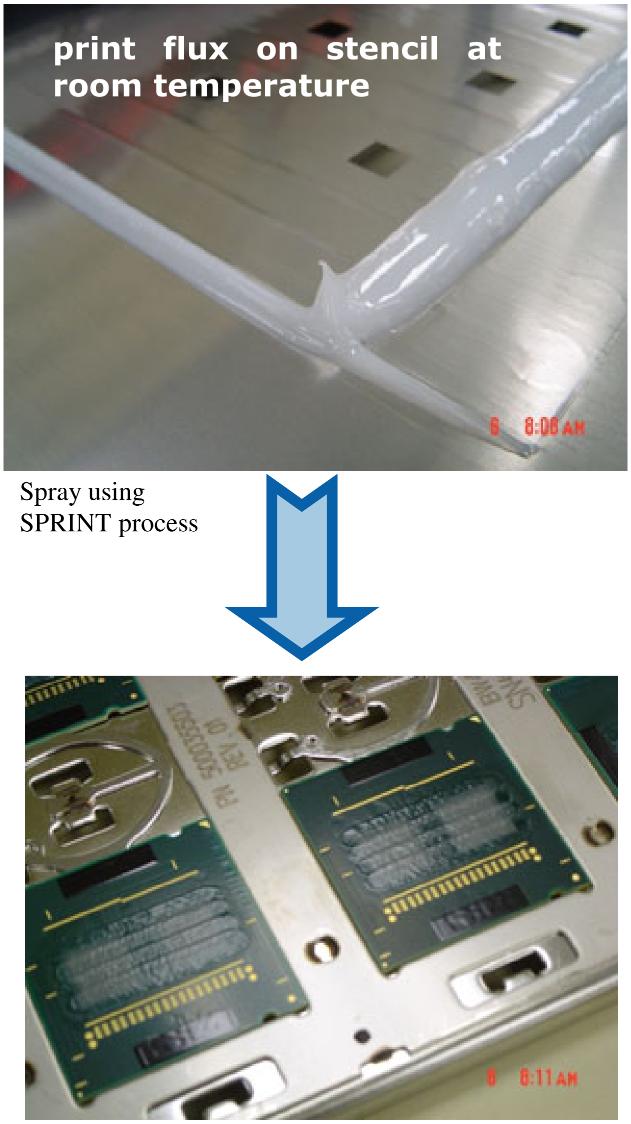

Figure 5: Conceptual description of "SPRINT" process—spraying a Print flux material using a dispenser

The print flux material is a non-Newtonian fluid with shear thinning properties. Several equipment and process changes had to be made to get the required dispense characteristics (Figure 5). An optimum fluid path heater design equipped with sufficient flux hold-up volume and heated to the target temperature prior to dispensing (Figure 6) was needed to enable a stable and capable dispensing process. Significant process characterization work had to be carried out to optimize different dispense parameters such as fluid and atomizing coaxial air-pressure, dispense temperature, dispense height and width, and line speed. The goal was to get just the right amount of flux on the substrate bumps: too little flux led to poor quality joints between substrate and die bumps, and too much flux caused die misalignment during the reflow process. All the process characterization work led to the fundamental understanding of the impact of flux dispense parameters on die misalignment yield and FLI joint quality.

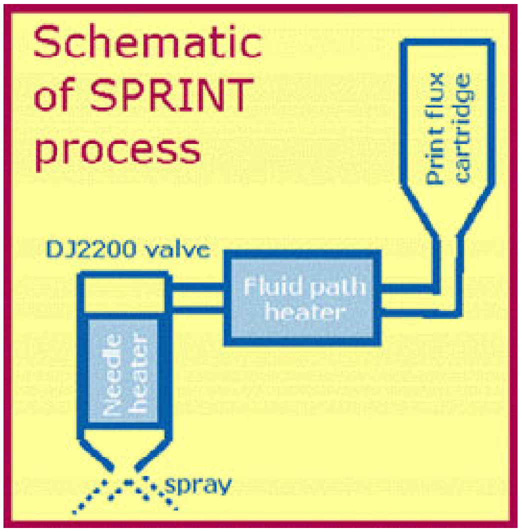

Figure 6: Schematic of "SPRINT" (spraying the print flux) process

Results and Discussions

To overcome the challenges of integrating Pb-free, flip-chip packaging with 45nm silicon, significant work was carried out from design, materials, processing, and metrology perspectives. Based on over five years of research experience on Pb-free materials, Intel selected *Sn-Ag-Cu* solder metallurgy as the flip-chip die attachment material. This material has showed significant improvement in solder-joint quality compared to the other more commonly used Pb-free alloys in our case.

Enabling the SPRINT process to high-volume manufacturing involved solving several manufacturability issues specific to ease and repeatability of tool maintenance.

The SPRINT process has met yield and reliability goals both during the development of Pb-free packages and during high-volume manufacturing ramp in Intel factories. At the end of the development cycle, the SPRINT process is at 99.5+% in three different Intel sites, and the samples used during the development phase show no die misalignment.

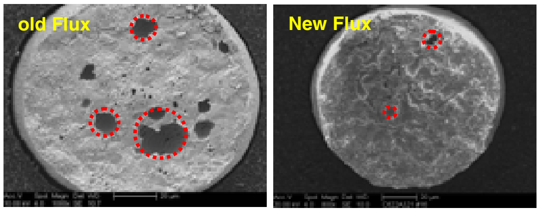

Figure 7: Comparison of interfacial defects between old and new fluxes: new flux is significantly better

Figures 7, 8, and 9 show the comparison of FLI joint interfacial defects, solder voiding, and electromigration performance between the new flux and previous-generation fluxes. The new flux provides significantly better performance in all three attributes. Figure 10 shows the comparison between leaded (65nm process technology) and Pb-free electromigration performance with optimized materials/process.

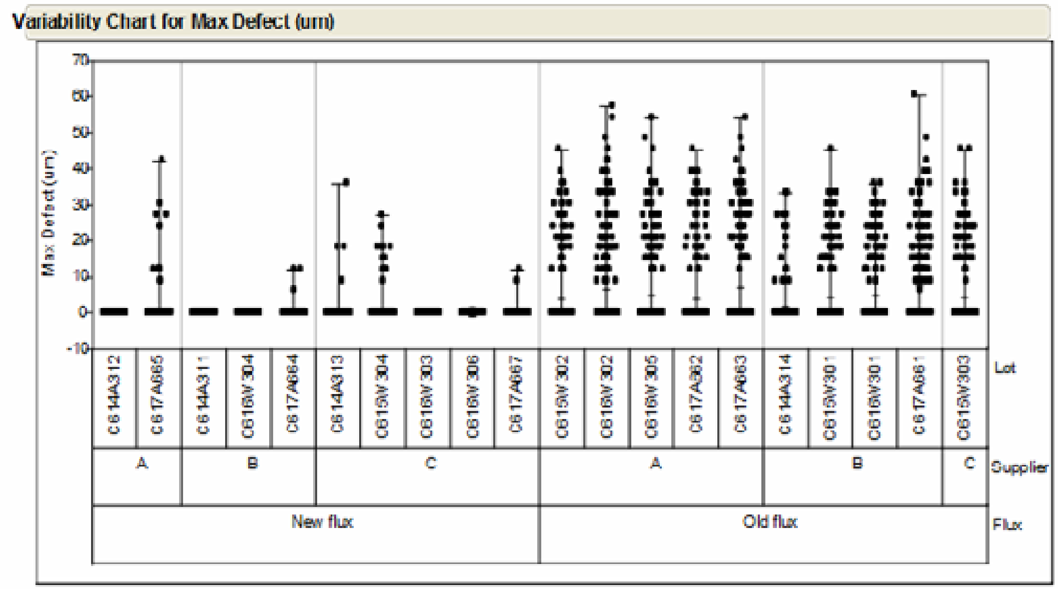

Figure 8: Comparison of FLI solder voids between new (left) and old (right) fluxes: new flux is significantly better

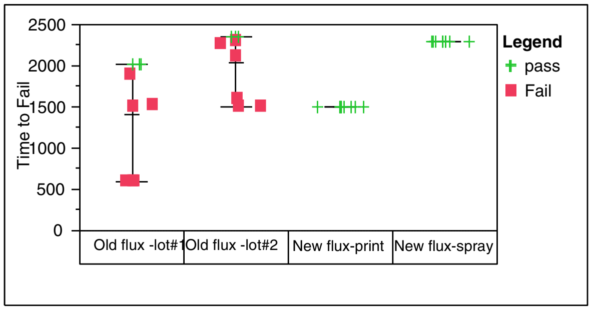

Figure 9: Comparison of electromigration performance between old flux, new flux (print formulation) and new flux (spray formulation): new flux is significantly better

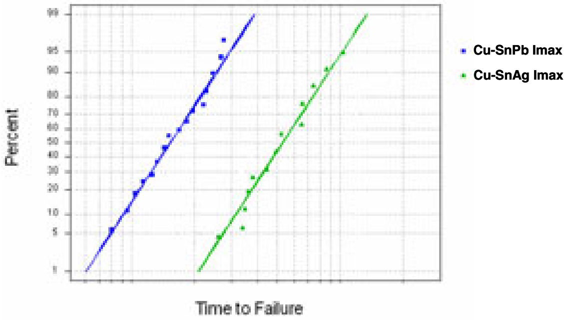

Figure 10: Comparison of bump electromigration performance of *Cu-Sn/Pb* and 100% *Pb-free* FLI

Figure 11 shows C-mode scanning acoustic microscope (CSAM) images of product units (complete stack-up). Cracking or interface delamination in the ILD or TM9 stack will show up as white or black spots apart form the contrast variation of the underlying pattern. The image on the left was taken after packaging: no contrast areas are observed, showing that the unit is free of cracking and/or interface delamination. These results have been reproduced in high volume, at process extremes, and have been proven to have significant margin through execution of well-designed hammer tests that impart significantly higher stress on the die than typically observed in manufacturing. The image on the right shows that the parts are clean of any issues even after reliability stresses.

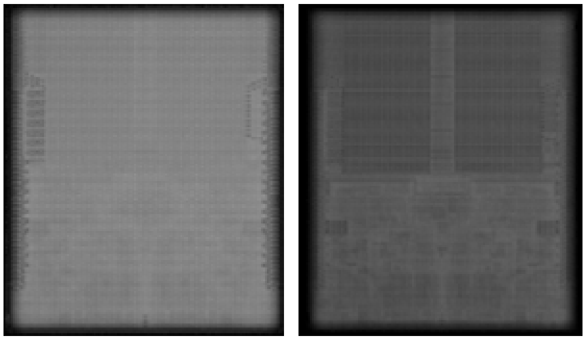

Figure 11: C-SAM units of production units: image on the left represents a unit post packaging and the image on the right is a unit post 25 hrs of HAST

These results indicate that the 45nm technology FLI architecture meets the stringent quality and reliability criteria despite the higher stress induced by Pb-free solders. Intel's FLI architecture with *Cu*-bumps is very unique and provides significantly better electromigration performance and power distribution performance than typical 100% solder-based FLI interconnects, as shown in Figure 12.

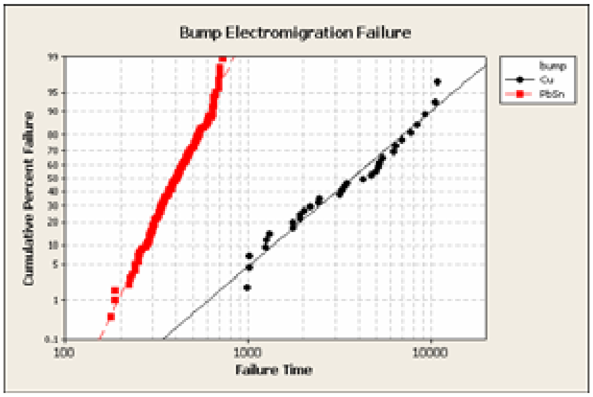

Figure 12: Comparison of bump electromigration performance of high *Pb*-bumps and Pb-free FLI

Sn-Ag-Cu solders have better wettability to metal pads, leading to reduced solder voiding, bumping, and assembly solder joint open yield loss. They also possess increased solder joint strength due to the suppression of under-bump nickel barrier layer diffusion and intermetallic growth. SAC solders also possess enhanced electromigration resistance arising from the synergistic reactions of reduced metal diffusion and interfacial defects.

As discussed earlier, the loss of solder joint collapse margins with the advent of Pb-free materials requires more stringent solder bump dimensional control. To achieve this control, solder bumping, flux material, and the reflow process were improved. The substrate C4 solder bump metrology was also modified significantly to screen out bump-level defects at high through-put speeds. Additionally, substrate packaging materials and design were also optimized to accommodate the higher reflow temperature of Pb-free solder to mitigate the associated reliability issues.

FORM FACTOR MANAGEMENT

Development of small form-factor packaging technologies required significant engineering effort in addition to the challenges involved with the integration of Pb-free, 45nm silicon technology. Key technical challenges include package size reduction in XY dimension and a reduction in the thickness of the package itself, by reducing die thickness and substrate thickness. Thin die challenges include the thinning process, stress-induced electrical property changes, and package warpage concerns. In addition, wafer thinning would require ensuring relief of residual stresses caused by the thinning process and protecting the die from chipping and cracking during wafer thinning and die singulation. Handling of the significantly warped thin wafer and die is another key challenge. A thin package with thin die is prone to warpage due to its low stiffness. Decreases in die thickness can make this problem worse, impacting the board assembly yield. Making the problem even more challenging is the need for a more coplanar BGA ball field to enable board assembly with finer BGA pitch. Solutions for these challenges required significant innovation and re-engineering in packaging material and process technologies. The approach, along with a few of the examples, is discussed below.

PACKAGE SIZE REDUCTION IN XY

The top surface of a flip-chip package contains the silicon die attached to the organic substrate and is underfilled with an epoxy material. The underfill material's primary function is to protect the flip-chip solder joints from failing due to stresses induced by the CTE mismatch between the die and the package during processing and use. The underfill material can occupy a significant area on the package as shown in Figure 13.

Figure 13: Example of underfill spread on a flip-chip CPU package

One of the key factors that controls the underfill spread on the package are the flow characteristics of the underfill material. Underfill flow under the die is driven by capillary flow. A line of underfill material is dispensed next to the die at high temperature, and capillary pressure in the material pulls the material under the die. In order to minimize the underfill spread away from the die, it is critical to increase the flow speed of the underfill material under the die, as schematically illustrated in Figure 14.

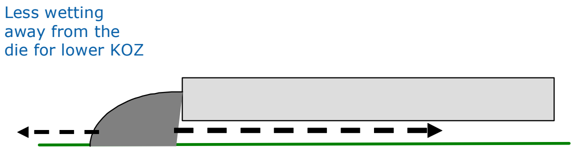

Figure 14: Competing forces for underfill spread under the die vs. away from die

In an idealized case, underfill flow can be modeled as flow between parallel plates [6], where the time to fill for an underfill between parallel plates can be calculated using this equation:

$$\text{Flow Time} = \frac{3\mu L^2}{h\gamma\cos\theta}$$

where γ is the surface tension of the underfill material, μ is the viscosity of the material, h is the gap between the plates, θ is the angle of wetting between the underfill and two surfaces, and L is the flow distance. Based on this elementary flow model, minimizing the μ/γ ratio can improve the flow speed of the underfill material.

Results and Discussion

A series of formulations with surface tension of the underfill material varying from ~20 dynes/cm^2 to 40 dynes/cm^2 at 110°C, and viscosities varying from 0.5 poise to 1.6 poise, were tested in a simple parallel plate flow experiment. Figure 15 shows the time to flow versus distance results for the formulations tested.

Based on the data from this simple flow test, it was observed that over a distance of ~15mm, significant reduction in flow time could be observed. These formulations were then tested on a package, leading to significant improvement on the flow speed of the material and therefore a reduction in the underfill spread on the package as shown in Figure 16.

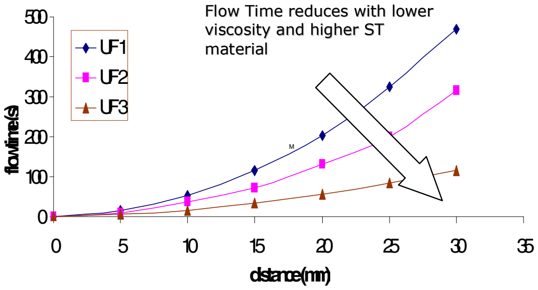

Figure 15: Flow time vs. distance for various underfill materials

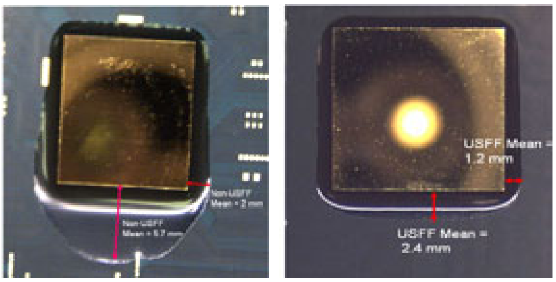

Figure 16: Underfill epoxy spread on the die with normal UF and optimized UF

The underfill material is a highly engineered epoxy-silica composite material with optimum thermo-mechanical properties (*Tg*, CTE, Modulus, etc.) to minimize stress transfer to die, and to prevent bump fatigue and die-cracking. In addition, the underfill material is also designed for toughness and adhesion to various interfaces (solder resist on substrate, passivation on die, *Cu*-bump, FLI solder, and silicon) under Pb-free, reflow conditions. These requirements lead to a very specific choice of epoxy resin chemistries that can be used in underfill material development. Adding the challenge of improved flow with higher μ/γ ratio required careful study of the surface tension/viscosity of each of the resin components in the material and to the selection of the right combination of components in order to provide good flow, and yet not compromise the reliability of the underfill. As shown in Figure 16, optimization of the μ/γ ratio of the underfill is very influential in minimizing the underfill spread on the package. However, it is also critical to note that there is a limit to how much the underfill viscosity can be reduced and to how much the surface tension of the underfill can be increased beyond which other effects take over. These can lead to increased spread of the underfill on the sides (due to very low viscosity of the material) and de-wetting of the underfill from the substrate, due to too high a surface tension of the material. Using this approach, new underfill formulations have been developed and deployed in high volume for enabling small form-factor, flip-chip packages. Utilization of this technology in combination with other novel process and design optimization approaches have led to significant reduction (up to 60%) in the package size for small, form-factor packages.

Z-HEIGHT REDUCTION

Industry benchmark trends indicate that overall package height in high-end smart phones are typically less than 1mm. While most of these packages to date are wirebonded and overmolded, there is an increased need to develop high *I/O* flip-chip packages that have *z*-heights of less than 1mm. In order to achieve significant package height reduction we discuss die thinning and the use of thinner/coreless substrates.

Results and Discussion

The typical thickness of a 12 inch wafer is ~750–800um. Since the active silicon needed for functioning of the device is less than 20-30um, a significant reduction in *z* height can be achieved by die thinning. Wafer backgrinding is common for devices used in stacked die, wirebond packaging technology, where die thinning down to 50-75um is routinely employed in high-volume manufacturing. However, die thinning of a high-density bumped flip-chip die is a significant challenge. Figure 17 shows the SEM image of a bumped wafer with *Cu*-bumps with the bump height nominally ~50 um.

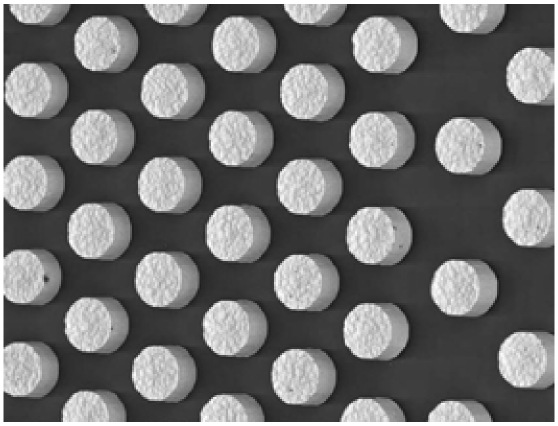

Figure 17: SEM image of a Cu bumped wafer

In order for the backgrinding process to work effectively, it is critical for the backgrinding tape to completely encapsulate the bumped wafer without any voids. This is essential since the presence of voids or the inability of the tape to completely encapsulate the bumps can lead to cracking of the wafer or non-uniform backgrinding. In addition to the encapsulation, it is also critical that the tape be removed without leaving any residue or damaging the *Cu*-bump/BLM during the tape peel step. In order to achieve this critical balance of lamination, uniform backgrinding and clean removal post backgrinding, a multi-layer adhesive, UV, curable tape with a soft backing layer was developed. The backgrind tape is laminated to the wafer, and the hardness of the multilayer adhesive layer contacting the wafer surface is well controlled to allow complete encapsulation of the bumps. After the backgrinding process, the tape is exposed to UV cure, leading to cross-linking and hardening of the multi-layer adhesive. This allows for easy detaping of the tape from the backgrinded wafer, since the harder *x*-linked adhesive can easily delaminate from the wafer/bump surface. Using this technology, Intel has been able to develop a high-volume manufacturing process for wafer thinning 12-inch, high-density bumped wafers down to 75um.

In addition to wafer thinning, the other element that can enable further z height reduction is minimizing the substrate thickness. In the case of the organic substrate, a standard build-up core of ~800um is used for typical packages. This core thickness in the substrate is typically selected in order to balance the electrical requirements of the package and its ability to go through the assembly line and SMT processing. In order to decrease the overall thickness of the package, one of the approaches is to reduce the thickness of the core layer in the package. Depending on the need for the overall package thickness, either die thinning or substrate thinning, or both, can be employed to produce the overall desirable thickness. With the combination of die thinning and substrate thinning, Intel now has the capability to produce flip-chip packages with package heights that are 33% less than standard packages (Figure 18).

Figure 18: Comparison of a standard package z-height with a thin core-thin die package

Board Level Interconnect

Intel's 45nm technology is useful for a wide variety of products from servers to mobile devices. In order to meet the size requirements of ultra mobile personal computers and mobile Internet devices, the 45nm packaging technology had to scale the physical size of the packages to meet the demands of the ultra mobile products.

Scaling down the size of these packages while maintaining the product functionality of Intel Architecture requires the board-level interconnect to scale as well. In the case of the Intel Atom processor, the ball pitch scaled down to 0.6mm from a 0.8 to 1.27mm pitch for PCs. This scaling creates two key challenges: routing the signals on the board and ensuring a robust solder joint.

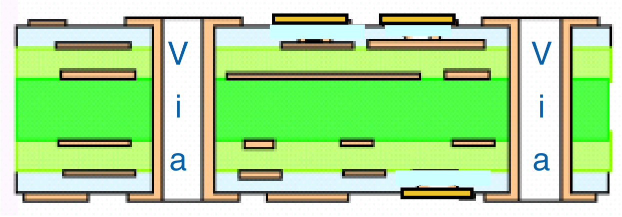

Figure 19: Cross section of a Type 3 motherboard

Traditional PCs utilize a Type 3 motherboard that is characterized by mechanically drilled vias as shown in Figure 19. In mobile stripline routing, the signals that come out of the package have to travel through these vias on their way out of the package. Unfortunately, these mechanically drilled vias do not scale well and limit the package ball pitch to approximately 0.8mm. The routing issue is solved by using High Density Interconnect (HDI) motherboards shown in Figure 20. HDI boards contain one or more layers that are connected to other layers through microvias. As the name implies, the laser drilled microvias are significantly smaller than the mechanically drilled vias and allow the signals to break out from the package.

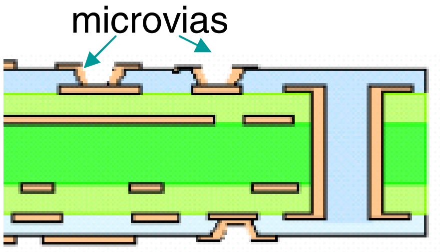

Figure 20: Cross section of an HDI motherboard

Solder joint reliability is the other board-level challenge with SFF packages. By the very nature of their use, mobile products are subject to drops. The smaller solder joints of SFF packages have less mass to handle these mechanical stresses. Gluing the corners of the packages provides the additional strength and mechanical margin for the mobile drop condition as shown in Figure 21.

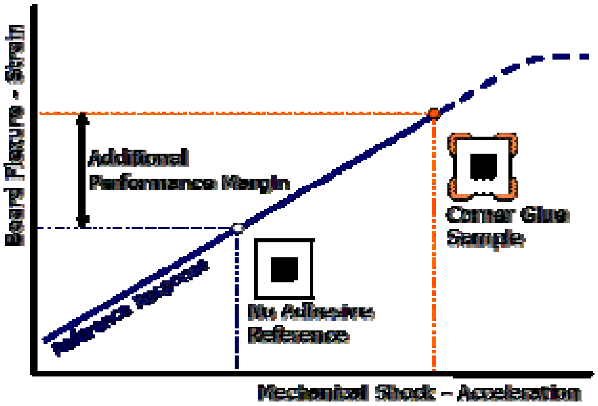

Figure 21: Corner glue provides mechanical margin for mobile drop condition

CONCLUSION

A series of iterative optimizations of design, fab, assembly materials, and process led to a high-yielding, 100% Pb-free, 45nm packaging process. The on-time and on-target delivery of this technology led to Intel’s continued one-generation-ahead lead in the 45nm product, underlining Intel’s assurance that it will develop a new process technology with enhanced microarchitecture or an entirely new microarchitecture every year. The elimination of lead in this technology also makes Intel the leader in achieving environmentally green products

In this paper we shared some of the key challenges associated with the development of a high-volume manufacturing compatible assembly process for packaging Intel’s 45nm, completely Pb-free devices. Key technical challenges were addressed through development of novel FLI solders, fluxing material, and process solutions. In addition, stress transfer to silicon and its impact to low-k ILD integrity were reduced, by the use of novel interconnect designs. Small form-factor packaging challenges were overcome by a series of innovative materials and process changes to achieve a reduction in form factor while meeting the technology reliability goals. This enables Intel’s continuing leadership in thin and light notebooks and smart phone devices.

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