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Intel's 45nm CMOS Technology

Managing Process Variation in Intel's 45nm CMOS Technology

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ABSTRACT

The key message of this paper is that process variation is not an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome. This message is illustrated with data from the 45nm process generation where process variation is shown to be at least equivalent to (and in many cases better than) process variation in the 65nm- and 90nm-process generations.

We begin this paper with an introduction and historical overview of process variation. Although there has been a trend in recent years to convey process variation as a new challenge associated with advanced CMOS technologies, process variation has been a continuing theme throughout the history of semiconductor process engineering.

We continue with a review of critical sources of variation specific to the 45nm generation, including highly random effects (random dopant fluctuation, line-edge and line-width roughness), variation associated with the gate dielectric (oxide thickness, fixed charge, defects and traps), patterning proximity effects (classical, and those based on optical proximity correction (OPC)), variation associated with polish (shallow-trench isolation, gate, and interconnect), variation associated with strain (wafer-level biaxial, high-stress capping layers, and embedded silicon-germanium (SiGe)), and variation associated with implants and anneals (implant tool-based, implant profile, rapid-thermal anneal, and implant variation associated with poly-grain boundaries).

We then explore the variety of process, design, and layout techniques used in the 45nm generation to mitigate the impact of variation. Pure process mitigation techniques include targeting key transistor properties to reduce random dopant fluctuation, reducing traps at the high- k metal-gate (HiK+MG) interface to reduce random charge variation, improving patterning techniques to reduce line-edge roughness and endcap variation, and improving polishing technologies to reduce systematic cross-wafer variation. Combination design-process techniques include optimizing topology, using OPC to reduce random and systematic variation, and adding dummy features to reduce systematic variation. Pure design techniques include chopping techniques to compensate for random variation and common-centroid layout techniques to compensate for systematic variation.

We move on to illustrate the success of these mitigation techniques by reviewing detailed data characterizing variation in the 45nm generation. Three different types of measurements are presented to illustrate various variation mechanisms. The first is in-fab measurement of variation, used to characterize gate dimensional variation for the 45nm versus 65nm and 90nm generations. The second is low-frequency electrical measurement of matched transistor pairs, used to extract random variation for 45nm versus 65nm transistors. The third is measurements of product ring oscillators, used to determine both systematic and random within-wafer and within-die variation for 45nm versus 65nm products.

Finally, we reinforce the key message that variation does not pose an insurmountable barrier to Moore's law, but is simply another challenge to be overcome.

INTRODUCTION AND HISTORICAL OVERVIEW

Moore's-Law-driven technology scaling has improved VLSI performance by five orders of magnitude in the last four decades. As advanced technologies continue the pursuit of Moore's Law, a variety of challenges will need to be overcome. One of these challenges is management of process variation [1, 2].

Although there has been a trend in the CMOS literature in recent years to convey process variation as a new challenge associated with advanced CMOS technologies, that viewpoint does not effectively capture the history of process variation. Process variation has always been a critical aspect of semiconductor fabrication.

The first discussion of random variation in semiconductor devices was Shockley's 1961 analysis of random fluctuations in junction breakdown [3]. Shockley's concepts of random variation were extended to MOS devices by Keyes [4] in 1975 when he modeled the effect of random fluctuations in the number of impurity atoms in the depletion layer of a field-effect transistor (FET). Systematic variation in MOS devices was first addressed formally in 1974 by Schemmert and Zimmer [5] when they computed the sensitivity of ion-implanted MOS threshold voltages as a function of the implantation energy and the oxide thickness. A more extensive analysis of threshold voltage sensitivity using a closed-form numerical simulation was presented by Yokoyama et al. in 1980 [6] with a Monte Carlo approach developed by Alvarez in the same year [7]. Interconnect variation has also received significant attention over the years, with Lin et al. presenting a detailed treatment in 1998 [8] that was expanded by many authors in the early 2000s [37, 40–43].

While the continued decrease in the ratio of feature sizes to fundamental dimensions (such as atomic dimensions and light wavelengths) means that management of variation will play a significant role in future technology scaling, the evidence shows that process variation has been a continuing theme throughout semiconductor history.

CRITICAL SOURCES OF VARIATION IN THE 45NM GENERATION

45nm technology is subject to a number of variation effects that are well documented in the literature [9–63]. Examples include highly random effects (random dopant fluctuation (RDF) [9–17], line-edge and line-width roughness, line-edge and line-width roughness (LER) and

(LWR), respectively [18–21]), variations in the gate dielectric (oxide thickness variations [22–26], fixed charge [27], and defects and traps [28–34]), patterning proximity effects (classical, and those associated with OPC [35]), variation associated with polish (shallow trench isolation (STI) [36, 40], gate [37–38], and interconnect [39,42-44]), variation associated with strain (wafer-level biaxial 46–49, 57), high-stress capping layers [50–52], and embedded silicon-germanium (SiGe) [53–56]), and variation associated with implants and anneals (tool-based [58], pocket implants [59–60], rapid-thermal anneal RTA [61] and variation associated with poly grains [62–63]).

Random Dopant Fluctuation (RDF)

MOS threshold voltage variation due to random fluctuations in the number and location of dopant atoms is an increasingly significant effect in sub-micron CMOS technologies (see Figure 1 and [9–17]). As the number of dopant atoms in the channel decreases with scaled dimensions, the impact of the variation associated with the atoms increases. Figure 2 illustrates the decreasing average number of dopant atoms in the channel as a function of the technology node. Note the change from the 1 μ m technology node (with many thousands of dopant atoms in the channel) to the 32nm technology node (with less than 100 atoms in the channel).

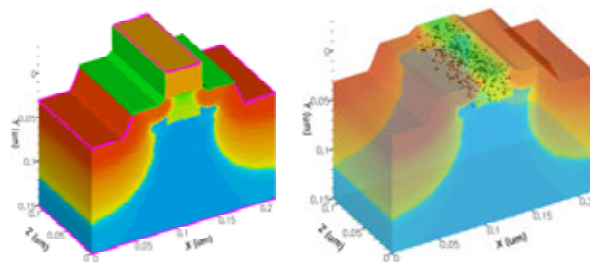


Figure 1: Random dopant fluctuations (RDF) are an important effect in sub-micron CMOS technologies

RDF is assumed to be the major contributor to device mismatch of identical adjacent devices and is frequently represented by Stolk's formulation (Equation 1)

$$\sigma V_{T_{ran}} = \left(\frac{\sqrt[4]{4q^3 \epsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\epsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{W_{eff} \cdot L_{eff}}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{W_{eff} \cdot L_{eff}}} \right) \quad (1)$$

illustrating that matching improves with decreases in channel doping (N) and gate oxide thickness (T_{ox}), and it degrades when device area decreases [12].

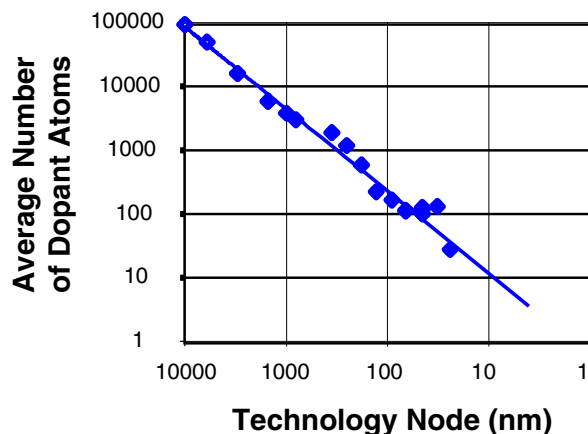


Figure 2: Average number of dopant atoms in the channel as a function of technology node

While Equation (1) assumes that the only contribution to random variation between two adjacent matched devices is random dopant fluctuation, in practice it is known that additional effects also contribute to the measured variation [14]. Identifying the magnitude and root cause for these additional effects is important in facilitating the development of mitigation techniques. Many groups have attempted to estimate the size of these additional effects by comparing measured data to simulation [15–16]. As an example, we reported the results of such a study [17] where we compared simulation results to 65nm silicon data and showed that simulated RDF is ~65% of the total NMOS σV_T . Similar results were obtained when we compared 45nm simulation results to data where the simulated RDF is ~60% of the total PMOS σV_T .

Line-edge and Line-width Roughness (LER and LWR)

While random fluctuations in patterned lines occur in both the front-end and the back-end of the process, the primary concern with LER/LWR is variations in poly-gate patterning (see Figures 3 and 4). For poly-gate patterning, LER and LWR are associated with increases in the sub-threshold current [18, 19] as well as degradation in the threshold voltage (V_T) characteristics [20, 21].

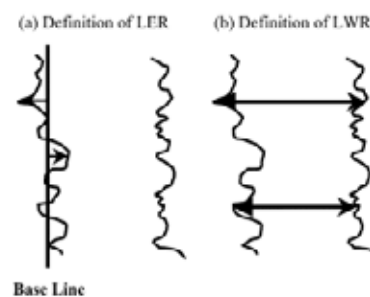


Figure 3: LER/LWR definitions [19]

Diaz et al. [18] quantified the impact of LER on transistor performance by comparing devices from a 130nm technology (80nm nominal gate lengths and 17Å oxide) that were patterned with a 193nm binary solution (9.3nm LER) and 248nm alternating phase shift mask (APSM) solution (6.5nm LER). LER reduction from 9.3nm to 6.5nm translated into measured improvement of 1.5X for a nominal device. For the subnominal 70nm device, a 2X improvement was observed.

In a similar experiment, Kim et al. [19] evaluated the impact of LER and LWR on device performance using a set of 80nm node single nMOS transistors from low-power SRAM devices fabricated with various combinations of gate length, gate width, LWR, and LER. The amount of LER and LWR was controlled by applying different resist materials, defocus, and overetch time. Their experimental data showed that LER effects began when the gate length was less than 85nm. They observed a four-order of magnitude increase in the standard deviation of the subthreshold current for the smallest gate lengths in the study.

Fukutome et al. [20] were able to use scanning tunneling microscopy (STM) to directly assess the impact of LER on the carrier profiles of source-drain extensions in sub-micron MOSFETs. They observed that the roughness of extension edges induced by gate LER depended on the implanted dose, halos (pockets), and various co-implantations. They showed an improvement of 4nm in V_T roll-off with a decrease in the average LER, and they confirmed that co-implants induced a degradation of 5mV in the standard deviation of V_T .

Asenov et al. [21] studied the combined effect of LER and random discrete dopants on current fluctuations. They were able to demonstrate that the two sources of fluctuations act in a statistically independent manner when taken into account simultaneously in the simulations. They also showed that the LER-induced current fluctuations have a much stronger channel length dependence and, as devices are scaled to shorter dimensions, LER is expected to supplant RDFs as the dominant variation source.

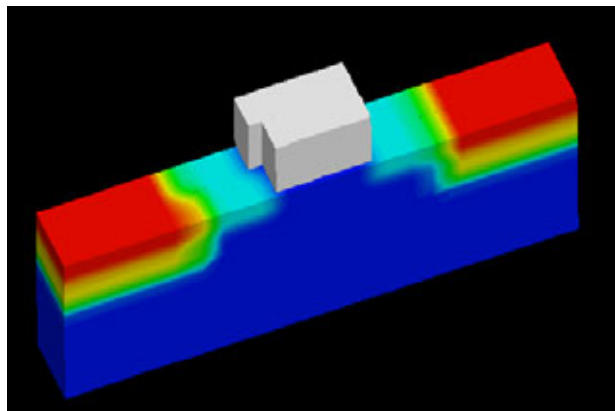


Figure 4: LER/LWR of poly gates has been modeled by a number of researchers [18–21]

Variations in the Gate Dielectric

The high- k metal-gate (HiK+MG) devices used in the 45nm generation are subject to a number of variation effects in the gate dielectric [22–34]. These include variations in oxide thickness, fixed charge, and interface traps. These physical changes in the dielectric result in parametric variations in drive current, gate tunneling current, or threshold voltage.

Oxide Thickness

Asenov et al. [22] have studied the intrinsic threshold voltage fluctuations introduced in the atomic scale roughness of the gate interfaces in deep submicrometer MOSFETs through carefully designed simulation experiments. Their simulations show that intrinsic threshold voltage fluctuations induced by local oxide thickness variations become comparable to voltage fluctuations introduced by RDF for conventional MOS devices with dimensions 30nm and below.

Koh et al. [26] have evaluated gate-tunneling leakage current both experimentally and theoretically for MOSFETs with 1.2- to 2.8nm-thick conventional SiO₂ gate oxides. They showed that the statistical distribution of gate-tunnel leakage current causes significant fluctuations in V_T when the gate oxide tunnel resistance becomes comparable to the gate poly-Si resistance. They set the scaling limits (when using a low-resistive silicide gate, and with a conventional gate oxide) at an 0.8nm gate oxide thickness.

Fixed Charge

The presence of fixed charge in the high- k layer can affect the mobility and the threshold voltage. As a consequence, variation in the fixed charge may affect the uniformity of the threshold voltages on devices. Kaushik et al. [27] have studied this effect and estimated the fixed charge in high- k dielectric films based on a slant-etched SiO₂ layer that allows a thickness series on a single wafer.

Defects and Traps

Electron mobility degradation and V_T instability due to fast transient charging (FTC) in electron traps is a continuing concern in high- k dielectrics.

Lucovsky [28] has extensively investigated defects in HfO₂ gate dielectrics through the combination of spectroscopic measurements with electrical detection of defect states. Two types of defects have been proposed, those associated with grain boundaries in the nanocrystalline HfO₂ and those associated with different charge states of the O-atom vacancy. Similar conclusions are reached by other researchers [29–31].

Wen et al. [32] have investigated the effects of FTC by studying the impact of metal gate electrodes on mobility degradation. Their studies suggest that the increase of FTC in HfSi_x may be attributed to higher density of the O vacancies in the high- k dielectric caused by the HfSi_x-induced O scavenging process.

Optimization of HfO₂ processing such as N incorporation [33] or use of HfSiO_xN_y [34] has also been shown to reduce the charge-trapping effects.

Patterning Proximity Effects

The general lithography expression for the minimum resolvable critical dimension (CD)—assumes equal line/space—is given in Equation (2),

$$CD_{\min} = k_1 \frac{\lambda}{NA} \quad (2)$$

where k_1 is a measure of lithographic aggressiveness (small is aggressive) and includes illumination conditions, resist materials/chemistry, OPC and other resolution enhancement techniques (RETs). The continued decrease in k_1 for more advanced technologies is illustrated in Figure 5.

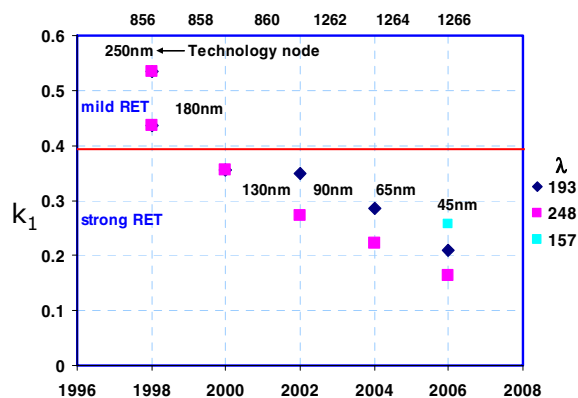


Figure 5: Generational trend in k_1

A variety of techniques can be applied to layers with low k_f to improve the lithographic patterning and reduce the variation. One of the most powerful of these is OPC [35].

OPC pre-distorts the mask data following specific algorithms in order to achieve a desired pattern on the wafer. OPC is based on a highly phenomenological process model that incorporates lumped optics, resist, wafer stack, and mask effects. This model generates a mask-to-wafer optical transfer function, and an OPC algorithm is written to invert the transfer function. An OPC recipe is developed using an iterative algorithm that modifies the starting database in order to achieve the desired pattern on the mask. An example of the power of OPC is shown in Figure 6, which compares patterning with and without OPC applied.

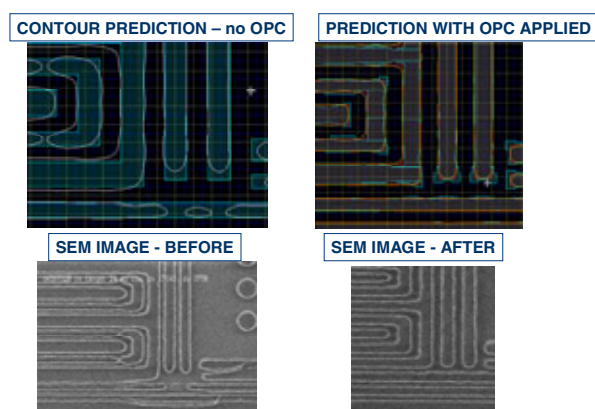


Figure 6: OPC pre-distorts the mask data in order to achieve a desired pattern on the wafer

Polish

Chemical mechanical polish (CMP) is a critical process step in advanced semiconductor technologies. In the front end, CMP has been used for polishing STI [36], and more recently for polishing gate-in, gate-last, metal gate processes [37]. In the back-end, CMP is used for polishing dielectrics in a conventional process and metals in a damascene process [37].

In a traditional STI process [36], shallow trenches are etched into silicon using a nitride hard mask followed by oxide deposition to fill the trenches. A CMP step removes the excess oxide on top of the nitride and partially polishes the nitride layer. The remaining nitride is stripped to expose the active regions where subsequent processing forms the transistors. Subsequent process steps (poly patterning, spacer, silicide formation, etc.) are sensitive to variations in the height of the oxide “steps” between the edge of the STI and diffusion produced by CMP variation.

In a high- k , first gate-last process [37], SiO_2 growth is replaced by high- k gate dielectric formation. After interlayer dielectric ILD deposition, a poly polish step

exposes poly gates, and a gate trench is formed by removal of the dummy poly. Workfunction and conduction metals are deposited in the gate trench and then planarized using a metal polish step. The gate-fill step is sensitive to variable height gates produced by the poly gate CMP variation, and subsequent process steps are sensitive to both height and recess variation from the combination of poly-gate and metal-gate CMP variation [38].

In the back-end [39] the traditional subtractive process uses a metal etch to pattern and remove titanium and aluminum. The subtractive metal process is followed by ILD, a CMP planarization step, and tungsten via fabrication step. In the subtractive process, the sensitivity is to ILD variation produced by the dielectric CMP planarization. Damascene-copper reverses the process, by etching troughs and vias into an insulator, depositing a copper diffusion barrier and copper into the troughs, and using CMP to remove excess copper and barrier material. An ILD is added after the Cu-CMP. In the damascene process, the sensitivity is to Cu and ILD variation produced by the metal CMP planarization.

One commonly applied method for improvement of variation in any CMP process is the addition of dummy-features. Tian et al. [40] review some of the historical approaches to dummy-feature placement and modeling and present a time-dependent relation between post-CMP topography and layout pattern density for CMP in STI.

In the back end, much recent literature has been devoted to the topic of modeling interconnect variation produced by CMP. For example, Yu et al. [41] characterize the smoothing and planarization effects of ILD polishing by a polynomial equation with a small number of fitted parameters. Choi et al. [42] combine a set of scripts and commercial tools to incorporate Cu-interconnect CMP effects in a full-chip static timing analysis. Soumyanath et al. [43] present a nonintrusive time-domain technique to characterize interconnect performance on a 0.25 μm , 1.8V process. The technique is based on simple time-delay measurements from a repetitive waveform. Finally, Mehrotra et al. [44] analyze interconnect timing performance in a high-speed microprocessor by using timing analysis in conjunction with a post-extraction net adjustment.

Strain

Prior to the 130nm process generation, classic “Dennard” transistor scaling [45] was sufficient to support the 0.7X delay reduction per generation required by Moore’s Law. For the 90nm generation and beyond, additional enhancements have been required. Primary among these enhancements is the use of strain.

During the 1980s, researchers began to explore channel strain approaches for transistor enhancement where thin Si layers were grown on relaxed SiGe substrates such that the thin Si layer would take the larger lattice constant of the SiGe and create biaxial tensile stress in the channel [46–49].

In the early 2000s, a new class of transistor strain approaches was developed that used process features external to the transistor (rather than strain in the channel itself as with the biaxial approaches) to strain the transistor. Among these approaches were high-stress capping layers [50–52] and the use of embedded SiGe in the PMOS source-drain regions [53–56].

Process strain creates a number of new variation challenges, both random and systematic. Researchers are beginning to focus both theoretically and experimentally on quantifying the magnitude of strain-induced variation. In Tsang et al. [57] for example, an analytical model was developed to predict threshold variation as a function of Ge fraction, layer thickness, channel length, and doping profile. This model was verified with simulations and experimental data for n- and p-MOSFETs in both single- and dual-channel architectures.

Implant and Anneal

In addition to the fundamental variation mechanism of random dopant fluctuation (discussed earlier), there are also a number of variation sources associated with the physical implant and anneal processes.

The implant tool conditions are a significant source of transistor variation. Al-Bayati et al. [58] have studied the device sensitivity of ultra-shallow junction processes to tool-related implant and annealing parameters. In their work, NMOS and PMOS devices were studied to quantify variation as a function of the accuracy of dose, purity of dose, spike anneal peak temperature, and the ramp-up and cool-down rates.

The architecture of the pocket (halo) and extension (tip) implants is also critical for variation management. Tanaka et al. [59–60] have investigated the statistical V_T distribution for a variety of pocket (halo) implantation conditions through both experimental measurements and device simulation. They showed that the increase in V_T asymmetry caused by the pocket profile degrades the total fluctuation of V_T by greater than 15%.

The advent of advanced RTA processes has introduced new variation sources. Ahsan et al. [61] investigated the impact of RTA anneal on process variation and noted that most of the observed variation can be accounted for by lamp annealing-driven variations in R_{ext} and V_T . They also showed that the variation correlates with the calculated reflectivity for the lamp RTA spectrum and is dependent on the local, mm-scale pattern density.

An additional variation mechanism related to implant technology arises from the poly-crystalline nature of conventional gates. Enhanced diffusion, variations in dopant activation, and implant channeling along grain boundaries can all cause increased variation. Fukutome et al. [62] have investigated the effect of randomly oriented and rotated poly-Si gate grains on lateral carrier profiles of extension regions in sub-50nm MOSFETs by direct observations and electrical measurements. By optimizing the grain boundary they were able to demonstrate a 26% reduction in threshold voltage variation. Brown et al. [63] developed a coherent 3-D statistical simulation study of the impact of poly-Si granularity on the variability in CMOS transistors and concluded that for realistically scaled bulk MOSFETs, the poly-Si and random dopant-induced variations compete at 35nm and 25nm channel lengths. They further concluded that if LER does not scale by the International Technology Roadmap for Semiconductors (ITRS), fluctuation due to poly-grain boundaries becomes the dominant source of variability for channel lengths below ~25nm.

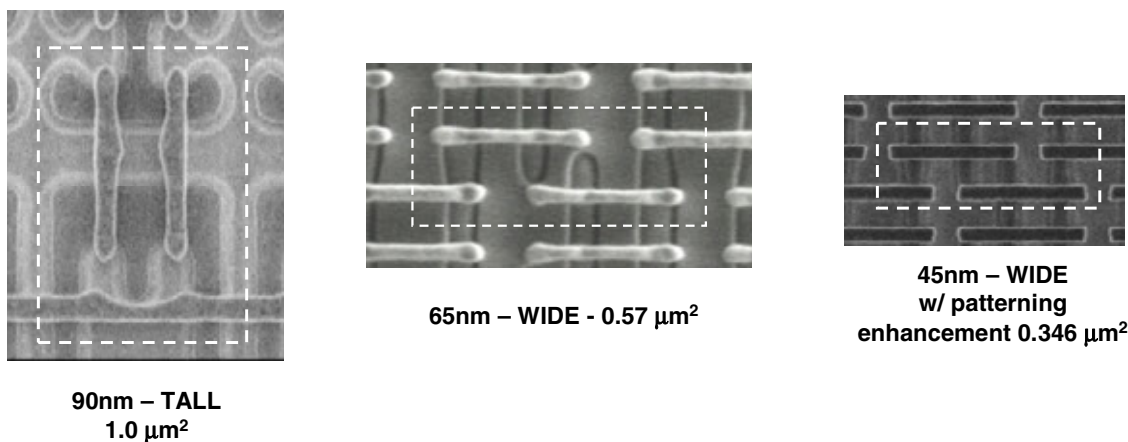


Figure 7: Cell topology enhancements for mismatch improvement

PROCESS, DESIGN AND LAYOUT TECHNIQUES USED IN THE 45NM GENERATION TO MITIGATE THE IMPACT OF VARIATION

Many techniques were applied in the 45nm generation to mitigate the impact of process variation. These techniques can be characterized as pure process techniques (i.e., techniques transparent to design), combination process-design techniques (i.e., techniques that exercise tight cooperation between process and design), and pure design techniques (i.e., techniques transparent to process). Examples of pure process mitigation techniques include targeting key transistor properties to reduce random dopant fluctuation, reducing traps at the HiK+MG interface to reduce random charge variation, improving patterning techniques to reduce LER and endcap variation, and improving polishing technologies to reduce systematic cross-wafer variation. Examples of combination design-process techniques include optimizing topology, using optical proximity correction to reduce random and systematic variation, and adding dummy features to reduce systematic variation. Pure design techniques include chopping and autozeroing to compensate for random variation and common-centroid layout to compensate for systematic variation.

Process Mitigation Techniques

Pure process mitigation techniques are techniques implemented by the process and transparent to design. As an example, recall that RDF is a major contributor to random variation and is frequently represented by Stolk’s formulation (Equation 2)

$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \epsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\epsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{W_{eff} \cdot L_{eff}}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{W_{eff} \cdot L_{eff}}} \right) \quad (2)$$

illustrating that matching improves with decreases in channel doping (*N*) and gate oxide thickness (*Tox*), and degrades when device area decreases [12].

Historical scaling (which reduces gate oxide thickness) suggests a continued improvement in the random variation coefficient (*C2*). However, as illustrated in Figure 8, the historical improvement trend in *C2* slowed when gate leakage concerns limited gate oxide scaling with conventional gate oxides at the 65nm generation. The introduction of 45nm HiK+MG, which restored historical gate oxide scaling due to reduction in gate oxide leakage, was a pure process technique that mitigated the impact of RDF and enabled a return to an historical scaling trend.

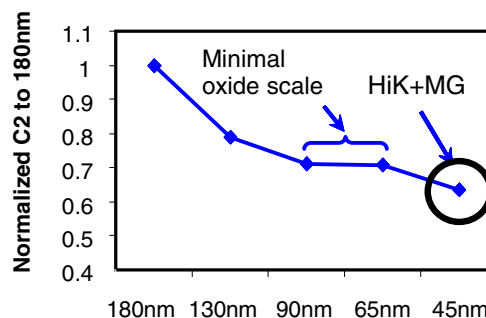


Figure 8: HiK+MG enables a return to an historical scaling trend with associated improvement in C2

Traps in the HiK+MG dielectric are another source of random variation. A number of process improvements were incorporated in the 45nm process to reduce the impact of traps. Figure 9 shows pulsed IV characteristics for early versions of the HiK process vs. a later improved version. Initial HiK+MG material showed a large hysteresis effect—as well as high-bias-temperature instability (BTI) degradation in direct-current (DC) stress. Later versions of the process (incorporating a variety of

improvements) showed negligible hysteresis demonstrating that traps were virtually eliminated.

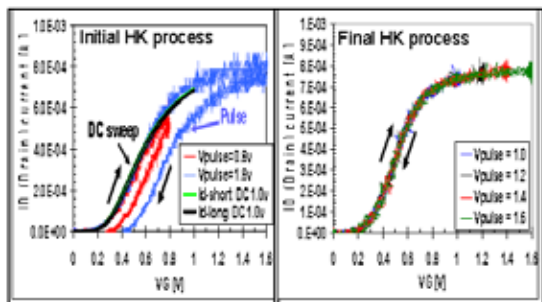


Figure 9: Dielectric trap improvement in the 45nm generation as measured with pulsed IV [64]

LER and LWR are key contributors to random variation in advanced technologies. A variety of advanced patterning techniques were applied in the 45nm generation to improve the patterning and reduce the LER (see Figure 10).

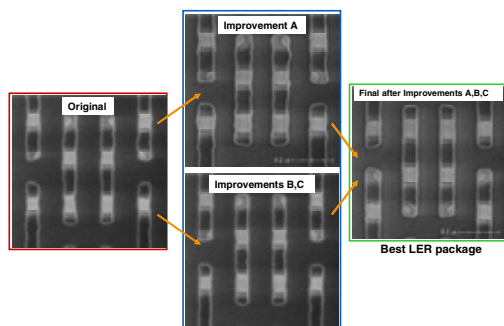


Figure 10: A variety of techniques were applied in the 45nm generation to improve the patterning and reduce the LER

Another lithographic variation improvement incorporated in the 45nm generation was to change the poly-patterning process so that the poly endcaps are square rather than rounded (see Figure 11 and 7). Square endcaps eliminate the systematic variation associated with “dogbone” and “icicle” endcaps.

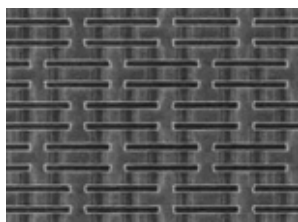


Figure 11: Square poly endcaps implemented in 45nm technology to eliminate the variation of “dogbone” and “icicle” endcaps

A number of modules in the 45nm generation were able to incorporate significant process improvements to reduce systematic variation. One of many examples is shown in Figure 12, which illustrates the improvement in 45nm MT1 within-wafer (WIW) resistance uniformity over the 65nm generation due to improvements in Cu CMP.

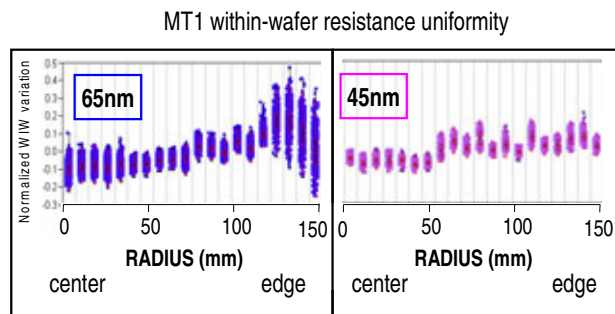


Figure 12: Improvement in 45nm MT1 within-wafer resistance uniformity due to improvements in Cu CMP

Combination Process—Design Mitigation Techniques

Combination process-design mitigation techniques are techniques that exercise tight cooperation between process and design. An example of a combination process-design mitigation strategy is to change the topology of the SRAM from a “tall” design to a “wide” design (see Figure 7 and Ref. [19]). The wide design improves CD control and variation by aligning the poly in a single direction, eliminating diffusion corners, and relaxing some patterning constraints on other critical layers.

Combination design-process improvements resulting from optimization between reticle enhancement techniques and the lithography process were widely used in the 45nm generation. An example is shown in Figure 13, which shows the improvement resulting from an OPC/RET update that resolved the issue of a poor resist profile causing variation in metal pattern after etch.

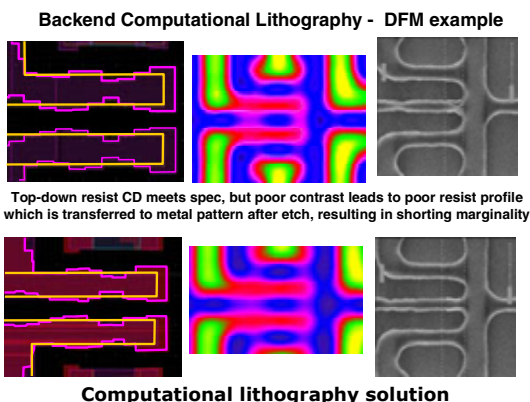


Figure 13: An example of a design-process OPC/RET update in the 45nm generation that resolved the issue of a poor resist profile causing variation in metal pattern after etch

Combination process-design strategies such as dummification and fill techniques at diffusion, poly, and in the back-end have been used historically to reduce systematic variation induced by the lithography, etch, and polish modules. The 45nm generation continued this improvement trend by extending the dummification and fill methodologies of past generations. Figure 14 illustrates this improvement by comparing poly dummification between 65nm and 45nm test vehicles.

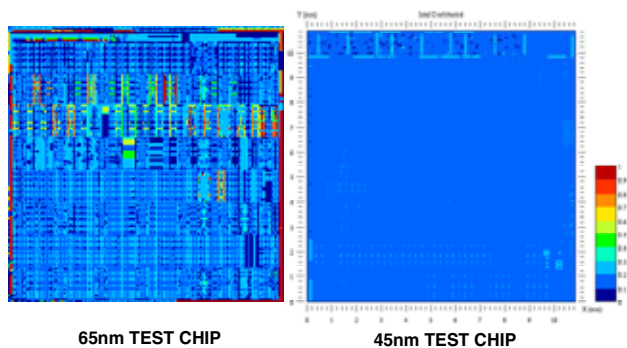


Figure 14: Poly dummification improvements between 65nm and 45nm generations as demonstrated on a test vehicle

Recent generations have seen the impact of non-uniformities at the poly layer extend beyond lithography, etch, and polish into modules such as RTA anneal [60]. Figure 15 shows an example of a combination design-process mitigation strategy where dummy features were incorporated to improve poly density and thus improve RTA temperature uniformity to reduce systematic transistor variation.

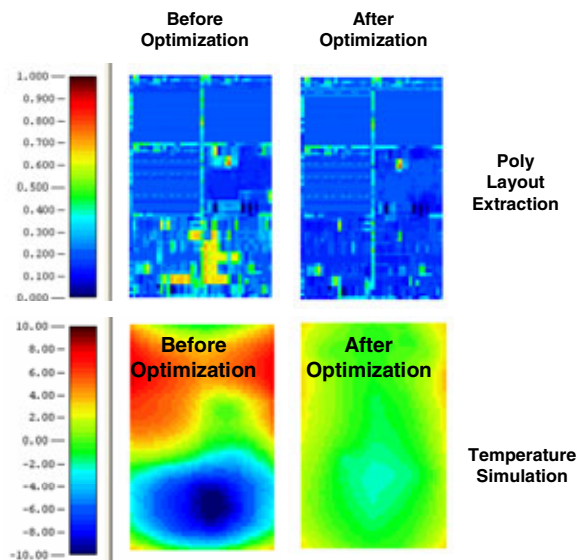


Figure 15: Dummy features were incorporated in 45nm generation to improve poly density and thus RTA temperature uniformity

Design Mitigation Techniques

Pure design mitigation techniques are techniques implemented by design and transparent to process. An example of a pure design mitigation technique used in the 45nm generation to reduce the impact of random variation is chopping, as shown in Figure 16. In chopping, the inputs to a differential amplifier are swapped, or chopped, under the control of a clock signal. The same clock signal is used to swap the outputs, and then the results are low-pass filtered.

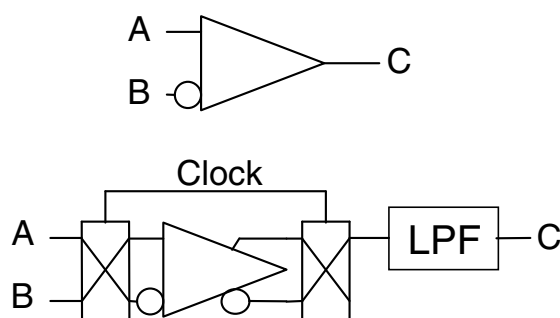


Figure 16: Chopping was used in the 45nm generation as a pure design technique to mitigate the impact of random variation

A more sophisticated design approach used in the 45nm generation to reduce the V_{ccmin} impact of mismatch due to random variation in the SRAM was the incorporation of dynamic forward body bias (FBB) as shown in Figure 17.

In this approach, the Nwell is partially discharged 1-cycle before the word-line by a programmable pulse. The Nwell then remains at lower bias during back-to-back access to minimize switching power. The SRAM PMOS FBB circuitry is integrated along the 8-column boundary and consumes less than 2% area overhead.

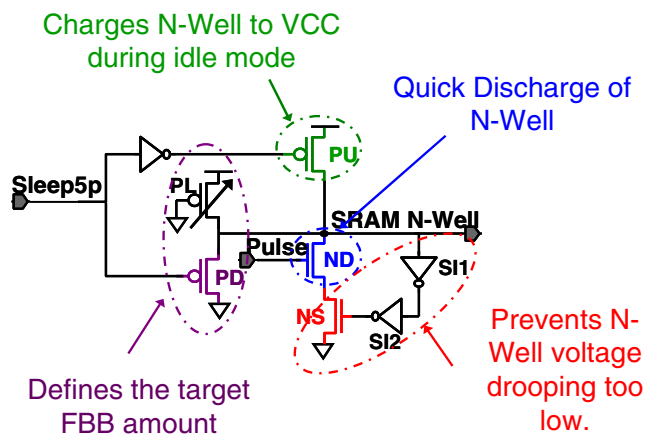


Figure 17: Use of SRAM PMOS FBB to reduce the Vccmin impact of mismatch due to random variation

Systematic variation is best minimized through the use of good layout techniques. One of the design techniques used in the 45nm generation was to lay out matched devices so that they have the same centroid or center of gravity (see Figure 18); then, any device effect that manifests itself as a gradient across the layout will impact each set of matched devices equally.

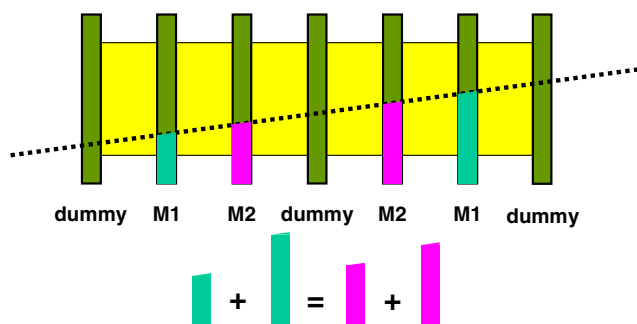


Figure 18: Common centroid layouts were used in the 45nm generation as pure design techniques to mitigate the impact of systematic variation

CHARACTERIZATION OF VARIATION IN THE 45NM GENERATION

We illustrate the success of these mitigation techniques by reviewing detailed data characterizing variation in the 45nm generation. Three different types of measurements are presented to illustrate various variation mechanisms. The first is an in-fab measurement of variation, used to characterize CD variation for 45nm versus 65nm and

90nm generations. The second is DC electrical measurement of matched transistor pairs, used to extract random variation for 45nm versus 65nm transistors. The third is frequency measurements of product ring oscillators, used to determine both systematic and random WIW and within-die (WID) variation for 45nm versus 65nm products.

In-Fab Characterization of Critical Dimension (CD)

Maintaining poly-gate control is critical for managing variation between process generations. Figure 19 presents summary data from in-line measurements of gate CD across four generations that show that the 45nm technology generation was able to maintain a 0.7X scaling to prior generations for WID, WIW, and total variation.

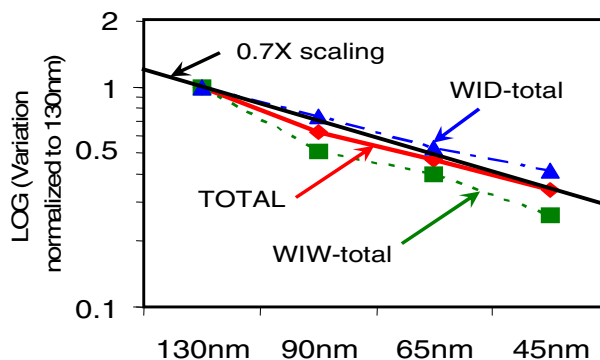


Figure 19: The 45nm generation continued the historical scaling trend of 0.7X in poly-gate variation control

DC Measurement of Matched Transistor Pairs

DC electrical measurement of matched transistor pairs is a basic technique used to extract random variation for 45nm versus 65nm transistors. Figure 20 illustrates the random variation for both 65nm and 45nm generations as extracted from matched transistor pairs. Note an ~20% improvement in intrinsic random variation from the 65nm to 45nm generations.

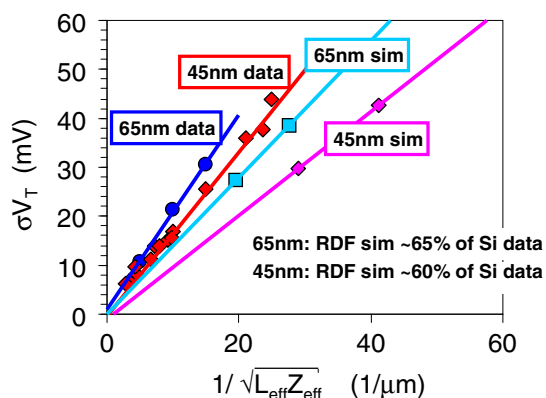


Figure 20: Pelgrom plot illustrating the improvement of the 45nm over 65nm generations

Ring Oscillator Measurements

A powerful tool for assessing process variation is locating ring oscillators (see Figures 21 and 22) routinely in all product designs. The detailed ring-oscillator data can be used to identify areas of concern for process teams to resolve.

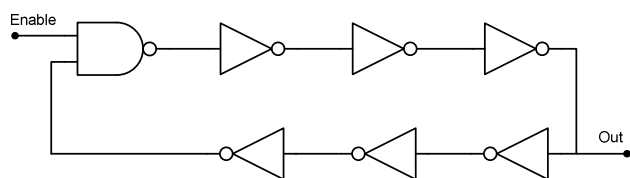


Figure 21: Ring oscillators can be located in product die

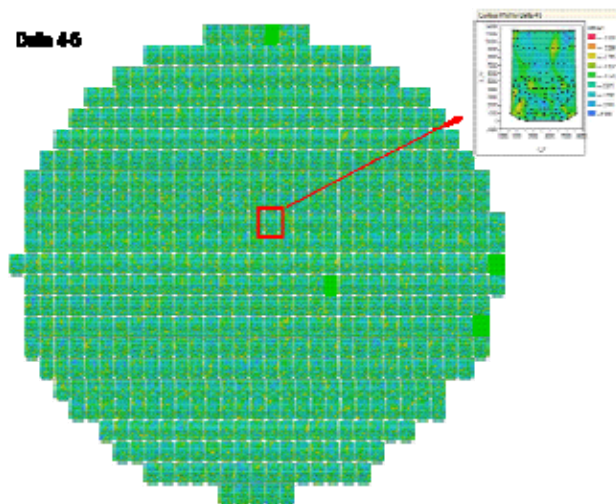


Figure 22: Ring oscillators were added to 45nm products to provide detailed within-die and within-wafer variation data on revenue product material

Figures 23 and 24 show examples of the use of ring-oscillator frequency to determine systematic and random WIW variation across generations. Systematic WIW variation data from ring oscillators (Figure 23) on microprocessor product material illustrates that systematic variation has remained essentially constant across the last four generations. Random WIW variation data from ring oscillators (Figure 24) on microprocessor product material illustrates the ~50% improvement in random variation between the 65nm and 45nm generations enabled by HiK+MG. Note also that the 45nm random WIW variation is comparable to the 130nm process generation.

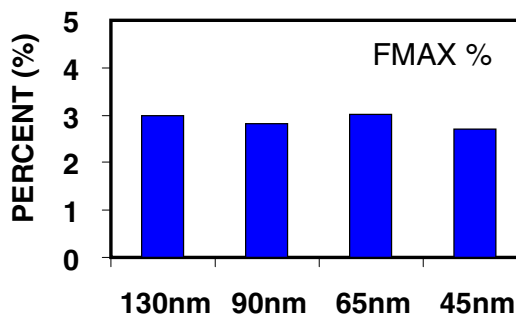


Figure 23: Systematic within-wafer variation data from ring oscillators on microprocessor product material illustrating that systematic variation has remained constant across the last four generations

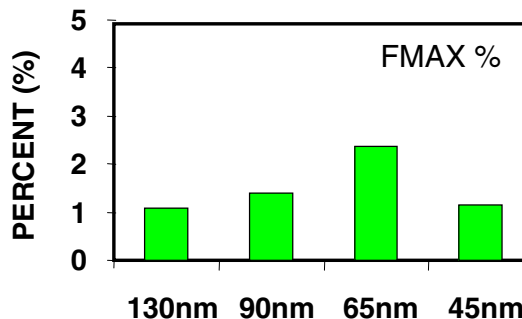
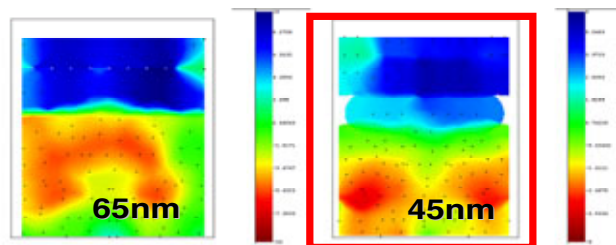
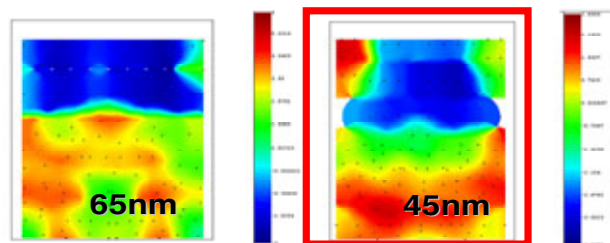


Figure 24: Random within-wafer variation data from ring oscillators on microprocessor product material illustrating the ~50% improvement in random variation enabled by HiK+MG between the 65nm and 45nm generations

Figure 25 gives an example of ring-oscillator data (used in conjunction with a calibration structure) to extract average systematic WID V_T variation comparisons between 65nm and 45nm generations. Note that NMOS has improved 45% (from 20mV to 11mV) and PMOS has improved 22% (from 9mV to 7mV) between the 65nm and 45nm generations.



VTN variation (Mean die VTN – VTN)
Range: 20mV for 65nm → 11mV for 45nm



VTP variation (Mean die VTP – VTP)
Range: 9mV for 65nm → 7mV for 45nm

Figure 25: Ring-oscillator data (used in conjunction with a calibration structure) to extract 65nm to 45nm systematic within-die NMOS and PMOS V_T variation illustrating the improvement is enabled by HiK+MG between the 65nm and 45nm generations

CONCLUSION

Although there has been a trend in the CMOS literature in recent years to convey process variation as a new challenge, process variation has always been a critical element in semiconductor fabrication. From the first discussion of random variation by Shockley in 1961 [3] to the most recent 45nm results [14, 17], understanding and mitigating process variation has been a continuing theme throughout semiconductor history.

While management of process variation is likely to play an increasingly important role in technology scaling, a variety of process, design, and layout techniques can be applied to mitigate the impact of this variation. Examples of pure process mitigation techniques used in the 45nm technology include targeting key transistor properties to reduce RDF, reducing traps at the HiK+MG interface to reduce random charge variation, improving patterning techniques to reduce LER and endcap variation, and improving polishing technologies to reduce systematic cross-wafer variation. Examples of combination design-process techniques used in the 45nm generation include optimizing topology, using OPC to reduce random and systematic variation and adding dummy features to reduce systematic variation. Examples of pure design techniques

used in the 45nm generation include chopping techniques to compensate for random variation and common-centroid techniques to compensate for systematic variation.

The success of the 45nm process variation mitigation techniques is well illustrated by 45nm data. In-line measurements of gate CD across four generations show that the 45nm technology generation was able to maintain a 0.7X scaling to prior generations for WID, WIW, and total variation. Intrinsic random variation extracted from matched transistor pairs shows an ~20% improvement in intrinsic random variation from the 65nm to 45nm generations. Systematic WIW variation data from ring oscillators on microprocessor product material illustrates that systematic variation has remained essentially constant across the last four generations. Random WIW variation data from ring oscillators on microprocessor product material illustrates an ~50% improvement in random variation between the 65nm and 45nm generations enabled by HiK+MG. Ring oscillator data (used in conjunction with a calibration structure) shows that NMOS average systematic WID V_T variation has improved 45% (from 20mV to 11mV) and PMOS has improved 22% (from 9mV to 7mV) between the 65nm and 45nm generations.

The key message of this paper is that process variation is not an insurmountable barrier to Moore's Law, but is simply another challenge to be overcome. This message is illustrated with data from the 45nm process generation where process variation is shown to be at least equivalent to (and in many cases better than) process variation in the 65nm and 90nm process generations.

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