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Intel's 45nm CMOS Technology

**45nm High-k+Metal Gate  
Strain-Enhanced Transistors**

# 45nm High-k+Metal Gate Strain-Enhanced Transistors

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Index words: CMOS transistor, logic technology, high-k gate dielectric, metal gate

## ABSTRACT

For the 45nm technology node, high-k+metal gate transistors have been introduced for the first time in a high-volume manufacturing process [1]. The introduction of a high-k gate dielectric enabled a 0.7x reduction in  $T_{ox}$  while reducing gate leakage 1000x for the PMOS and 25x for the NMOS transistors. Dual-band edge workfunction metal gates were introduced, eliminating polysilicon gate depletion and providing compatibility with the high-k gate dielectric.

In addition to the high-k+metal gate, the 35nm gate length CMOS transistors have been integrated with a third generation of strained silicon and have demonstrated the highest drive currents to date for both NMOS and PMOS. An SRAM cell size of  $0.346\mu^2$  has been achieved while using 193nm dry lithography. High yield and reliability has been demonstrated on multiple single-, dual-, quad-, and six-core microprocessors.

## INTRODUCTION

One of the key methods to enable transistor gate length scaling over the past several generations has been to scale the gate oxide. This improves the control of the gate electrode over the channel, enabling both shorter channel lengths and higher performance. As the gate oxide was scaled the gate leakage increased; this increase in gate leakage was insignificant until the 90nm technology node (Figure 1). At the 90nm and 65nm nodes, the scaling of

the gate oxide slowed as a result of the power limitations from the increase in gate leakage. In order to overcome this at the 45nm technology, a gate dielectric with a higher dielectric constant (high-k) has been introduced. This enabled a >25x gate leakage reduction while scaling the  $T_{ox}$  by 0.7x.

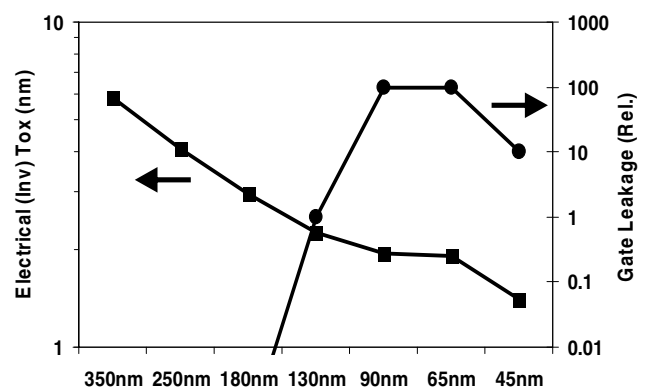


Figure 1: Trend of inversion  $T_{ox}$  and gate leakage vs. Intel technology node

The introduction of high-k gate dielectrics has been slowed by several issues [2–4]. The first was the interaction by the high-k material with the existing polysilicon gates. This interaction led to high trap densities at the interface that pinned the  $V_t$  of the transistor to an undesirable value. The second was the

degradation of the channel mobility in the presence of high-k dielectrics. The third issue was the poor reliability of the high-k dielectric.

The gate electrode effectiveness has also been increasingly impacted by poly depletion effects. This has led to lower drive currents when the transistor is turned on. By selecting a compatible metal gate electrode with the high-k gate dielectric, both the poly depletion effects and the  $V_t$  pinning at the high-k/polysilicon interface can be eliminated while providing higher channel mobilities [5].

In introducing high-k+metal gate transistors for the 45nm generation, these significant challenges needed to be overcome. First, we had to determine which material to use for the high-k dielectric and find dual-band edge metals that were compatible with that high-k dielectric. Second, an integrated CMOS flow needed to be developed that matched the channel mobility of  $\text{SiO}_2$  while meeting the reliability requirements for the technology. The development of this CMOS flow was complicated by the need to mesh the process requirements of the metal gate process with both the thermal limitations of the junction formation steps and the uniaxial strain-inducing steps, both of which have become central to the transistor architecture.

Along with the above-mentioned improvements in performance and gate leakage with high-k+metal gate, a key requirement of the technology node was an increased packing density for the transistors. For each node, an ~50% area scaling is expected, and this technology continues that trend. A key challenge to overcome in this scaling is the loss of performance due to scaling of the stress-inducing features of the technology. Use of 193nm dry lithography for critical layers at the 45nm technology node was preferred over moving to 193nm immersion lithography, due to lower cost and greater maturity of the toolset. In order to achieve the tight 160nm gate and contact pitch requirements, unique gate and contact patterning process flows were developed and implemented.

## TRANSISTOR PROCESS FLOW

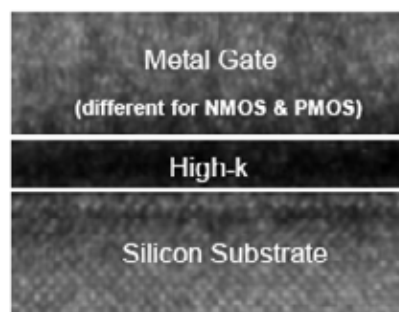
The two common methods for introducing a metal gate to the standard CMOS flow include either a “gate-first” or “gate-last” process. Most comparisons of these two process flows focus on the ability to select the appropriate workfunction metals, the ease of integration, or the ability to scale; however, these comparisons typically fail to comprehend the interaction of the process flows with the strain-inducing techniques. By use of a high-k first and metal gate-last flow, it is possible to maximize the benefits of the stress-inducing steps and high temperature junction

formation, while minimizing the thermal processing of the workfunction metals.

In the metal gate-first flow (Table 1), the high-k dielectric and dual-metal processing are completed prior to the polysilicon gate deposition. The dual metal gates are then subtractively etched along with the poly gates prior to Source/Drain (S/D) formation. In contrast, for the high-k first and metal gate-last flow used in this work, a standard polysilicon gate is deposited after the hafnium-based, high-k gate dielectric deposition (Figure 2). This is followed by a standard polysilicon processing flow through the salicide formation steps.

**Table 1: Comparison of unique steps in gate-first and high-k first, metal gate-last process flows. Key differences are highlighted in bold.**

Gate-First	High-k first, Gate-Last
Isolation	Isolation
High-k gate deposition	High-k gate deposition
<b>Dual Metal-Gate Deposition</b>	Poly-Silicon gate deposition/patterning
Poly-Silicon gate deposition	S/D formation
<b>Poly-Silicon/metal etch</b>	Salicide/Contact etch stop
S/D formation	<b>Poly-Silicon gate removal</b>
Salicide/Contact etch stop	<b>Dual-Metal Gate deposition</b>
1 <sup>st</sup> ILD deposition/polish	Contact formation
Contact formation	Contact formation



**Figure 2: TEM of high-k/metal gate stack**

After deposition of the contact etch stop and the first Interlayer Dielectric (ILD) films, a polish step is used to expose the poly gates and enable removal of the dummy poly. The PMOS workfunction metal is then deposited. A patterning step removes the PMOS metal from the NMOS

area. The NMOS workfunction metal is deposited, and the gate trenches are filled with Al for low gate resistance. By using novel gap-fill techniques, robust gate resistance is enabled to sub-30nm gate lengths (Figure 3). A metal polish step is used to remove the excess metal and planarize the gate trenches. The flow then continues with the contact and interconnect processing steps.

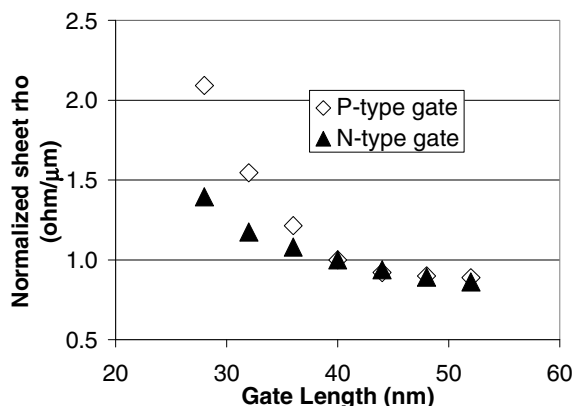


Figure 3: Gate sheet rho versus gate length showing scalability of gate fill process

Figure 4 shows a TEM of the high-k/metal gate NMOS and PMOS transistors with the embedded SiGe S/D strain layer on the PMOS and Ni salicide. The strained silicon techniques that Intel first introduced at the 90nm and 65nm nodes were further enhanced in this generation. The Ge concentration of the embedded SiGe S/D was increased to 30% from the previous generations of 23% in Intel’s 65nm technology [6] and 17% in the 90nm technology [7].

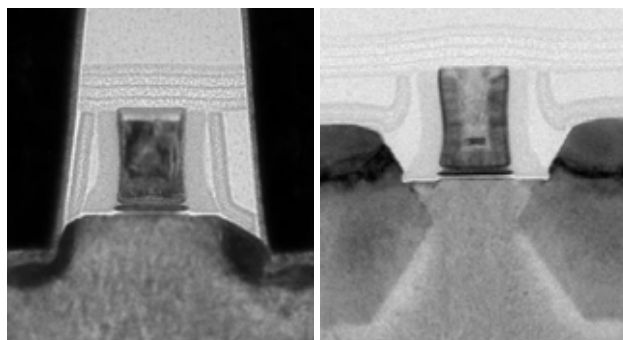


Figure 4: TEMs of high-k+metal gate NMOS and PMOS transistors

### DESIGN RULES AND 193NM DRY PATTERNING

Contacted gate pitch is a key measure of front-end density, and the scaling to 160nm maintains the 0.7x scaling trend (Figure 5). This is the most aggressive contacted gate pitch reported to date for a 45nm high-performance logic

technology. The contact process has also been modified, with trench contacts replacing conventional contacts for lower series resistance. Trench-contact-based local routing improves layout density, especially for cross-coupled inverter pairs that are very common in microprocessor SRAM and register file arrays. Tight pitches and trench contacts allow SRAM cell size to be scaled to 0.346μm<sup>2</sup> (Figure 6).

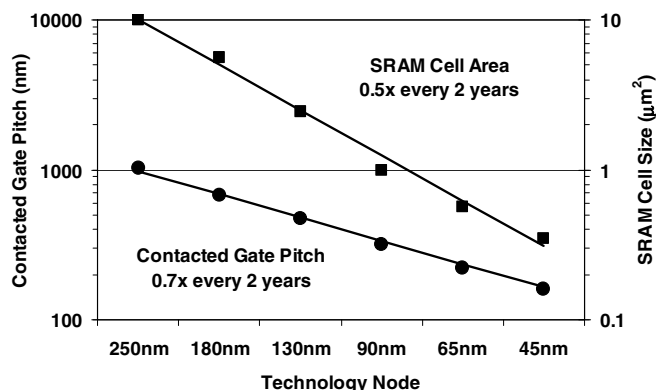


Figure 5: Contacted gate pitch and SRAM cell size scaling trend for Intel’s technology nodes

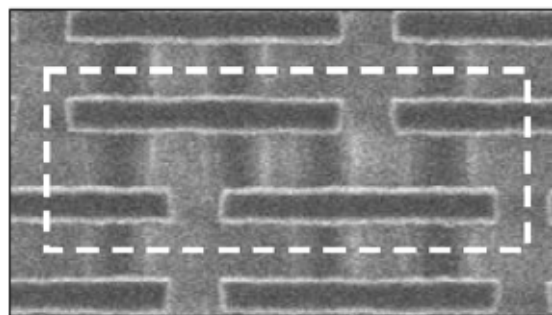
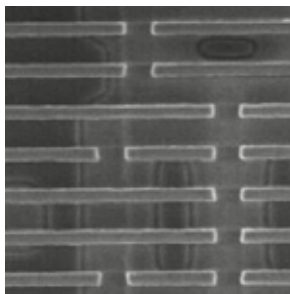


Figure 6: Diffusion and poly layers for 0.346 μm<sup>2</sup> 6-T SRAM cell

In order to enable these tight pitches by use of low-cost 0.92NA 193nm dry patterning, innovative processes were developed to produce robust patterning. This is demonstrated by the fidelity of the poly lines in Figure 6. The gate patterning process uses a double patterning scheme. Initially the gate stack is deposited including the polysilicon and hardmask deposition. The first lithography step patterns a series of parallel, continuous lines. Only discrete pitches are allowed, with the smallest at 160nm, to assist in the patterning. A second masking step is then used to define the cuts in the lines. The two-step process enables abrupt poly endcap regions, devoid of rounding that allows for tight contact-to-gate design rules (Figure 7). There are no additional masking steps from this process, since the 65nm generation also used two reticles for poly patterning.

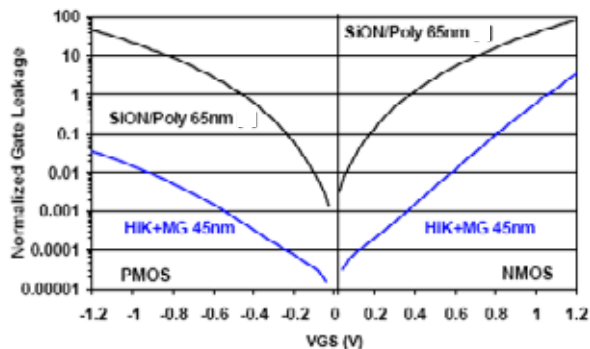


**Figure 7: Top-down SEM post-poly-patterning process showing 160nm poly pitch with minimum gate length lines. Note the square poly ends, devoid of rounding.**

The contact patterning process uses a similar pitch restriction to facilitate lithography. Trench diffusion contacts run parallel to the gates with discrete pitches, while trench gate contacts run orthogonal to the gates. Use of trench contacts has the added benefits of lowering the contact resistance by >50% and allowing their use as a local interconnect, which improves SRAM/logic density by up to 10%.

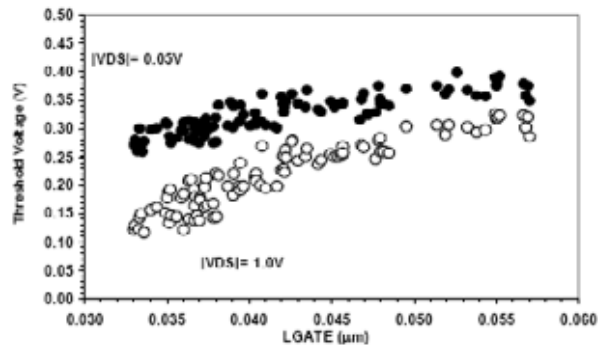
**TRANSISTOR RESULTS**

The introduction of the high-k gate dielectric delivered a dramatic gate leakage reduction relative to 65nm transistors of >25X for NMOS and 1000X for PMOS (Figure 8).

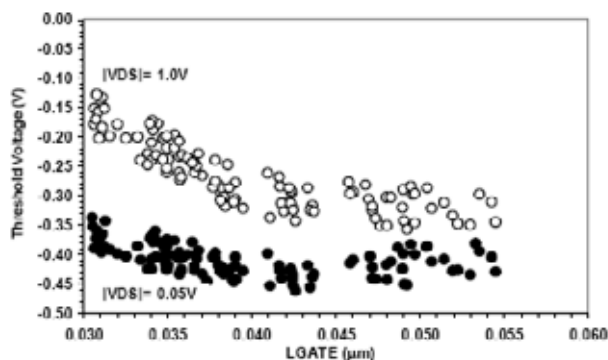


**Figure 8: Gate leakage reduction of 25-1000x with use of high-k+metal gate relative to 65nm technology**

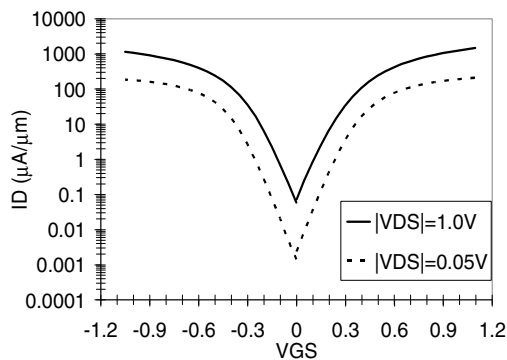
The high-k+metal gate transistors exhibit excellent short channel characteristics due to the combination of  $T_{ox}$  scaling and the optimal workfunction metal gates (Figures 9 and 10). The excellent gate control is also illustrated in the well-behaved subthreshold characteristics (Figure 11).



**Figure 9: NMOS  $V_t$  vs.  $L_g$  shows excellent SCE and DIBL**



**Figure 10: PMOS  $V_t$  vs.  $L_g$  shows excellent SCE and DIBL**



**Figure 11: Subthreshold  $I_d$ - $V_{gs}$  for both NMOS and PMOS transistors**

PMOS performance is improved by using high-k+metal gate as well as by the enhancements to the embedded SiGe processing. The PMOS drive current (Figure 12) of 1.07 mA/ $\mu$ m is a marked 51% improvement over 65nm [8]. NMOS drive current (Figure 13) is 1.36mA/ $\mu$ m, 12% better than the previous-generation, 65nm transistors. The average drive current improvement versus 65nm is 32% at the same voltage and  $I_{off}$ , despite scaled transistor pitch. The linear drive currents show similar enhancements with PMOS (Figure 14) at 0.178mA/ $\mu$ m and NMOS (Figure 15) at 0.192mA/ $\mu$ m. These drive currents are benchmarked at 1.0V, a low 100nA/ $\mu$ m  $I_{off}$  and at 160nm

contacted gate pitch. Both the saturated and the linear drive currents represent the best drive currents reported to date for a 45nm technology at low  $I_{off}$ . Figure 16 shows the transistor performance vs. gate pitch for this generation illustrating that both density and performance are improved with this transistor flow.

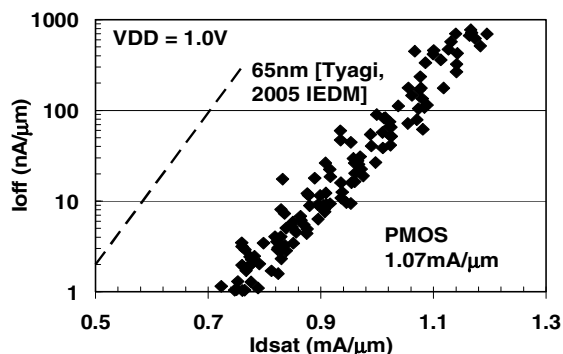


Figure 12: PMOS  $I_{dsat}$  of 1.07mA/μm at 100nA/μm  $I_{off}$  and  $V_{dd}=1.0V$

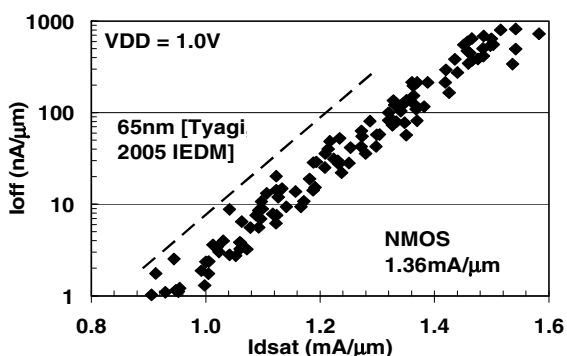


Figure 13: NMOS  $I_{dsat}$  of 1.36mA/μm at 100nA/μm  $I_{off}$  and  $V_{dd}=1.0V$

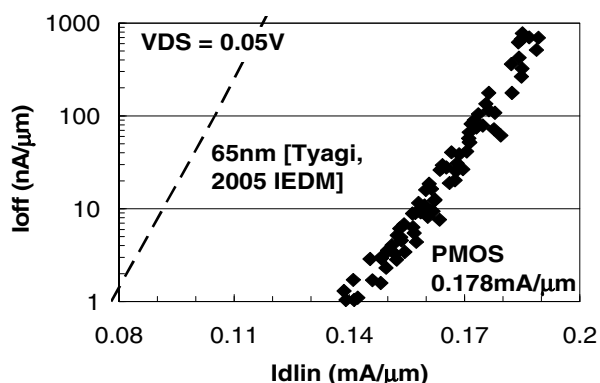


Figure 14: PMOS  $I_{dlin}$  of 0.178mA/μm at 100nA/μm  $I_{off}$  and  $V_{ds}=0.05V$

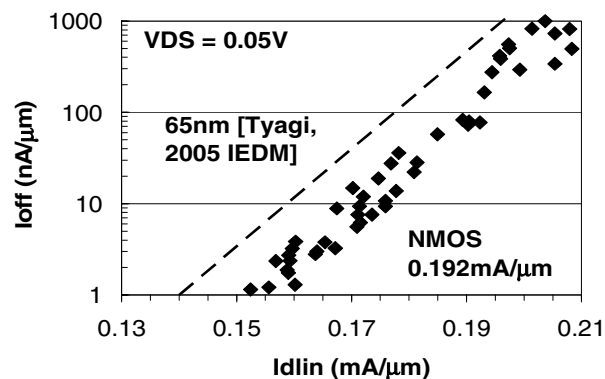


Figure 15: NMOS  $I_{dlin}$  of 0.192mA/μm at 100nA/μm  $I_{off}$  and  $V_{ds}=0.05V$

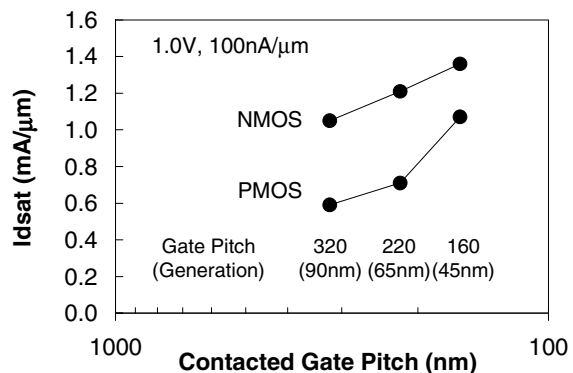


Figure 16: Performance vs. gate pitch for 90, 65, and 45nm generations

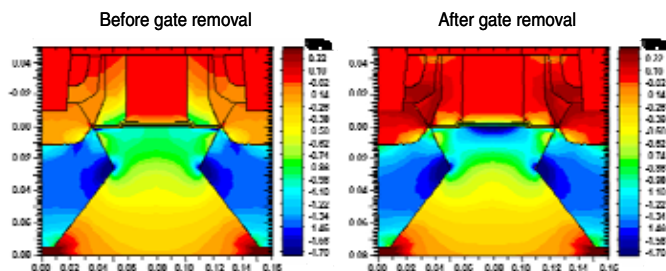
### STRESS ENHANCEMENT IN A METAL GATE FLOW

Since its introduction at the 90nm node, strain has become a central performance enhancement element for the standard CMOS flow. The most commonly used techniques for implementing strain in the transistors include embedded SiGe in the PMOS S/D, stress memorization for the NMOS, and a nitride stress-capping layer for NMOS and PMOS devices (Table 2).

**Table 2: Comparison of stress enhancement methods for 65nm and 45nm nodes. New features are highlighted in bold.**

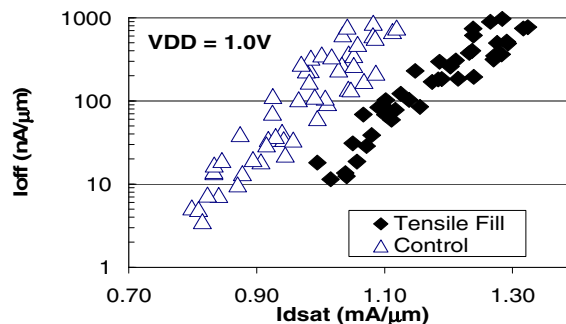
65nm Method	45nm Method
<b>PMOS</b>	<b>PMOS</b>
Embedded SiGe S/D	Embedded SiGe S/D with <b>higher %Ge</b>
	<b>Poly Gate Removal Enhancement</b>
<b>NMOS</b>	<b>NMOS</b>
Tensile Nitride Cap	<b>Tensile Trench Contacts</b>
Gate Stress Memorization + S/D Stress Memorization	<b>Metal Gate Stress (MGS) + S/D Stress Memorization</b>

A key benefit of using a gate-last flow comes from removing the poly gate from the transistor after the stress-enhancement techniques are in place. It has been shown that the stress benefit from the embedded S/D SiGe process is enhanced through this removal of the poly gate, since the poly gate acts as a buffer counteracting the effect of the embedded S/D SiGe [9]. This benefit can be illustrated in simulation with an estimated 50% increase in lateral compressive stress by removal of the polysilicon gate (Figure 17). The combined impact of the increased Ge fraction in the embedded S/D and the strain enhancement from the gate-last process allow for a 1.5x higher hole mobility compared to 65nm, despite the scaling of the transistor pitch from 220nm to 160nm.



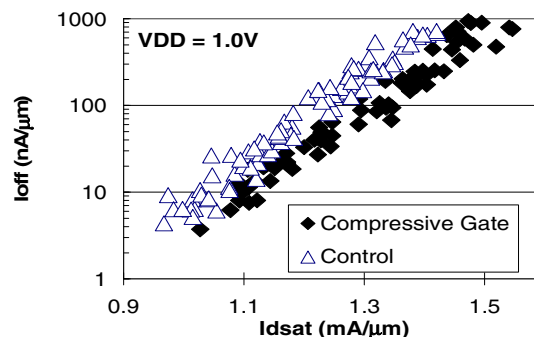
**Figure 17: Stress contours in the PMOS transistor before and after the removal of the polysilicon dummy gate. Stress in the channel is shown to increase 50% from 0.8GPa to >1.2 GPa.**

For the NMOS device, two methods of stress enhancement have been employed in this technology. First, the loss of the nitride stress layer benefit, due to scaling the pitch from the 65nm technology node, has been overcome by the introduction of trench contacts and by tailoring the contact fill material to induce a tensile stress in the channel. The NMOS response to tensile (control) vs. compressive contact fill materials is shown in Figure 18. The stress impact of the trench contact fill material on the PMOS device is mitigated by use of the raised S/D inherent in the embedded SiGe S/D process.



**Figure 18: Ion-Ioff benefit of tensile contact fill showing a 10% NMOS Idsat benefit. Contact resistance is matched for the two fill materials.**

For NMOS stress memorization, there are two primary methods commonly used, one is memorization of stress in the (S/D) of the device and the other is memorization in the poly gate [10]. The metal gate-last flow is compatible with the S/D method while the poly gate component would be compromised. To compensate for this, the poly gate component is replaced by Metal Gate Stress (MGS), i.e., modifying the metal-gate fill material to directly induce stress in the channel [11]. By introducing a gate fill material with a compressive stress, the performance of the NMOS device is enhanced and adds to the contact fill technique (Figure 19). By use of a dual-metal process with PMOS first, the stress of the NMOS gate is decoupled from the PMOS gate through optimization of the PMOS gate stack to buffer the stress.

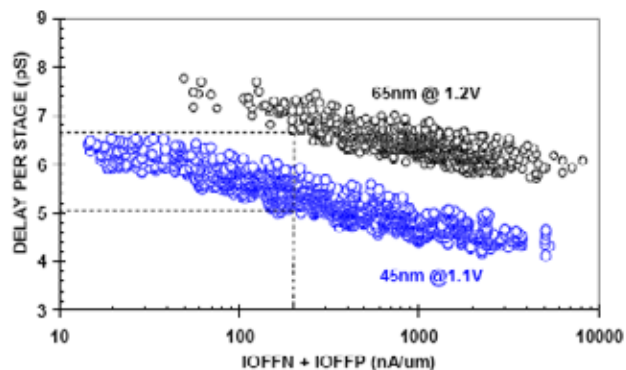


**Figure 19: Ion-Ioff benefit of compressive gate stress showing a 6% NMOS Idsat gain. Tensile contact fill is used on both sets of data.**

## RING OSCILLATORS

The transistor performance gains are reflected in the ring oscillator performance data. Gate delay data from ring oscillators with a fanout of 2 is benchmarked at 100nA/μm Ioff each for NMOS and PMOS, at 1.2V for 65nm and a lower 1.1V for 45nm. The ring oscillators use the minimum contacted gate pitch (220nm and 160nm) for

each technology. Despite the scaling of both voltage and gate pitch, FO=2 gate delay is reduced from 6.65pS (65nm) to 5.1pS (45nm), for a gain of 23% (Figure 20). Table 3 breaks out the RO gains between NMOS/PMOS  $I_{dsat}$ ,  $I_{dlin}$ , and the gate and junction capacitances, illustrating the marked impact of the PMOS performance gains on the ring oscillators.



**Figure 20: Ring oscillator delay vs. leakage for fanout=2. Comparison of delay for 65nm vs. 45nm is at 1.2 and 1.1V, respectively.**

**Table 3: Breakdown of RO gains vs. 65nm results. The voltage scaling term accounts for the reduction in VDD from 1.2V (65nm) to 1.1V (45nm).**

Component	Benefit (%)
PMOS $I_{dsat}$	+13
PMOS $I_{dlin}$	+18
NMOS $I_{dsat}$	+3
NMOS $I_{dlin}$	+2
Cjunction	+2
Cgate/Cov	-8
Voltage Scaling	-7
Total	+23

## CONCLUSION

High-k+metal gate transistors have been integrated into a manufacturable 45nm process for the first time. Selection of the metal-gate flow (high-k first, metal-gate last) was made to maximize the benefit from the strained silicon steps. Novel stress techniques were also developed to replace the stress methods that are compromised due to scaling and the metal gate flow. The scaling of the transistor density was achieved through development of new poly and contact patterning schemes. The resultant transistors provide record drive current at low leakage and

at tight contacted gate pitch achieving both performance and density benefits. This is demonstrated in the ring oscillators with a 23% gate delay reduction compared to 65nm at the same  $I_{off}$  and 10% lower VDD.

## ACKNOWLEDGMENTS

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## AUTHORS' BIOGRAPHIES

**Chris Auth** joined Intel in 1997 after completing his Ph.D. degree in Electrical Engineering from Stanford University. He initially developed the NOR flash cell for Intel's 0.18 $\mu$ m node. After joining Portland Technology Development in 2000, he developed the industry's first use of strain for transistor enhancement at the 90nm and 65nm nodes. At the 45nm node, he led the process development and introduction of the industry-first, high-k/metal-gate process. He has received two IAAs, holds five US Patents, and has authored/co-authored 18 publications. His e-mail is chris.auth at intel.com.

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