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Technology with the Environment in Mind

Evaluation Process for Semiconductor Fabrication Materials that are Better for the Environment

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ABSTRACT

The successful future of the semiconductor industry is dependent upon the development of an array of new and novel materials to make semiconductor devices. In parallel, there is a growing sentiment in public policy and regulatory forums for a highly conservative precautionary approach to approving the introduction of new chemicals into commerce. Intel's business model of *Copy Exactly!* requires new material development very early in the technology development cycle. Therefore, Intel's approach to chemical development, and selection of materials, must incorporate consideration of the environmental impact of its policies and materials extremely early.

Prior to the selection and purchase of fab manufacturing materials at Intel, procedures are in place at the development and selection stages to integrate consideration of the materials' impact on the environment, to collaborate with suppliers and others to reduce that impact, and at the same time to meet Intel's technology needs. In this paper, we provide an overview of what drives the procedures used by Global Fab Materials, we look at how the procedures are used, and we look at the successful results through a case study.

INTRODUCTION

Technology Trend for Material Development

For more than four decades the semiconductor industry has been successfully producing one of the smallest and most effective devices that man has made, in step with Moore's Law [1] which basically predicts a doubling of the number of transistors per chip every two years. Today's modern semiconductors have nearly one billion transistors on them.

It takes over 400 individual steps of manufacturing and testing to make such a device. An individual semiconductor chip (with a postage-stamp-size of manufactured silicon inside, called a die) has not substantially changed in size relative to those seen in the mid 1980s, but the circuitry has increased in complexity 1,500 times. The Intel 386 chip had 275,000 transistors on a 1-micron feature size. Today's Intel® Penryn quad-core chip contains 820 million transistors on a 45-nanometer feature size. This increased complexity is attributable to both the continuous reduction in the size of the transistors on the die that allows for more transistors on the die, and the increased number of layers and features created within the external package surrounding the die, that are necessary to dissipate the intense heat away from the die.

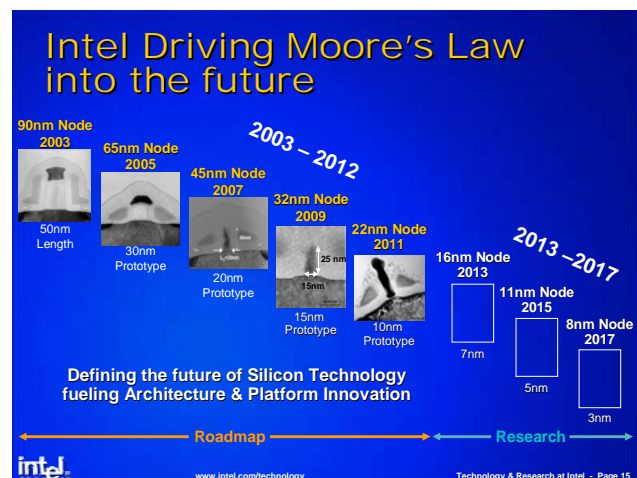


Figure 1: Continuum of reduced feature size

The shrinking feature size of modern semiconductors has created the need to be atomically precise in manufacturing and to have chemicals that are ultra pure. When one examines a 45-nm feature size transistor (see Figure 1), the channel (the area where electrons flow from one leg of

the transistor to the other) is as little as 20 nm, or approximately 100 silicon atoms across. With such a relatively small number of atoms responsible for the overall performance of each transistor, it is critical that they be manufactured without defects or impurities and provide exactly the technical attributes required for the semiconductor to function.

Control of the manufacturing process at the atomic scale has led to a new generation of materials. Examples of these include material changes driven by the need to reduce the particle size and types of chemical interactions in the chemical mechanical polishing (CMP) of the silicon wafers¹. As the feature size continues to decrease, the size of the mechanical polish particles has to decrease as well in order to prevent destruction of the features. For example, transforming a rough-cut stone into a lustrous gem requires many polishing steps using finer and finer grit. Similarly, the chemicals used in the CMP process will likely change any time the material composition of a feature changes (e.g., using mineral spirits to clean up oil-based paint versus water to clean up latex-based paint). Another example of chemicals that have changed in the past is those used in the etching and deposition² manufacturing process steps. In many of these process steps gas-based chemicals are used in place of liquid-based chemicals, since more control can be achieved with the etch depth and deposition thickness in gas-phase chemical reactions. The last example of materials change is in the wafer patterning area, referred to as lithography³. The challenges for lithography, in light of continually smaller features, are several, and two are described here. First, the feature size is now smaller than the wavelength of the light beam being used to make it, which means either the light source must be changed and/or the engineers must play chemical tricks with the patterning material (called photoresist) that is layered on the silicon wafers. Second, the intensity of the light source and the harshness of subsequent etch process steps both play a role in the composition of the photoresist that is used for any one lithography step. Further complexity arises due to the fact that each step may require a different photoresist.

Future semiconductor devices are critically dependent on the ability of stable and reliable materials to support device operation. As the market continues to demand an increase in scaling (miniaturization) with no penalty in performance, the need for new materials with increased mobility—lower energy and higher speed—is greater. Since devices are comprised of several materials and interfaces, the properties of new materials and their ability to interface with the properties of other materials will require materials with dramatically improved or new properties. All of these changing materials needs have led to an explosion in the use of differing atoms from the Periodic Table of Elements (see Figure 2).

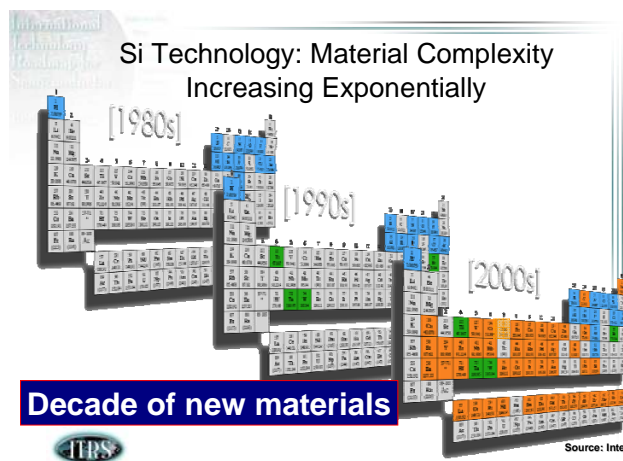


Figure 2: Increasing complexity of materials

PRECAUTIONARY POLICY

Thousands of chemicals have been developed and are used to manufacture the products we use in everyday life. Despite the widespread use of chemicals, until recently the prevailing thought was that exposure to most industrial chemicals was unlikely, especially outside the industrial environment. For years, regulatory policies toward such chemicals have presumed them to be safe with little or no information on their health implications. The U.S. EPA has found that even a basic level of toxicity information exists for less than ten percent of the approximate 2800 high-production-volume chemicals (those produced over one million pounds per year). The absence of information is often misinterpreted as evidence of safety. Growing evidence that some chemicals can potentially cause harm, and concern that current global chemical policies are not sufficient to predict or prevent potential harm to individuals or the environment, have led to major reforms in industrial chemical policies worldwide. The most prevalent perspective today is known as the Precautionary Principle, which in effect requires that precautionary action be taken before there is scientific certainty of cause and effect.

Seeking out and evaluating alternatives is preferred rather than asking what level of contamination is safe or economically optimal. The precautionary approach asks how to reduce or eliminate the hazard and considers all possible means of achieving that goal [2].

The precautionary perspective underscores a basic difference between hazard approach vs. risk approach. The first is absolute in terms of eliminating materials should they pose an “unacceptable” hazard. The risk approach evaluates whether or not a hazard will have an impact (e.g., human exposure) and determines how the impact can be mitigated.

“Copy Exactly!” Factory Strategy

Intel introduced its “Copy Exactly!” factory strategy in the mid-1980s and completed its adoption in 1996. Intel can credit “Copy Exactly!” with enabling the company to bring factories online quickly with high-volume practices already in place; hence, decreasing time to market and increasing production yields.

“Copy Exactly!” solves the problem of getting production facilities up to speed quickly by duplicating everything from the technology development facility to the volume-manufacturing factory. In particular, it means ensuring that the process devised at the development facility is fine-tuned not just for performance and reliability, but for high-volume production as well. (Background information on Intel’s Copy Exactly! strategy can be found at [4].)

“Copy Exactly!” Versus Traditional Semiconductor Factory Strategy

In most semiconductor factories, equipment and processes used in research vary greatly from those used in high-volume manufacturing. At many companies, each new technology is brought to a technology development facility where a team of engineers precision-tune the process until it is perfected. Then the process is transferred to a high-volume manufacturing facility where a new set of engineers modifies the process so that it can be produced in large quantities.

The impact of Intel’s Copy Exactly! policy on materials is that development and selection must occur much earlier in the technology development cycle, including the evaluation for Environmental Health and Safety (EHS) performance.

INTEL® GLOBAL FAB MATERIALS ORGANIZATION SYSTEM

Intel’s Global Fab Materials (GFM) organization is responsible for early chemical development and procurement of semiconductor die manufacturing materials. Intel conducts a thorough EHS evaluation of chemicals prior to their use at Intel and implements state-of-the-art exposure control and environmental emissions abatement technology for managing their use. GFM deals with EHS considerations at the earlier stages of chemical development and selection from both industry and company perspectives. GFM’s strategy is to enable continued global growth of our operations, while identifying and prioritizing new chemicals of EHS concern for further evaluation. We determine information requirements; and work on collaborating with our supply chain, consortia, and research and development organizations to balance the demands for new technology development, Copy Exactly!, and public policy concerns

as part of materials development. Components of the GFM Materials EHS system include 1) External Research and Development, 2) Supplier Engagement, and 3) Integration with the overall Materials Risk Evaluation System.

EXTERNAL RESEARCH & DEVELOPMENT

Consortia Engagement

The mission of our external programs is to influence the direction of the research; then to extract the value from external R&D organizations and activities and to bring this back to Intel. These are some of the items that we look at:

- The current (and evolving) EHS trends and their potential impact on Intel.
- The response needed from university and fundamental research to address these EHS trends.
- The research needed to develop science and technology leading to simultaneous process performance/cost/EHS gain.
- Incorporating EHS principles into engineering and science education.
- Promoting Design for Environment and sustainability as a technology driver and business benefit.

On an industry level, Intel collaborates on EHS issues with other semiconductor manufacturers and with our suppliers of tools and chemicals in national associations, such as the International Sematech Manufacturing Initiative (ISMI), and the U.S. and European Semiconductor Industry Associations (SIA and ESIA, respectively). Broad industry needs with regard to EHS elements of new technology (including chemicals) are integrated into the International Technology Roadmap for Semiconductors (ITRS). The ITRS is a global industry 15-year roadmap that identifies technology requirements for the continued success of the semiconductor industry.

Intel also actively participates in the World Semiconductor Council (WSC), a global industry body whose efforts include pre-competitive cooperation on major EHS policy issues for the industry. Membership is composed of semiconductor trade associations from six leading global centers of manufacturing (EU, China, Taiwan, Japan, Korea, and the U.S.). Global collaboration at the WSC level has led to voluntary global industry agreements on the responsible use of chemicals. A key initiative has been the reduction of global warming by reducing perfluorinated compounds (PFCs) emissions by 10% lower than 1995 levels by 2010. A second example is

the full phase-out of perfluorooctyl sulfonates (PFOS) in non-critical applications while also continuing R&D to eventually phase out critical uses, where possible.

Environmentally Benign Materials Research (EBMR) is a key program that GFM-EHS uses to enhance the sustainability of current and future technologies. This program identifies critical material research needs for environmental purposes, such as alternatives to PFCs, and targets research to find solutions, or at a minimum, gain better knowledge about the nature of the problem. These projects can be accomplished internally with direct assistance from suppliers, or via industry consortia such as the ISMI, the Semiconductor Research Corporation's Engineering Research Center (SRC-ERC), and the semiconductor consortia in Belgium (IMEC), for example.

Intel has been a promoter of collaborative R&D efforts to create the science, technology, and educational methods to remain in a leadership position in promoting a safe and environmentally conscious supply chain.

Consortia External Supplier Engagement

Via some of these consortia efforts, Intel GFM has some indirect interaction with suppliers to assist in directing their efforts towards the industry's needs. An example of this is the SEMATECH Supplier Data Council. This team consisted of chemical suppliers and device makers whose mission was to determine how to obtain consistent timely EHS data for semiconductor chemicals. The team created a standardized methodology to guide the development of consistent EHS data by suppliers and a method to communicate the data to suppliers and downstream manufacturing users.

DIRECT SUPPLIER ENGAGEMENT

Addressing EHS concerns and issues successfully for the long-term sustainability of our industry requires close collaboration with Intel's suppliers. Furthermore, integrating EHS into the design of new chemicals is generally easiest in the early stages of development (see Figure 3). This is also one of the challenges stated in the ITRS. The specific challenge is a lack of timely information flowing to the technology teams about the EHS characteristics of new materials in order to help minimize the EHS impact of chemicals used.

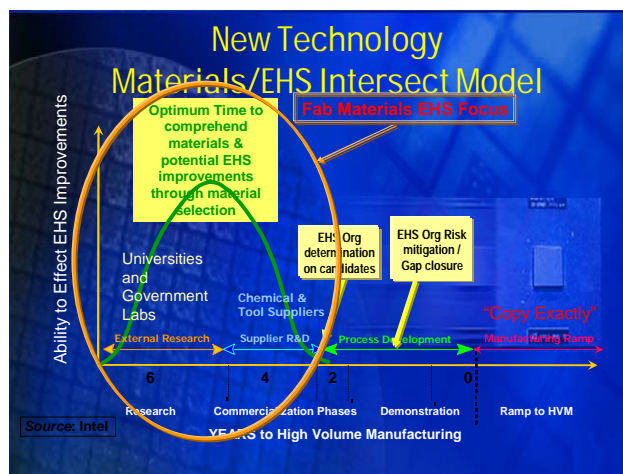


Figure 3: Integrating EHS into the design of new chemicals

One of the Intel GFM's goals is to close the chemical data gap by ensuring that Intel's chemical suppliers generate, distribute, and communicate information on chemical toxicity. Chemical suppliers are best equipped to acquire and provide this information and in some instances are required to do so by law. This is seen as necessary to meet the requirements of the European Union Registration, Evaluation, Authorization and potential Restrictions of Chemicals (REACH) legislation. REACH represents the EU's effort to address long-standing deficiencies in chemical information.

An electronic template was developed through collaboration between semiconductor manufacturers and suppliers that allows suppliers to provide specific EHS information data sets as a condition of the purchase of the chemicals. This information is then used to make risk-based chemical decisions to enable the use of the chemistry. In addition, we have certain basic supplier guidelines for developing new chemicals [3].

On an annual basis, Intel GFM EHS communicates with supplier executives on EHS expectations and exchanges information regarding EHS trends and issues at Intel Supplier Day. In 2006 for example, Intel provided pertinent information on the new REACH regulation that communicated the primary supplier requirements to ensure a continued supply of chemicals to Intel's European operations. We provided information on the new international mandate for a globally harmonized hazard classification and compatible labeling system, including material safety data sheets (MSDS) and easily understandable symbols. Intel also provided information on the new global restriction of hazardous substances regulations and Intel's supplier intellectual property management systems. Intel Material Supplier Day presentations are an effective mechanism to engage

supplier executives outside traditional supplier-to-customer relationships.

Intense competition for chemical market share makes the security of intellectual property (IP) a critical component of supplier management. Simultaneously, accurate and timely disclosure of EHS data for proprietary chemical ingredients is crucial for a comprehensive EHS risk assessment and avoidance of any current and future regulatory consequences. A mechanism was developed by Intel's GFM and EHS groups to improve the flow of EHS data to ensure the safe use of chemicals while simultaneously improving the protection of suppliers' IP. This mechanism, the Supplier EHS IP Management System (SEIMS), is a data management application for EHS-related documents containing supplier intellectual property. These are some of its key features:

- Design to enhance the security of suppliers' IP and limiting dissemination within Intel to only those with a need-to-know to make sure that chemicals can be used safely.
- Ensures appropriate and secure document management within Intel.
- Enables supplier document submission online to Intel, eliminating the inefficiency and security issues of manual document management.
- Intel personnel without a need-to-know are unable to view, physically control, or manipulate the supplier's IP.

Chemical suppliers play a vital role in our quest toward greener chemistry and sustainable manufacturing. On a proprietary basis, Intel identifies areas where specific EHS concerns with certain materials exist, and we coordinate closely with suppliers to develop material solutions where both technical and EHS needs can be met.

INTEGRATION WITHIN INTEL

The final parts of the GFM EHS system are a Regulatory Early Screening process, EHS elements in the general Materials Risk Assessment, and integration of the GFM results into Intel's overall EHS material evaluation and risk mitigation process. At this stage of technology development, a list of candidate materials is created that focuses the development and EHS systems on likely chemicals for the new generation of technology.

Early Screening

GFM developed and implemented a regulatory early screening procedure to proactively evaluate and mitigate associated risks identified through government authorities responsible for approving new chemicals for the industrial market. The scope of early screening covers all legacy

materials as well as potential candidate chemicals for the new technology. This analysis is done in conjunction with Intel suppliers who develop the EHS and industrial application information portfolio for their materials. Since requirements vary with regard to both the location of chemical manufacturing and the final location for semiconductor manufacturing, this screening can include multiple schemes of data and information from various geographies (e.g., U.S. Toxics Substances Control Act, Korean Toxic Substances Control Act, etc.).

Materials Risk Assessment

Another key responsibility of Intel GFM-EHS is to ensure that regulatory or EHS constraints in the Fab materials supply chain are mitigated prior to chip high-volume manufacturing (HVM) proliferation. Failure to comply with regulatory requirements can lead to prohibition of materials shipment to the factories. Lack of proper EHS risk evaluation of materials before HVM use may result in last-minute risk mitigation actions being required as the new semiconductor technology is ready for delivery to HVM facilities.

A Materials Risk Assessment (MRA) program is utilized to determine and then mitigate potential risk in materials EHS readiness and regulatory compliance. Throughout the development lifetime of each new technology, any issues identified through the MRA evaluation are logged, mitigation actions are identified, and a completion plan is implemented to manage each issue identified.

Internal Collaboration with Intel's EHS Cross-site HVM Review Process

Intel policy requires a comprehensive EHS review of all chemicals identified for use at Intel. GFM development and procurement experts and evaluators in EHS departments across the company all work closely to achieve the Intel EHS mission. Materials evaluation is conducted before the first sample shipment to an Intel facility. The evaluation starts with a thorough chemical EHS characterization including, but not limited to, environmental impacts, human health and toxicity hazards, and occupational safety considerations. This review builds upon the information compiled during GFM's development and supply chain efforts, and it extends analysis to site-specific environmental, health, safety, and waste issues. The GFM system dovetails with the EHS organization's program at this stage, resulting in a complete EHS materials program from concept to technology end-of-life.

CASE STUDY ON PERFLUORINATED COMPOUNDS (PFCs)

PFCs are key materials used for plasma chamber cleaning in chemical vapor deposition (CVD) and for plasma dry etch. They are also a group of materials that have been identified as having high Global Warming Potentials (GWPs) in reference to the GWP of carbon dioxide (CO₂). In some instances, these GWPs can be thousands of times higher than that of CO₂. The high GWP of PFCs led to a great deal of focus on the reduction of their emissions beginning in the late 1990s, and that focus is expected to continue for many years.

The reduction of PFC emissions was the first effort by the WSC to establish a voluntary agreement across the semiconductor industry. The goal was a 10% reduction in absolute PFC emissions from 1995 levels, by 2010. This required extensive collaboration between semiconductor manufacturers, equipment suppliers, materials suppliers, and research from universities and consortia. To develop the agreement and a roadmap for reductions also required collaboration within Intel between Government Affairs, Legal, EHS, Technology Development, and GFM-EHS.

The reduction efforts focused on the high-end of the pollution prevention hierarchy where reduce, reuse, and replace were the priority. The search for alternatives tied into another GFM-EHS strategic program, Environmentally Benign Materials Research (EBMR). Significant progress has been achieved over the past 10+ years in reducing emissions through the evaluation and integration of these environmentally benign materials into the manufacturing process. Using the screening process on new potential materials allowed for the selection of the best alternative, without replacing one environmental problem for another. The development of replacements came from a wide range of sources from universities to suppliers. However, the integration of these materials into the manufacturing process required significant work due to the complexity of making a chip.

Currently, Intel Corporation is on track to meet the voluntary goal for 2010 and continues to not only focus on opportunities for reducing emissions but inserting distinct requirements for reduction into future technology development roadmaps. This continues to push us to seek out new alternatives and methods for reductions.

CONCLUSION

The Intel Materials' environmental, health and safety early screening and materials management program has been implemented to ensure stability of the Fab materials supply-chain through identification and management of EHS-associated risks. This supports both Intel and semiconductor industry leadership in developing

environmentally preferable materials, protecting public health and the environment, and maintaining a safe and healthy workplace, while continuing to enable new technology.

ACKNOWLEDGMENTS

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Our EHS-focused colleagues and managers from many organizations at Intel who participate in and support the efforts to meet the objectives of this process successfully.

Fellow travelers in the semiconductor industry—Manufacturers, Suppliers, Researchers and Educators—without whose common vision none of this would be possible.

REFERENCES

- [1] See <http://www.intel.com/technology/mooreslaw/index.htm>
- [2] Joel Tickner, Carolyn Raffensperger, and Nancy Myers, *The Precautionary Principle in Action: A Handbook*, at <http://www.biotech-info.net/handbook.pdf>
- [3] <https://supplier.intel.com/static/EHS/materials.htm>
- [4] Background information on Copy Exactly!, at http://www.intel.com/pressroom/kits/manufacturing/copy_exactly_bkgrnd.htm

AUTHORS' BIOGRAPHIES

Victor S. Fan is a Senior TD Materials Engineer with Strategic EHS Programs in Intel's Global Fab Materials (GFM). His experience with Intel includes chemical EHS characterization, business program establishment, and as an Intel representative to SEMATECH. Experience outside Intel includes engineering and management positions in petrochemical and health care industries. He received an M.S. degree from Harvard University and a PhD degree from Johns Hopkins University.

David Harman is a Senior Environmental Engineer in the Intel Technology Development EHS Group. He works on a variety of strategic and technical programs to support materials, equipment, and process development of new technologies. He also is the Intel representative to Sematech EHS programs. He has a B.S. degree in Chemical and Environmental Engineering from the University of Arizona.

Jim Jewett is a Principal Engineer and Manager of Global Fab Materials' (GFM) EHS group, whose responsibility is to ensure that Fab materials provide cost-effective environmental and health solutions in their

design and selection, while enabling Fab process technologies and maintaining a secure supply chain. In addition to the internal responsibilities, Jim chairs both the Chemical (EHS) Management program for the World Semiconductor Council and the International Technical Working group on EHS for the ITRS (International Technology Roadmap for Semiconductors). He is Intel's Industrial Advisory Board member to the SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor manufacturing. During his 23 years at Intel, Jim has remained focused on environmental programs while belonging to a variety of organizations including Corp EHS, Fab Manufacturing, Components Research and Materials.

Robert (Bob) Leet is a Senior TD Materials Engineer at Intel Corporation, in Portland, Oregon, USA. He holds a Bachelor's and Master's degree in Chemical Engineering from Arizona State University, his Master's degree focusing on Semiconductor Processing and Manufacturing. He has a specialty in Environmental Health and Safety business processes and information systems for Intel's Global Fab Materials organization. He is the holder of four patents and has four patents pending for semiconductor devices as well as waste treatment technology. He has published several industry-forum papers related to both corporate responsibility and government regulatory topics. Bob is a founding member of the EICC (Electronics Industry Citizenship Coalition) and participates in several working groups within the semiconductor and electronics industries.

Dawn E. Speranza has held various positions in the EHS field and is currently a Senior TD Materials Engineer and REACH program manager for the Intel Global Fab Materials EHS group. Prior to this, Dawn was on assignment at International SEMATECH where she managed various global chemical initiatives and EHS assessments of new materials and processes for advanced technologies. She also worked at the Intel Hudson facility in Construction Safety, Mergers and Acquisitions, Industrial Hygiene, and Occupational Safety. She has a B.S. degree from Tulane University and an M.S. degree from the University of Massachusetts at Amherst. Dawn is a certified Industrial Hygienist and Safety Professional. She currently holds the position of president elect on the SSHA (Semiconductor Environmental, Safety and Health Association) board of directors.

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ENDNOTES

¹ Silicon wafers are a thin disc of pure silicon upon which up to a couple of thousand semiconductor die can be manufactured simultaneously. Afterwards, the discs are cut apart into a single die in preparation for the package-assembly and test process steps, before finally being shipped to end users.

² Etching is the process of removing material from predefined areas of the surface of a wafer. Deposition is the building up of material on the wafer surface.

³ Lithography is the process of transferring an image from a pattern onto a surface by using light. In the manufacture of semiconductors, it is the process that predefines the device features on the silicon wafer prior to the etch process steps.

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