Volume 11 Issue 02 Published, May 16, 2007 ISSN 1535-864X DOI: 10.1535/itj.1102.01

Intel® Technology Journal

The Spectrum of Risk Management in a Technology Company

Managing New Technology Risk in the Supply Chain

Managing New Technology Risk in the Supply Chain

Janice Golda, Technology and Manufacturing Engineering, Intel Corporation
Chris Philippi, Technology and Manufacturing Engineering, Intel Corporation

Index words: supply chain, risk management, lithography, R&D investment

ABSTRACT

How do we decide to make strategic bets on multiple, sometimes competing technologies across a portfolio of technology options to maximize our potential for success? Ideally, we can minimize risk by investing in technologies that enable multiple competing technology options; however, not all critical capabilities fall into this category. Investment in orthogonal options must be judicious, as high-risk, high-reward, long lead-time developments will likely also be high cost. In some cases, these larger investments may enable the desired option or a competing option. As long as at least one technology option is available when needed, the investment is ultimately successful. Finally, there may be unique capabilities that may be under-funded, where a nominal investment can enable a technical linchpin.

In this paper, we examine a method to make these strategic bets in the lithography supply chain. We start by looking at a system to assess technical and business risk for all components of the supply chain as they evolve over time. We discuss a methodology for identifying fellow travelers, including consortia, to create programs to establish a foundation of common technologies. We discuss the contractual and competitive aspects of creating investment and joint development programs, with the ultimate goal of improving our probability of success in delivering the right technology at the right time in high volume.

INTRODUCTION

Intel competes in an extremely efficient market. Overinvestment in research and development will compromise product margins, while conversely, underinvestment will likely result in the competitive catastrophe of missing a technology node. Historically, Intel has been successful in making the most strategic, and often most expensive, technology decisions at the last possible moment by ensuring that multiple options were available. Enabling the readiness of multiple options is becoming increasingly difficult in the lithography area with the demise of "simple" scaling. The complexity of developing an equipment and materials infrastructure to support high-volume manufacturing (HVM) while solving fundamental physics problems can cost billions of dollars. It is imperative that we make strategic bets to create the right technology options at the right time, lest there be an unaffordable spike in R&D costs each time a new lithography generation is introduced.

The nature and scope of the strategic bets in the lithography supply chain differ dramatically between evolutionary and revolutionary technology transitions. For evolutionary technologies, the proposed approach is relatively straightforward, albeit often expensive. Development-level capability is brought in house as soon as possible in order to begin characterizing the issues in integrating the new technology into existing processes and starting the yield learning cycle. This prepares Intel for HVM of the new technology. Evolutionary changes require very few nontraditional strategies beyond buy-sell supplier relationships.

For revolutionary technologies, efforts must begin far in advance, sometimes 10-15 years, of the anticipated high-volume ramp of the new technology. In this case, engagement can start as early as the proof of concept. The scope of engagement must span practically all aspects of the technology, as traditional buy-sell relationships with payment upon delivery of goods often do not meet the needs of the supply chain. Figure 1 illustrates this dramatic difference in scope between evolutionary (193nm) and revolutionary (Extreme UltraViolet–EUV) lithography development, spanning eleven critical aspects of the technology covering the lithography and mask equipment, chemicals, materials, and defect control.

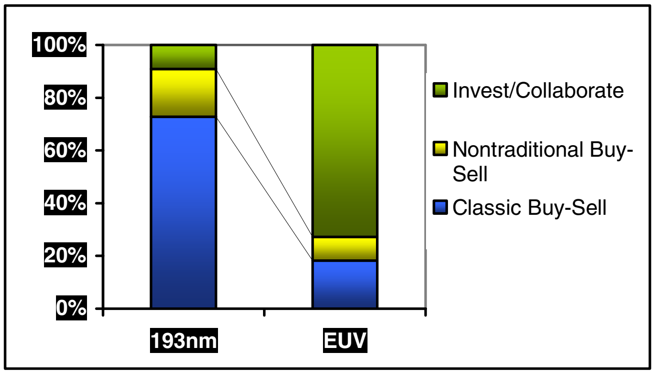

Figure 1: The nature of supply agreements for 11 key lithography component technologies differs dramatically for an evolutionary 193nm transition vs. a revolutionary EUV transition

As part of moving to a revolutionary technology, a thorough risk assessment needs to be completed (and continually updated based on new information). Using the EUV lithography technology as a case study for the strategies discussed, we examine successful business engagements as well as lessons learned from the unsuccessful ones, and we show the importance of effective R&D funding and product strategies to survive the "Valley of Death" encountered prior to high-volume adoption of a new technology. The "Valley of Death" is the process of transitioning from R&D to the commercial market. If a company spends so much money during the R&D phase to develop a technology, it may put itself out of business before it has a chance to commercialize the product [1].

Evolutionary Versus Revolutionary Technology

Intel has always pursued multiple approaches for each lithography generation, with the final decision for each generation being made roughly two years prior to high-volume ramp.

The first approach under consideration is typically evolutionary: enhancing the existing technology. In the case of lithography, evolutionary enhancements have included higher numerical aperture lenses, improved photoresists, optical proximity correction, phase shift masks, and design for manufacturability improvements. Generally, an evolutionary technology has fewer technical risks than a revolutionary technology, so suppliers and customers endeavor to extend existing technologies as long as possible with only incremental research and development costs.

The alternative approaches under consideration are often revolutionary, requiring the commercialization of new inventions in a number of areas. In the case of lithography, transitioning to a shorter wavelength has been mostly evolutionary to this point. However, future changes will likely be revolutionary, as they can require new hardware architecture, new optical designs and materials, and new resist chemistries. Switching to a revolutionary technology increases the overall technology risk since there are more, and often new, major problems that need to be solved. The uncertainty in the time needed to solve these new problems increases the risk to the technology delivery schedule, which consequently increases the business risk to both the supplier and the customer. This is because most customers are not willing to make solid financial commitments when the delivery time is unknown.

Given these risks, there is a natural desire to extend the existing technology as long as possible, until it reaches a capability wall or the cost/complexity of evolution becomes unaffordable. For lithography, the evolutionary approaches currently under consideration require increasing product layout restrictions and can also require multiple process steps thereby increasing the cost of ownership and the manufacturing cycle time. The revolutionary shift can only occur when the new technology is ready to deliver layout, cost, and/or cycle time advantages. In this paper we explore how to enable the supply chain to deliver the new technology, rather than assessing when the old technology has run its course.

Infrastructure Risk Assessment

Technical Risk Assessment

Multiple methods exist to assess a project's technical risks, and Intel has often used some combination of the following approaches to manage technical risk:

1. *"Stoplight" chart*: Classifies risk areas into three categories: red (potential showstopper/invention required), yellow (development required), and green (path demonstrated).
2. *Intel risk scorecard*: A 5-point scale, ranging from a score of 1 for invention required to a score of 5 for HVM ready. This is a slightly higher resolution version of the stoplight chart.
3. *Sematech Relative Orders of Magnitude Improvement (ROMI)*: This assesses the order of magnitude of improvement required for key performance components of a new technology. These are summed to calculate an overall risk rating.

Regardless of the tool used, it is critical that the inputs come from a variety of content experts with different perspectives on the technology to minimize blind spots. It is also critical to examine risk reduction over time to determine if the components of the technology are converging to be ready in time. The end result of the technical risk assessment as it pertains to the supply chain is to identify the critical areas where the supply chain must dramatically improve to deliver a revolutionary technology.

Business Risk Assessment

Evolutionary and revolutionary development differs in the required R&D funding and time to Return on Investment (ROI). Figures 2 and 3 illustrate this point, showing that on a revolutionary technology, the development cycle is significantly longer and the costs of development are larger. This, coupled with fewer firm commitments from customers, puts suppliers in a difficult position regarding ROI. Where a company's initial investment cost is high and its ability to make money is far in the future, there is a risk that the company might reach bankruptcy prior to delivering its product.

In our experience, the fear of the "Valley of Death" has caused larger, more established companies to delay their investment so they can hit the sweet spot of the market where the bulk of their customers will adopt the new technology. Additionally, large, established suppliers need to balance the innovation and timing of new technology with the potential cannibalization of its existing technology. Often, this does not meet Intel's goal of being the leader in introducing new technologies on a two-year cycle. Consequently when switching to a revolutionary technology, it may be necessary to take calculated risks and engage with suppliers who are not currently in the market but are aggressively trying to enter it. Often, these are small startups with limited cash reserves, so it is essential that suppliers have strategies to both raise funding from outside sources and adeptly manage their revenue and expense streams. An additional benefit that may occur by engaging with these smaller or newer suppliers is that it may encourage the incumbent to start its efforts earlier than it would have otherwise, in order to head off a competitive threat.

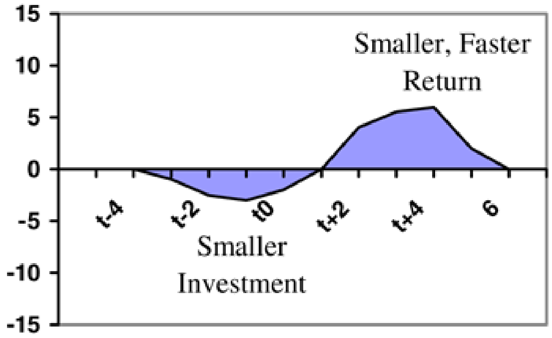

Figure 2: "Valley of Death" for an evolutionary technology. The investment lead-time is shorter, time to return is faster, but longevity of return is limited.

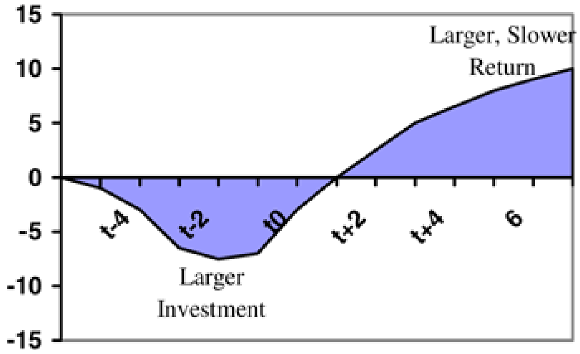

Figure 3: "Valley of Death" for a revolutionary technology. The investment lead-time is long, market adoption takes longer, but ultimate rewards are larger.

A compounding issue when contemplating a revolutionary technology is the "ecosystem risk," i.e., there is additional risk because all links in the supply chain need to be in place for success, or it may be the case that a deficiency in one area increases the burden on another. The chain is only as strong as its weakest link. For example, if a supplier develops a production-worthy lithography exposure tool but product masks are not available due a technology hurdle not yet solved, the lithography tool is, for the most part, useless. In this case, the mask hurdle impacts the mask equipment suppliers, mask making suppliers, and also the lithography tool maker. This highlights the importance of leaving no stone unturned in assessing *all* components of the technology.

The end result of the business risk assessment as it pertains to the supply chain is to identify the critical areas where the supply chain needs financial stimulus to deliver an innovative technology.

Before moving on to funding strategies in the "Strategy" section of the paper, we want to mention two approaches to manage cash flow that are within a small supplier's direct control, and these are areas that Intel evaluates when determining if a small supplier is managing itself wisely:

1. Standards/use of standard components/subsystems.

   Suppliers can minimize R&D costs by using existing standards and/or standard components and/or subsystems where appropriate rather than inventing every component or subsystem. Otherwise, the investment required to develop non-differentiating components may mean the difference between surviving or not surviving the "Valley of Death." This may require smaller suppliers to develop industry-savvy and influencing skills to drive standards-setting efforts and to understand their supply chain.

2. Identifying applications with shorter time-to-ROI.

   Suppliers engaging in revolutionary technology development can opportunistically find alternative, earlier production uses for the supplier's product. This can be a win for the supplier to be able to generate revenue sooner and collect field data to understand product performance, albeit sometimes in a less taxing environment relative to the ultimate requirements. Alternatively, some components of revolutionary technology development may enable evolution of a current technology, also generating revenue for the supplier. It is important in both cases that the alternative uses do not overly distract from reaching the end goal.

The above approaches help to minimize and smooth the "Valley of Death," but in some critical cases, dramatic actions are necessary.

RISK MITIGATION STRATEGIES

The risk assessment described above identifies technical and financial gaps that must be closed to deliver new technology when needed. If Intel expects to be a leader in adopting new technology, it is necessary to be a leader in driving the strategy to enable technology readiness.

If the technology is in an evolutionary phase, the primary method of help is by making commitments through a traditional buy-sell relationship. Purchasing an early tool, utilizing it in a development pilot line environment, and providing feedback so that the supplier can incorporate improvements into the production version of the tool are the quickest route to production capability. The earlier the influence Intel can provide at this stage, the more likely the tools will meet Intel's needs in HVM. To the extent there are specific areas of concern for the industry regarding the next-generation technology, the industry can work on development plans through avenues such as Sematech.

Intel has found the following strategies important in enabling revolutionary changes across our supply chain:

<u>Risk Mitigation Strategy # 1:</u> Know when to engage others.

History has shown that for major, revolutionary technology changes, supporters are needed, both from a supplier and customer basis. For nearly 30 years, a leading IC company worked on a lithography solution called 1-X X-ray. On top of several technical hurdles, there was really only one company supporting the concept. There was no support from major lithography suppliers and little interest from other IC manufacturers. Developing the technology in isolation failed to develop the needed infrastructure, and also failed to engage the equipment expertise of lithography suppliers.

At times, an evolutionary technology may need to incorporate one revolutionary component. For this situation, a company may find expertise in universities or national labs to explore the Proof of Concept (POC) on the revolutionary piece of the technology, or if the core expertise lies within the company's walls, the company may be able to develop a significant competitive advantage if the POC is successful for relatively low cost.

Alternatively, if the supply chain requires many revolutionary changes, forming pre-competitive alliances with suppliers and customers to pool expertise to demonstrate POC can help in engaging the entire ecosystem. In this alliance, IC manufacturers, tool makers, sub-component manufacturers, and peripheral technology manufacturers (in the case of lithography, the mask and resist manufacturers) can work together to solve the basic, fundamental problems of the technology. POC is a minimum requirement to get larger industry participation and investment. Once the POC has occurred, the alliance could continue to work together to drive the industry to develop a pre-HVM capability or it could disband.

Table 1 summarizes the considerations for developing a technology internally versus engaging the supply chain.

Table 1: Make vs. buy considerations

Competitive Advantage	High	Engage suppliers (See Table 2)	Make
	Low	Buy	Buy (usually)
		Low	High
		Internal core competency	

<u>Risk Mitigation Strategy #2:</u> Look for extendable solutions.

Developing a revolutionary technology, even after completing a thorough risk assessment, generally takes longer than originally anticipated. Some issues will be relatively minor while others may be showstoppers, or at a minimum, significantly delay development. Technology integration issues often extend the development cycle, often late in the process. For this reason, plus the fact that as the industry resists going to a revolutionary technology whenever possible, it is important to choose a technology that is extendable to accommodate future requirements.

Risk Mitigation Strategy # 3: Evaluate multiple options to enable commercialization.

Even though POC may have been achieved, experience tells us that going from POC to HVM commercialization, brings significant challenges. It is important to continually assess the risks until HVM happens. As part of the ongoing assessment, Intel has looked for potential competitive or financial opportunities as it evaluates the technology and enables the supply base. If an area of the technology is determined to be especially risky (remember, all of the parts of the technology need be achieved at the same time or else the entire technology will be gated by the missing piece), it is imperative to identify what is needed to close the gaps.

If funding and resources appear to be the solution, it is necessary to evaluate the potential return of engaging with suppliers to drive a solution. If the financial return is low or there is little competitive advantage to be gained; yet, the risk is still high for developing this piece of the technology, engaging industry consortia, such as Sematech, to address the issue, can be a way to reduce the infrastructure risk while sharing the costs across the industry.

For Intel, if the assessment of the possible commercial and financial returns of engaging directly with a supplier(s) working in the risky area turned out to be high, we have used a number of options to help drive a solution while at the same time gaining a competitive advantage.

1. *Financial Investment*. Sometimes a cash infusion would benefit a supplier working in the risky area. This could be accomplished through a direct investment in return for equity in the company, through a loan, through warrants, or other venture-capital mechanisms. This cash infusion to the supplier working on the risky area can enable it to hire new people, invest in facilities and equipment, and engage with other experts (universities, national labs, or others) to accelerate learning to deliver the revolutionary technology. This is typically not done for philanthropic reasons, but rather to receive a financial return on its investment if the supplier is successful.
2. *Collaboration/Joint Development*. Sometimes direct collaboration between Intel and the supplier can solve the problem. Approaches used to date have included providing data to the supplier on their product performance to increase the learning rate, committing to purchase the product if the program is successful, providing expertise to fill gaps, providing cash to fund engineering programs, licensing Intel Intellectual Property (IP), or a combination of any of these. Of course, these would be done in exchange for some direct benefit to the customer, such as better commercial terms on the product, early access to the product, or financial return, possibly in the form of royalties.

Table 2 summarizes our model for considering supplier funding options, and has been used in the Intel Technology Manufacturing Engineering (TME) organization over the past several years to determine courses of action. The case studies following show how this model is used to enable EUV lithography technology.

Table 2: Supplier funding options model

Competitive Advantage	High	Collaboration/JDP	Financial investment + Collaboration/JDP
	Low	Consortia	Financial investment
		Low	High
		Financial ROI	

CASE STUDY: EXTREME ULTRAVIOLET LITHOGRAPHY

Over the last 15 years, the lithography wavelength has evolved from i-line (365nm) to DUV (248nm) to 193nm, which is entering its third generation of production with the 45nm node in 2007. Lithography suppliers and sub-suppliers have been working with the same basic refractive optical design all these years: they use transmissive photomasks and have refined the equipment, materials, and patterning techniques over time, with somewhat isolated revolutionary changes, such as chemically amplified resist, along the way. In this model, normal supply and demand market conditions dominate the majority of the interactions. Suppliers and sub-suppliers assume the majority of risk and fund development from the previous generation's sales. Additionally, as the development approaches commercialization, the suppliers receive purchase orders from customers to reduce its business risk. The rest of the infrastructure, such as masks, is evolutionary also. The interdependence risk of the infrastructure is significantly lower in an evolutionary technology.

As Intel lithographers look at Intel's future requirements, it is becoming clear that there will be physics and material limitations to a purely evolutionary approach at some point. As the lithography wavelength shrinks, more materials absorb the light, few materials can refract or bend the light, and the high photon energy breaks many common chemical bonds, making further evolution difficult.

Development of 157nm lithography demonstrated this complication. The industry spent significant money trying to continue along what was initially assessed to be an evolutionary path. This initial assessment did not account for a revolutionary fact realized too late. The lens materials, in addition to being extremely difficult to produce at acceptable yield, exhibited a phenomenon called intrinsic birefringence. This initially produced confusing optical data on the first lenses measured, and it ultimately delayed programs by roughly one year as the discovery mandated the redesign of the lenses. Additionally, the industry had generally recognized that 157nm would be a one-generation technology, intended to fill the gap between 193nm and EUV, rather than being an extendable approach that would be an option for generations to come. When the material issues arose and delayed the program, there was not time to develop the revolutionary material to satisfy the requirements and meet the market window for the technology. This cost the entire industry hundreds of millions of dollars and distracted resources from working on other multi-generational approaches. Because it was generally thought that 157nm was going to be an evolutionary extension, the strategies discussed above were not implemented or followed. When it was realized that there was a revolutionary component to the technology, it was too late to implement proper risk mitigation strategies to ensure a timely success.

Fortuitously, while working on 157nm lithography, the equipment suppliers also initiated small-scale research programs to assess whether 193nm immersion lithography, using water between the bottom lens element and the wafer, might be a feasible approach to further extend 193nm. This technology currently appears to contain one revolutionary component, the lens fluid, making the development feasible on a shorter time horizon. 193nm immersion appears to fill roadmap gaps in the industry, starting with the 45nm node for many companies. Further extension may be possible using complex mask and multi-step patterning approaches.

As Intel evaluates the 22nm node and beyond, it is unclear that extensions of 193nm immersion coupled with new revolutionary techniques will continue to meet device scaling and affordability requirements (Figure 4). For this reason, Intel is continuing to evaluate a revolutionary technology and evaluate the needs of the overall infrastructure.

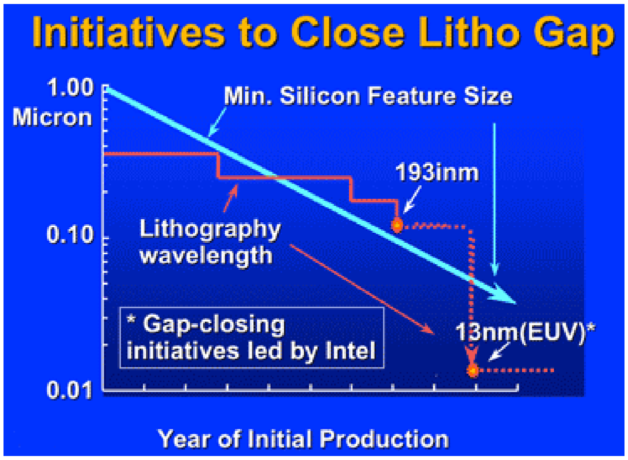

Figure 4: The large leap required from the current evolutionary path (193nm immersion) to the revolutionary path of EUV to maintain Moore's Law

EUV Proof of Concept: The Mid 1990s

In 1996, the US government discontinued funding for the Star Wars weapons program at its National Labs. The scientists working on Star Wars had developed expertise in the EUV region around the 13nm wavelength. At the same time, people within Intel were trying to identify "the cliff" of traditional lithography and its extensions. The National Labs and Intel scientists discussed the potential application of EUV for lithography, and a technical assessment determined that using EUV in lithography could work although there were significant hurdles to overcome. Initially, there were seven potential showstoppers identified with the technology; if just one could not be solved, the entire technology would not be viable. This would be an implied revolutionary change for both the lithography equipment and materials supply chains.

EUV is revolutionary for many reasons. It requires reflective (vs. refractive) optics. It must work in a vacuum environment. High-volume production will require EUV light sources in excess of >180W with power levels inside the source >10 times what they are for a 193nm source today. It will require making reflective optics that can withstand this source power. It will require a reflective mask with tolerances never before seen. New ways of handling the mask will need to be developed due to the lack of a protective pellicle, and a new low expansion material will be required for the mask substrate. It requires a new, novel approach to resist. Lithography has never required so many simultaneous changes, all of which are revolutionary.

After it was determined this was a potentially viable, but revolutionary approach for the future lithography nodes, Intel determined five things:

1. A POC program should be developed at the National Labs where the technical expertise resided, with the learning and IP being transferred to industry.
2. A formal structure needed to be formed to manage the POC development program.
3. The program needed to be set up as a focused risk reduction program to address each module of the technology.
4. The program needed to work with the supply base (litho and litho subcomponents) so the learning would be transferred instantaneously.
5. The program needed to have other IC companies participate to show there was strong support from the customer base.

The above requirements led Intel to conclude that the consortia model would work best in this phase of the technology, and the Extreme UltraViolet Limited Liability Company (EUV LLC), a private consortium, was formed to accomplish these goals. An agreement was secured with the National Laboratories, Intel contributed its risk mitigation methodology and program management expertise, the EUV LLC enlisted two (out of four at the time) lithography suppliers to participate, and the EUV LLC secured five other leading IC manufacturers to participate in and contribute to the ~$300M program. The goal of the program was to develop and demonstrate EUV as a viable lithography option while enabling the infrastructure with the IP and know-how and at the same time sharing costs and risks across the membership. Figure 5 illustrated the Engineering Test Stand (ETS) built at the EUV LLC to demonstrate POC.

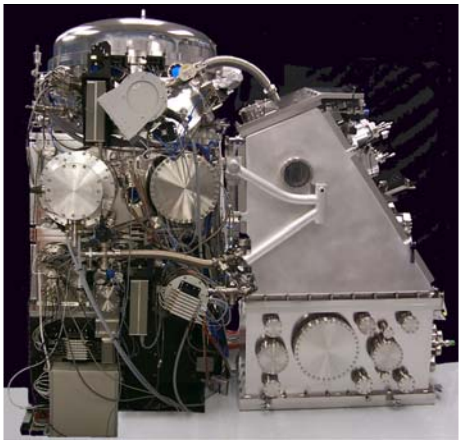

Figure 5: The EUV Engineering Test Stand, which demonstrated full field proof of concept for EUV

On a final note, the initial project timeline planned for this technology assumed that it could be ready for HVM in 2005 to intersect the 65nm node.

Infrastructure Challenges: Fast Forward to 2003

The POC was demonstrated in 2001. This was two years later than originally anticipated due to unforeseen technical issues and lower funding levels due to the general industry downturn. However, based on the success of the POC program, the industry accepted EUV as a leading candidate for “Next Generation Lithography” (NGL). This would not have happened if only a single IC manufacturer was supporting the technology in isolation. The six EUV LLC IC manufacturers then decided it was time to move from the pre-competitive to the competitive phase.

At that time, Intel reassessed the EUV lithography infrastructure and determined the two primary areas that were lagging behind the rest of the EUV infrastructure were the EUV light sources and mask materials/mask equipment. Intel then investigated numerous technical approaches being pursued for the light source and did an overall mask assessment to determine the final mask specs and the allocated error budgets for the mask blank and mask patterning. We then applied the supplier funding options model to determine the appropriate strategy to stimulate development in these areas.

Light Sources: Investment and Collaboration

Looking to both enable high power source capability for HVM and strengthen Intel’s competitive position on this critical technology, Intel had a collection of internal and external experts assess various approaches to the technology problem. Since there were many suppliers with many different approaches, we assessed each approach to determine which approaches might have the highest chance of success. Upon determining the most credible, we applied the supplier funding options model and decided to invest in two EUV source suppliers and fund a joint development agreement with a third supplier. All three of the proposed approaches were significantly different in the engineering risks. It was not anticipated that all three would succeed. However, given the risk level, it was best to work on accelerating all three approaches, pushing for at least one to be successful.

All agreements provide a financial return, a significant competitive advantage, or both, if the supplier is successful. Two of the agreements were with startups trying to enter a new market, while one was with an existing leader in the industry. Sources remain a key technical risk for EUV technology, so time will tell if the choice of funding models was optimal. Additionally, Intel continues to evaluate not only the suppliers it engaged, but also stays aware of the other potential solutions. If a previously dismissed approach makes substantial progress in the future, Intel can re-engage with the supplier.

Mask: Investment, Collaboration, and Internal Development

At the same time as Intel was assessing light sources, we were assessing the mask materials and equipment markets. We decided to do two things. The first was to develop the world's first full EUV mask pilot line. The plan was twofold: first, we needed to engage with suppliers to develop tools required to make a final EUV mask so that we could demonstrate to the industry it could be done while developing the industry infrastructure. Second, we needed to develop leading-edge capabilities and IP in-house before other companies did so.

Intel engaged with over seven suppliers to develop a pilot line. Assessment of supplier needs and application of the supplier funding model led to the decision to simply purchase tools in most cases, with some early funding being part of the deals. In one case, consortia funding helped to enable a standard tool purchase, while in another case, an equity investment was made in concert with a technical collaboration. Most of the tools have been delivered and excellent progress has been made on EUV mask making.

Out of this early involvement, we encountered both ends of the spectrum with regard to the "Valley of Death." Both suppliers were very small and signed up to deliver revolutionary, first-of-a-kind technology. The first worked in a disciplined fashion to meet schedules and worked closely with Intel engineers who were the expert users of the technology. The tool worked well when delivered, so the engineers on the program thought it might be backward compatible to existing optical mask making with some relatively minor changes. The supplier made the changes. The tool now works for both today's technology and EUV. The supplier has been able to start selling to other customers to quickly exit the "Valley of Death" and moreover was ultimately acquired by a larger company. The supplier funding model worked perfectly to deliver both a competitive technical advantage and a financial return on investment.

The second supplier was constantly late, would not engage with Intel as deeply as the first, started to have cash flow problems, requested an additional prepayment from Intel (with which Intel complied), but ultimately, the supplier went bankrupt. The second supplier was not well managed, practiced poor supply-chain management, and ultimately failed. In this case, the funding model chosen was probably appropriate. Unfortunately, in hindsight, the development complexity was underestimated: the problem was realized too late due to lack of indicators, and hence the funding was insufficient. This has led us to reconsider additional techniques to monitor the financial health of small, privately held companies, such as more frequent management review meetings (vs. just technical review meetings), more involvement from the Intel finance community to assess the ongoing financial situation of these suppliers, and instituting a "continuous reassessment" of the suppliers that fit this category.

Mask Materials: Investment and Collaboration

The second area Intel felt it necessary to engage in was that of mask material suppliers. Intel finalized two joint development agreements with materials suppliers. In one case, we decided to apply the supplier funding model to provide nominal funding along with technical expertise, as there was an opportunity for both technical and financial advantage. In the case of the other supplier, we provided technical expertise and data from the EUV mask pilot line. Both development projects have made tremendous progress, but still have some technical hurdles to clear to be ready for HVM. Initially, we attempted to engage with the large, incumbent material supplier, who had the majority of the market share. The supplier, for a variety of reasons, did not want to engage with Intel at that time. We engaged with the other, newer supplier and after some solid results were publicly announced, the incumbent increased its development effort. If both the suppliers are successful, these interactions will have enabled a dual supplier strategy for Intel to drive future capability and cost benefits.

DISCUSSION

The case study provides examples of "Risk Mitigation Strategy #1," knowing when to engage others, and illustrates the point that it is necessary to engage people or organizations with different competencies at different times in the research and development cycle. Engaging the National Labs and other IC manufacturers enabled acceptance of the technology as a viable option rather than as a research curiosity. The mask example also illustrates the extreme ramifications of "partially" engaging and not sharing information critical to technical or financial success. The case study does neglect one major incorrect assessment. During 1997, when the assessment was done, it was assumed that the future would be similar to the past. That is, traditionally, microprocessor companies adopted leading-edge lithography first and memory makers followed so the EUV LLC focused its efforts on attracting other microprocessor companies to join the EUV LLC versus memory companies. Today, microprocessor companies and memory companies adopt lithography at roughly the same time, and memory companies may start adopting new lithography even more quickly than microprocessor makers in the future. For this reason, having a larger group of memory makers in the EUV LLC likely would have been better for the EUV technology as it would have captured more of today's early adopters.

Regarding "Risk Mitigation Strategy #2," pursuing extendable solutions, when the initial program was created as part of the EUV LLC, it was anticipated to be an eight-year program from its inception to the delivery of the first HVM tool. It turned out, like many revolutionary technologies, to present greater challenges than initially anticipated and took longer and cost more than initially anticipated. The extendable nature of the technology has meant that a technology that was originally targeted for a 65nm insertion in 2005 is still a leading candidate for insertion for HVM at 22nm starting in 2011, more than six years later than originally planned. While the delay was not intended, it was not surprising since the industry as a whole will almost always push to solve the evolutionary challenges and extend the current technology for as long as possible, attempting to postpone the shift to a revolutionary change. Because Intel always assesses multiple approaches, even while Intel was investing and driving the EUV infrastructure, it was in parallel pushing for the solving of the issues on the evolutionary technology.

Moving on to "Risk Mitigation Strategy #3" regarding POC being the easy part, the prolonged development of the technology and infrastructure driving toward HVM does show that this is the harder part and requires commitment and judicious program and business management to have a chance at success in the end. In the EUV example above, it took ~four years to achieve the initial POC, but HVM is not planned to start for ~ten years after the initial POC was achieved.

During the time between POC and HVM, Intel has continued its learning of the technology through the continued interactions it has established with the supply base and its continued internal work on masks and process development. This, coupled with the competitive advantages captured in the commercial agreements, should allow Intel to insert and exploit EUV as a technology sooner and easier than other IC companies.

CONCLUSION

Intel has many relationships within the corporate world. Intel purchases equipment from suppliers, sells components to customers, enables new industries that require more processing power, and influences the industry to set standards. As the IC world continues to evolve, Intel will need to continue to be creative in its approaches. Where appropriate, we can be a leader in both shaping the world of silicon while securing a competitive advantage. Recognizing where business as usual may not achieve success or meet timing goals, we can exert our considerable influence and use our resources to help drive the industry and enable revolutionary approaches. In this paper, we discussed some of the key strategies Intel has applied to help enable a new, revolutionary technology, while at the same time generating industry support.

We looked at just one example, lithography, of a revolutionary approach. Intel, to date, has invested nearly $500M championing a new, revolutionary lithography option that will allow us and the industry to maintain Moore's Law for several more generations of lithography. In 1997, when we started this endeavor, EUV was not on any supplier's or any IC company's roadmap.

After a careful assessment of both the technology and business, we took a unique approach in forming a consortium of chip makers, tool makers, and infrastructure suppliers and demonstrated this technology could be applicable for manufacturing. Lithography equipment and materials had historically been capabilities that Intel purchased through traditional buy-sell relationships because, while lithography is key to the manufacturing of integrated components, it is not a core competency of Intel's. The investment and industry coordination has helped place this technology on the roadmaps of many equipment suppliers, infrastructure suppliers, and integrated circuit manufacturers. This program required us to take a huge risk, but our methods described in this paper have helped to mitigate both the capability and business risks while also providing capabilities that improve today's processes.

REFERENCES

[1] Evan Mills and Jonathan Livingston, "Traversing the Valley of Death," Forbes, November 17, 2005, p1.

AUTHORS' BIOGRAPHIES

Janice Golda is the Director of Lithography Capital Equipment Development (LCED). She manages an organization responsible for creating strategies and working with Intel's lithography suppliers and sub-suppliers to deliver equipment meeting Intel's technology, capacity, and cost roadmap requirements. Janice represents Intel on the Sematech Lithography Program Advisory Group and the US Lithography Technical Working Group. She joined Intel in 1989 and has held positions in lithography process engineering and program management. Janice received a B.S. degree in electrical engineering from Cornell University. Her e-mail is janice.m.golda at intel.com.

Chris Philippi is the EUV Commercialization Manager for Lithography Capital Equipment Development (LCED). Chris has been with Intel for nearly 16 years. He has held a variety of positions in finance and operations. He has been in LCED for 9 years, first as business manager for the EUV LLC, followed by Intel Mask Operations Commercial Manager and more recently EUV Commercialization Manager, in charge of driving the industry adoption of EUV. Chris graduated from Santa Clara University with a B.S. in finance. His e-mail is chris.s.philippi at intel.com.

BunnyPeople, Celeron, Celeron Inside, Centrino, Centrino logo, Core Inside, FlashFile, i960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel Core, Intel Inside, Intel Inside logo, Intel. Leap ahead., Intel. Leap ahead. logo, Intel NetBurst, Intel NetMerge, Intel NetStructure, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel Viiv, Intel vPro, Intel XScale, IPLink, Itanium, Itanium Inside, MCS, MMX, Oplus, OverDrive, PDCharm, Pentium, Pentium Inside, skoool, Sound Mark, The Journey Inside, VTune, Xeon, and Xeon Inside are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

Intel's trademarks may be used publicly with permission only from Intel. Fair use of Intel's trademarks in advertising and promotion of Intel products requires proper acknowledgement.

*Other names and brands may be claimed as the property of others.

Microsoft, Windows, and the Windows logo are trademarks, or registered trademarks of Microsoft Corporation in the United States and/or other countries.

Bluetooth is a trademark owned by its proprietor and used by Intel Corporation under license.

Intel Corporation uses the Palm OS® Ready mark under license from Palm, Inc.

Copyright © 2007 Intel Corporation. All rights reserved.

This publication was downloaded from
http://www.intel.com.

Additional legal notices at:
http://www.intel.com/sites/corporate/tradmarx.htm.

For further information visit:
developer.intel.com/technology/itj/index.htm