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Nano and Micro Technology-Based Next-Generation Package-Level Cooling Solutions

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ABSTRACT

The design requirement for electronics cooling is to maintain the hottest location (hotspot) on the die (chip) below the specified temperature. Due to the presence of multiple hotspots, the thermal resistance near the die is very high. Total thermal resistance (Ψ_{tot}) can be written as:

$$\begin{aligned}\Psi_{tot} &= DF \times (R_{si} + R_{TIM1} + R_{spreader}) + \Psi_{TIM2} + \Psi_{sink} \\ &= DF \times (R_{package}) + \Psi_{TIM2} + \Psi_{sink}\end{aligned}\quad (1)$$

where $R_{package}$, R_{si} , R_{TIM1} , and $R_{spreader}$ are the thermal impedances of package, silicon, first-level Thermal Interface Material (TIM), and heat spreader, respectively. Ψ_{TIM2} and Ψ_{sink} are the thermal resistances of second-level TIM and the heat sink, respectively, and Density Factor (DF) is a factor that accounts for the non-uniformity of heat generation. DF can possibly be greater than 1 if highly non-uniform power distribution exists or if the die size is very small. Since the thermal impedance near the die ($R_{package}$) gets multiplied by the DF, any reduction in the package impedance results in a larger reduction in Ψ_{tot} . Because of this reason, the focus of next-generation electronics cooling is on developing efficient cooling solutions near the package. Futuristic cooling solutions may be based on micro and nano technologies. These solutions might include a TIM made from micro and nanoparticles, a microchannel heat exchanger, and a Thin Film Thermoelectric Cooler (TFTEC) that is made of thin film superlattices, or nanocomposites, placed directly above the hotspots to provide localized cooling. In this

paper, we focus on the technical merits of these technologies and discuss the challenges that must be met to make these technologies a reality for electronics cooling. The main challenges are: a) to reduce the boundary resistance between the nanoparticles and the host medium for nanoparticles-based TIMs and to increase the reliability performance of TIMs; b) reduce the assembly-related parasitic effects seen in TFTEC (for example, due to the very thin dimension of TFTEC, electrical contact resistance reduces the effective ZT in a package making it much smaller than the intrinsic ZT); and c) pumping requirements and pump reliability for microchannels. Water cannot be used as a coolant because the freezing requirements for electronics cooling is dictated by shipping and handling requirements and is much lower than 0°C. Traditional antifreeze liquids have much lower thermal conductivity and higher viscosity than water, forcing very severe pumping requirements in order to get the same thermal performance as water.

INTRODUCTION

Over the past decade, thermal design for cooling microprocessor packages has become increasingly challenging, as silicon technology has continued to scale in accordance with Moore’s Law. Figure 1 shows the 2004 update of the International Technology Roadmap for Semiconductors (ITRS).

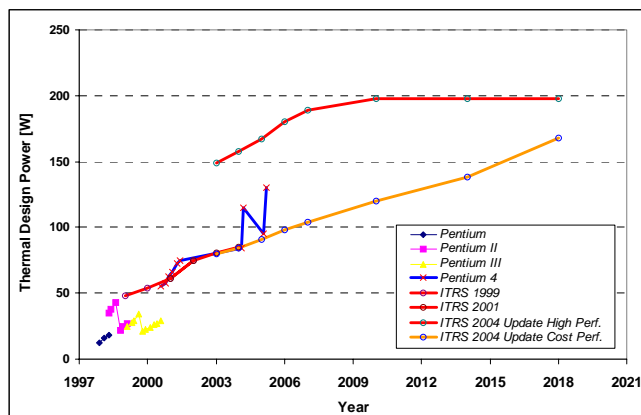


Figure 1: ITRS roadmap(s) and CPU historical data for high-performance computers

It can be seen that Thermal Design Power (TDP) rises linearly up to approximately the year 2009-2010 and will remain approximately constant afterwards. However, these data do not show if new cooling technologies are needed for future packages. Due to die shrinkage and other complexities of the microprocessor design, there is a possibility of increased local power densities, leading to highly non-uniform heat generation that will cause localized hotspots. Figure 2, taken from Watwe and Viswanath [1], shows a typical power map from a chip. The cell area in Figure 2 is 1×1mm. The package thermal cooling solutions must ensure that the junction temperature of the processor (die temperature) must be within the 90-110°C range, especially at the hotspots, in order to ensure device performance and reliability.

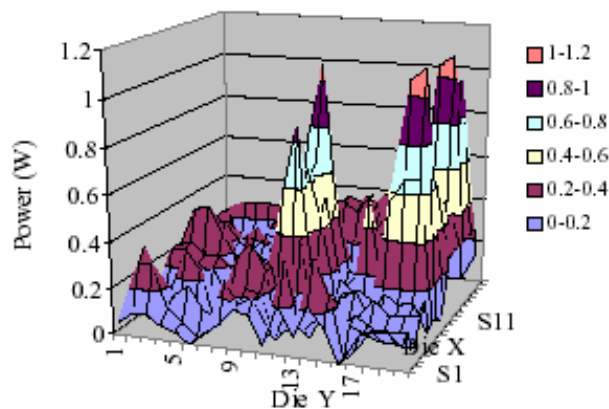


Figure 2: Example of non-uniform power distribution

The majority of Original Equipment Manufacturers (OEMs) within the microelectronics industry would like to further extend the application of air-cooling technologies. However, it was already shown in [2] that the current air cooling technologies present diminishing returns. Therefore, it is strategically important for the microelectronics industry to establish the research and development focus for future non air-cooling technologies. For a better understanding of the cooling capability for different thermal solutions used in CPU cooling, we use the concept of Density Factor (DF) proposed for the package performance by Torresola et al. [3]. This metric can be used to quantify the impact of non-uniform die heating on thermal management for a specific package. The advantage of using this metric is its ability to provide a better comparison of the impact of different power maps and die sizes on a specific package-based thermal management technology. Figure 3 shows the location of the temperature measurement for junction and case (lidded-type packages).

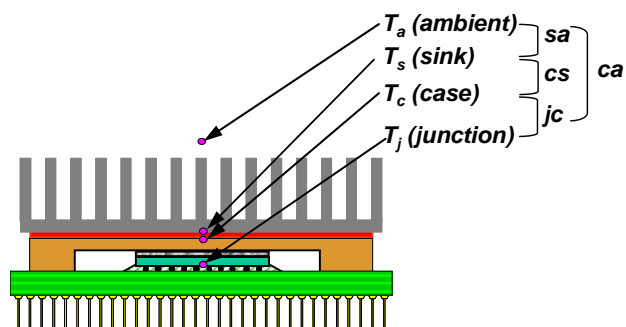


Figure 3: Lidded package and heat sink

Based on Figure 3 temperatures, the junction-to-case DF for a package is defined as:

$$DF_{jc} = \frac{\Psi_{jc}}{R_{package}} \tag{2}$$

where Ψ_{jc} ($^{\circ}\text{C}/\text{W}$) is the thermal resistance from junction to case and R_{package} ($^{\circ}\text{C}\text{-cm}^2/\text{W}$) is defined as the thermal resistance normalized by die area, when the die is uniformly powered. R_{package} is given by:

$$R_{\text{package}} = R_{\text{si}} + R_{\text{TIM1}} + R_{\text{spreader}} \quad (3)$$

where R_{package} , R_{si} , R_{TIM1} , and R_{spreader} are the thermal impedance of package, silicon, first-level Thermal Interface Material (TIM) and heat spreader, respectively.

Another important metric used for the cooling technology comparisons is the sink-to-ambient resistance:

$$\Psi_{\text{sink}} = \frac{T_s - T_a}{P} \quad (4)$$

where T_s is the sink maximum temperature, T_a is the ambient temperature, and P is the CPU power dissipation. The total thermal resistance is given by:

$$\Psi_{\text{tot}} = DF \times R_{\text{package}} + \Psi_{\text{TIM2}} + \Psi_{\text{sink}} \quad (5)$$

where Ψ_{TIM2} is the thermal resistance of second-level TIM. The junction temperature (T_j) is given by

$$T_j = P \times [DF \times R_{\text{package}} + \Psi_{\text{TIM2}} + \Psi_{\text{sink}}] + T_a \quad (6)$$

Note that P and DF depend on the electrical design of microprocessors. To stay on the course of Moore's Law, they are expected to increase for next-generation microprocessors. Equation 6 contains all the relevant terms in guiding thermal technology development. Assuming that T_j for next-generation microprocessors has to be the same as current technology, then the thermal resistance of various components has to decrease. Ψ_{TIM2} is typically a small portion of the total thermal resistance. Therefore, thermal designers are left with two choices: improve R_{package} and Ψ_{sink} . Since R_{package} is multiplied by DF , which is expected to be greater than 1, a reduction in R_{package} leads to a greater reduction in Ψ_{tot} . Because of this, the industry is putting a great amount of effort into reducing R_{package} . Ψ_{sink} is also important; however, the choices are limited here because the heat has to be dumped into air and is therefore limited by the low thermal conductivity of air. Consequently, to reduce Ψ_{sink} , the only choice is to increase the volume of the heat sink after exhausting all the other optimization techniques such as heat pipe heat sinks and an increase in the airflow rate. Increasing the airflow rate results in higher levels of noise. The volume of the heat sink is subject to space constraints and can only be increased by using a remote heat exchanger. (In this paper, a remote heat exchanger means that the heat sink is not directly attached to the top of the package, but is installed somewhere else in the chassis.) Because of all these factors, it is clear that if both P and DF increase in the future, thermal technology

development needs to focus on a) reducing R_{package} and b) the use of remote heat exchangers.

In this paper, we focus, among various key and promising strategies, on reducing R_{package} . R_{package} consists of three components: R_{si} , R_{TIM1} , and R_{spreader} . R_{si} can not be changed due to fixed conductivity of Si. R_{TIM1} can be changed by optimizing the TIM by the use of micro and nano particles. We focus on polymer-based TIMs in our discussion. R_{spreader} can also be changed. This can be achieved by using a microchannel liquid cooler. Liquid cooling technology will also enable the use of a remote heat exchanger and can possibly increase its efficiency. Since thermal design is based on the maximum T_j on the die, another strategy that could be followed is to locally cool the die at the hotspots by using Thin Film Thermoelectric Cooler (TFTEC) made of thin film superlattice or nanocomposites. Ψ_{jc} in Equation (2) is given by:

$$\Psi_{jc} = \frac{T_{j,\text{max}} - T_c}{P} \quad (7)$$

By locally cooling the hotspots using TFTEC, the net effect is a decrease in Ψ_{jc} leading to a decrease in effective DF , as seen from Equation 2. The use of TFTEC will, however, lead to an increased burden on the other cooling components, due to the electrical power that is put into the TEC to achieve the desired cooling effect. Since TFTEC is used only to cool a few localized hotspots, not the whole chip, the increase in the total power to be dissipated by the other components is expected to be low. Figure 4 conceptually shows the idea of the use of various nano and micro technologies for cooling the next generation of microprocessors.

We discuss these three technologies in detail in this paper. Our primary focus will be on the technological merits of each technology and also on the fundamental and practical challenges that must be met to enable these technologies. The rest of this paper is divided into three sections: particle-laden thermal interface materials, microchannel cooling, and TFTEC. In the final section, we discuss the challenges that must be solved to enable these technologies.

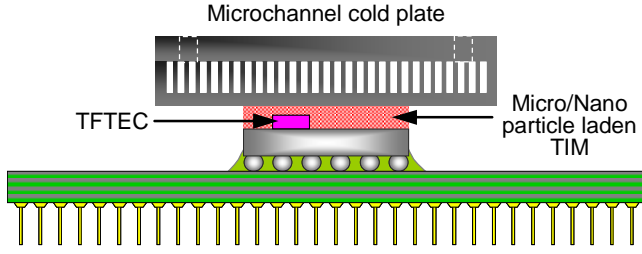


Figure 4: Schematic of futuristic thermal solutions

Nano and Micro Particle-laden TIM

Figure 4 shows the schematic of a particle-laden TIM (P-L TIM). Particles are added to enhance the thermal conductivity of the TIMs. Current commercial TIMs utilize micron-sized particles. Due to the advent of nanotechnology, particles of virtually any size can be made. The question that needs to be answered is whether nano-sized particles will lead to any benefits. The thermal resistance of a P-L TIM can be written as:

$$R_{TIM} = \frac{BLT}{k_{TIM}} + R_{c1} + R_{c2} \tag{8}$$

where R_{c1} and R_{c2} represent the contact resistances of the TIM with the two bounding surfaces. R_{TIM} depends on these contact resistances and on both k_{TIM} and Bond Line Thickness of TIMs (BLT). Both BLT and k_{TIM} are dependent on the particle volume fraction and size.

Prasher et al. [4,5] showed that k_{TIM} can be accurately captured by the Bruggman Asymmetric Model (BAM). BAM is given by following equation

$$\frac{k_{TIM}}{k_m} = \frac{1}{(1-\phi)^{3(1-\alpha)/(1+2\alpha)}} \tag{9}$$

where ϕ is the volume fraction of the fillers, k_m is the thermal conductivity of the matrix and $\alpha = 2R_b k_m / d$, where R_b is the interface resistance between the fillers and the matrix. Equation 9 assumes that thermal conductivity of the fillers (k_p) is much higher than k_m . Figure 5 shows the comparison of Equation 9 with data on various TIMs. Some of the other data in Figure 5 are from references [6] and [7].

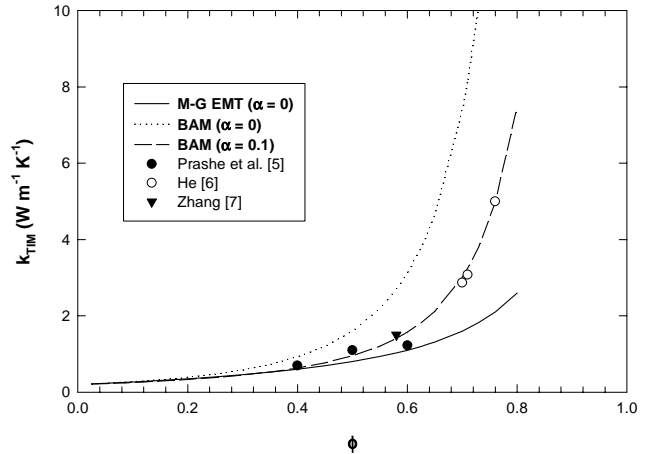


Figure 5: Thermal conductivity of TIMs with respect to volume fraction of fillers

The importance of R_b between the fillers and the matrix is shown in Figure 5. Equation 9 shows that at $\alpha = 1$, $k_{TIM} = k_m$, and for $\alpha > 1$, $k_{TIM} < k_m$ in spite of the fact that $k_p \gg k_m$. α can be large either for a smaller particle size or a large value of R_b . For nanoparticles, α can be very large, unless a substantial reduction in R_b is achieved. R_b at the interface between the particle and the matrix could arise due to two factors: 1) phonon acoustic mismatch (inherent property of interface of dissimilar material), and 2) incomplete wetting of the interface by the polymer. R_b due to phonon acoustic mismatch is of the order of $10^{-8} \text{ K m}^2 \text{ W}^{-1}$ at room temperatures [8]. This means that $\alpha = 0.0004$ due to phonon acoustic mismatch for $d = 10 \text{ }\mu\text{m}$ and $k_m = 0.2 \text{ W/m-K}$. Therefore, phonon acoustic mismatch could be ignored in comparison to the incomplete wetting; however, for nanoparticles, phonon acoustic mismatch could become important. Putnam et al. [9] measured R_b between polymer and alumina in the range $2.5 \times 10^{-8} - 5 \times 10^{-8} \text{ }^\circ\text{C-m}^2 / \text{W}$. This means that the critical radius ($\alpha = 1$) below which the thermal conductivity of the nanocomposite is less than the conductivity of the matrix varies between 10nm and 20nm. It is because of this reason that carbon nanotube-based composites have not been able to achieve high k . Therefore, using only nanoparticles in the TIM can lead to a decrease in k_{TIM} as compared to micron-sized particles. However, a mixture of micro and nano sized particles can possibly enhance the conductivity by providing a percolating chain between the larger particles. Nano-sized particles can also possibly reduce the BLT as compared to micro-sized particles.

Prasher [10] recently developed a model of BLT, which is given as

$$BLT = \frac{2r}{3} \left(\frac{\tau_y}{P} \right) + \left(\frac{cr}{1.5} \right)^{0.188} d^{0.811} \times \left(\frac{\tau_y}{P} \right)^{0.188} \tag{10}$$

where τ_y is the yield stress of the polymer, d the diameter of the particles, P the applied pressure, and r the radius of the substrate. Figure 6 shows the comparison between Equation 10 and experimental data collected on various TIMs including greases and Phase Change Materials (PCM) containing a different volume fraction of particles.

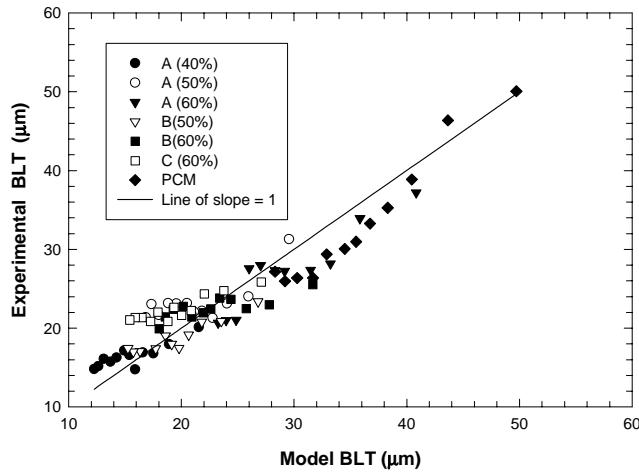


Figure 6: Comparisons of scaling bulk model (Eq. 10) with experimental data for the phase change material

Typically, k_{TIM} is used as the metric to compare various TIMs. Thermal resistance for a given pressure should be the metric to compare one TIM formulation with another because a higher k_{TIM} does not necessarily translate into a lower TIM resistance. Since both τ_y and k of TIMs depend on the volume fraction of the fillers, a minimum in thermal resistance can be achieved with respect to ϕ . Therefore, future P-L TIMs should be designed around this minimum.

Microchannel (MC)

Ever since Tuckerman and Pease [11] introduced the concept of microchannels, there have been numerous experimental and theoretical studies performed in the area of microchannels for heat transfer applications. Recently, the semiconductor industry has started to seriously consider microchannel cooling with liquid as the coolant [12, 13] due to the increase in total power generated by the microprocessor and also due to the presence of multiple hotspots [1]. A comprehensive review of microchannels using both single-and two-phase cooling is provided by Sobhan and Garimella [14]. Table 1 gives an overview of the difference between single-phase and two-phase cooling.

Table 1: Comparisons between single-phase and two-phase microchannel cooling technologies

	Single Phase	Two Phase
Flow rate	High (100-200 ml/min)	Low (10-30 ml/min)
Pressure drop	High (0.5-2 atm)	High (1-2atm)
Thermal resistance	<0.1 °C-cm ² /W possible	Less than single phase possible
Technological understanding	High	Low
Pump size	Small pumps possible	Smaller than Single phase possible
Modeling capability	Existing	To be developed

Before discussing the details of microchannel efforts at Intel Corporation, the Test Vehicle (TV) to capture the performance of the microchannels is briefly discussed. Figure 7 shows the schematic of the TV. Figure 8 shows the schematic of the heaters and the location of 20 integrated temperature sensors. The TV also has a small hotspot heater. This TV was used to assess thermal performance of single-phase and two-phase microchannels under uniform heating and hotspot heating conditions.

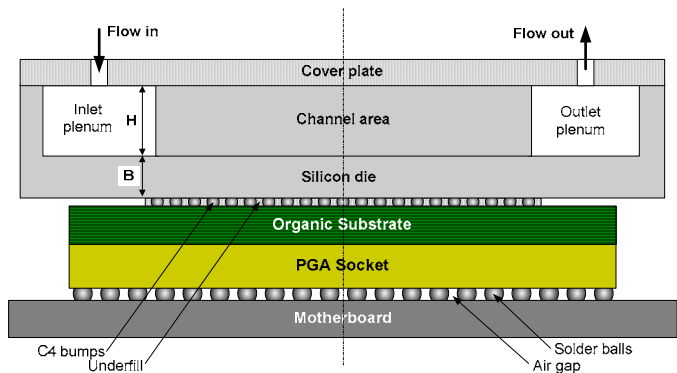


Figure 7: Schematic of the microchannel test device

Figure 9 shows the Scanning Electron Microscopy (SEM) pictures of the different microchannels considered in the experiment. Table 2 shows the dimensions of the various microchannels. For the two-phase case, the experiment was performed only on Microchannel 1.

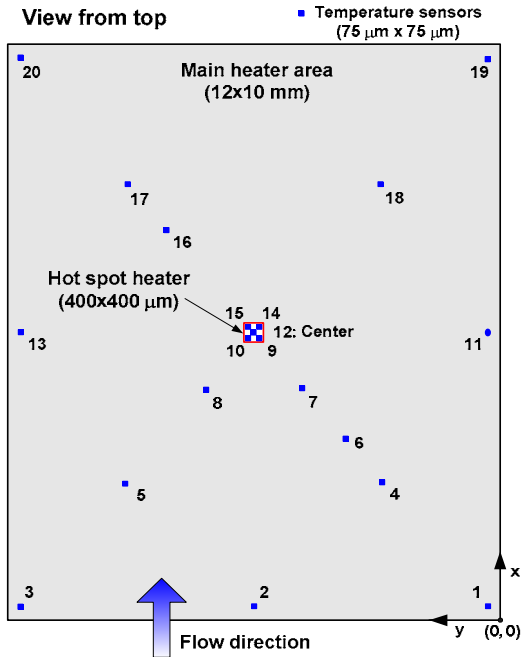


Figure 8: Layout of the temperature sensors and the hotspot heater on thermal test vehicle

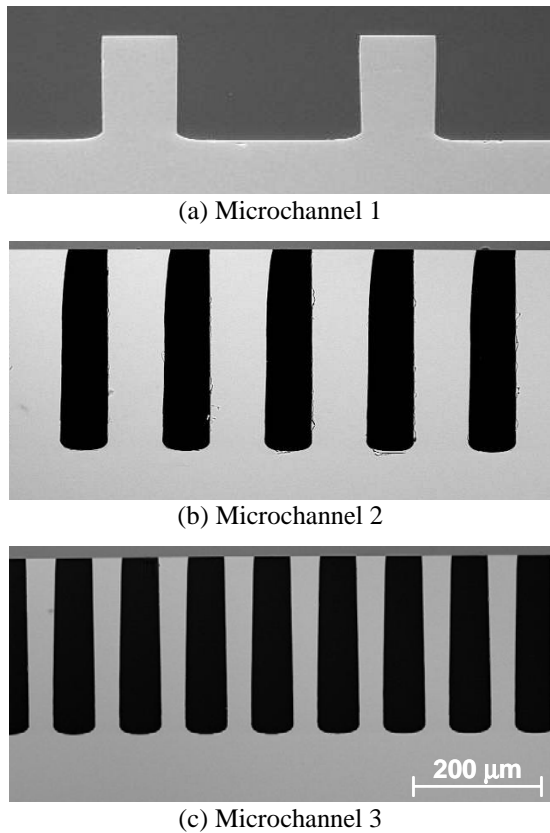


Figure 9: SEM photographs of cross-sections of three different microchannels

Table 2: Geometric details of various microchannels

	Microchannel 1	Microchannel 2	Microchannel 3
No. of channels	25ea	66ea	100ea
Channel width (w)	300 μm	65 μm	61 μm
Channel height (H)	180 μm	295 μm	272 μm
Channel length (L)	13 mm	15 mm	15 mm
Fin thickness (t)	104 μm	88 μm	39 μm
Silicon thickness (H+B)	350 μm	550 μm	
Inlet/outlet hole size (g)	1 mm		
In/out plenum size (R)	4 mm		
Flow width (D)	10 mm		
Cold plate width (D')	16 mm		
Cold plate length (L')	25 mm	27 mm	

One of the biggest fundamental challenges of two-phase cooling is the huge temperature and pressure oscillations. Figure 10 shows the data on the impact of hotspots on the temperature oscillation on a water-cooled two-phase microchannel. The flow rate in all the tests was kept constant at 2.5 ml/min. Figure 10 clearly shows that fluctuations in the wall temperature increase with increasing power to the hotspot. For the 0.6 W hotspot heating condition, the worst-case fluctuations are on the order of 30 °C, whereas for the 0.4 W hotspot heating condition, the worst-case fluctuations are of the order of 20 °C. The worst-case fluctuation for the uniform heating condition is on the order of 15 °C. This figure shows that temperature fluctuations depend on the power being dissipated from localized hotspots.

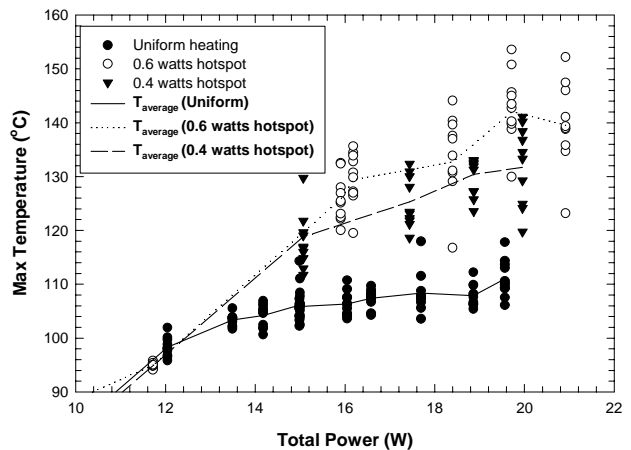


Figure 10: Fluctuation in the maximum temperature of the die under uniform heating and hotspot heating conditions

The temperature fluctuation must be controlled to consider two-phase microchannels as a serious technology. Poor flow distribution in two-phase

microchannels might lead to less flow in the regions of hotspots, leading to localized dry out on the hotspot which will result in a large and rapid increase in the temperature of the hotspot. Temperature and pressure fluctuations and poor flow distribution are the main fundamental challenges for two-phase microchannels.

Table 3 shows the parameters used in the testing of single-phase microchannels with water.

Table 3: Test conditions used for testing microchannel samples

	Microchannel 1	Microchannel 2	Microchannel 3
Fluid	Water		
Flow rate (ml/min)	159	110	98
Main heater (W)	70	70	70
Hotspot heater (W)	0, 0.5, 1, and 2	0, 0.5, and 1	0, 0.5, 1, and 2

Table 4 shows the comparisons between the experimental data and CFD modeling using Icepak*. It can be seen that the CFD model matches very well with the experimental data for both pressure drop and thermal resistance in uniform and non-uniform heating conditions. This shows that the existing commercial CFD tools can be used to design single-phase microchannels. Table 4 shows that a single-phase microchannel is capable of cooling very high heat flux hotspots (highest considered in this study is 1250 W/cm²) and is capable of achieving very small thermal resistance.

The main challenge for single-phase microchannel cooling is that water can not be used as a coolant because water freezes at 0 °C, whereas the freezing requirements for the electronics cooling industry is around -40 °C. Table 5 shows the comparison between the performance of widely used Propylene Glycol antifreeze and water mixture (50%-50%) for the same thermal performance, which means that both flow and convection resistance are the same. The microchannel dimension for this study is 50µm (D)×300µm (D) for water.

* Other brands and names are the property of their respective owners.

Table 4.1: Experimental and CFD results of Microchannel 1

Test conditions	Unit	Microchannel 1							
	Power (W)	Uniform				Non-uniform heating			
	Main heater	70		70		70		70	
	Hot spot heater	0		0.5		1		2	
Flow rate	159 ml/min								
Comparisons		Tests	Model	Tests	Model	Tests	Model	Tests	Model
R _{th} (°C/W)	R _{j,max-in}	0.41	0.40	0.53	0.52	0.70	0.70	1.04	1.05
	R _{j,max-out}	0.32	0.31	0.44	0.43	0.61	0.61	0.95	0.96
Temperature (°C)	T _{in}	20.1	20.1	20.1	20.1	20.1	20.1	20.0	20.0
	T _{out}	26.4	26.3	26.5	26.4	26.4	26.4	26.5	26.5
Pressure drop (kPa)		55.6	57.9	57.0	57.9	56.5	57.9	57.7	57.9

Table 4.2: Experimental and CFD results of Microchannel 2

Test conditions	Unit	Microchannel 2					
	Power (W)	Uniform			Non-Uniform heating		
	Main heater	70			70		
	Hot spot heater	0			0.5		
Flow rate	110 ml/min						
Comparisons		Test	Model	Test	Model	Test	Model
R _{th} (°C/W)	R _{j,max-in}	0.22	0.22	0.32	0.36	0.48	0.53
	R _{j,max-out}	0.09	0.09	0.19	0.23	0.35	0.40
Temperature (°C)	T _{in}	29.1	29.1	29.1	29.1	29.1	29.1
	T _{out}	38.3	38.5	38.3	38.4	38.3	38.4
Pressure drop (kPa)		55.6	57.4	56.3	57.4	55.7	57.3

Table 4.3: Experimental and CFD results of Microchannel 3

Test conditions	Unit	Microchannel 3							
	Power (W)	Uniform				Non-uniform heating			
	Main heater	70		70		70		70	
	Hot spot heater	0		0.5		1		2	
Flow rate	98 ml/min								
Comparisons		Tests	Model	Tests	Model	Tests	Model	Tests	Model
R _{th} (°C/W)	R _{j,max-in}	0.22	0.22	0.32	0.36	0.48	0.53	0.78	0.87
	R _{j,max-out}	0.08	0.07	0.17	0.21	0.33	0.38	0.63	0.72
Temperature (°C)	T _{in}	29.0	29.0	29.0	29.0	29.0	29.0	29.0	29.0
	T _{out}	39.4	39.3	39.6	39.4	39.8	39.5	39.8	39.6
Pressure drop (kPa)		44.1	46.1	43.5	46.0	42.7	46.0	43.3	45.9

Table 5 shows that the pressure drop of conventional antifreeze is very large. This is due to low thermal conductivity and the high viscosity of the antifreeze. The high pressure drop will lead to high forces on the bearings of the pumps to be used to pump the liquids. Therefore, for single-phase microchannel cooling, alternate antifreeze coolants are needed that have large thermal conductivity and low viscosity.

Table 5: Comparison of pressure drops between PG 50% and water for the same thermal resistance

Liquid	Flow rate (ml/min)	Pressure drop (kPa)
Water	200	80
PG 50%	220	900

Another big challenge for microchannel cooling technology is that the coolant will also be used as the lubricant for pump bearings, because the pump has to be hermetically sealed. From a lubrication point of view, a liquid with high viscosity is preferable, whereas from a

pressure drop point of view, a liquid with low viscosity is desired. These are opposing requirements. Figure 11 shows the thermal performance of the package-based microchannel cold plate as a function of the pressure drop through the microchannels. It can be seen that, in order to reduce the thermal resistance of the microchannels, a large pressure drop will result. In turn, this large pressure drop across the device will generate significantly large forces on the bearings, thus increasing the wear and possibly reducing the lifetime of the pumps. In addition, the low physical size of the pump shaft may impose significant additional challenges on the bearing design. At last, due to the requirement of having a complete seal device and no maintenance, the coolant fluid must be used as a lubricant as well. These are usually conflicting properties for any fluid. Due to above limitations, sleeve bearings may be the most advantageous for future pumping devices used in package cooling.

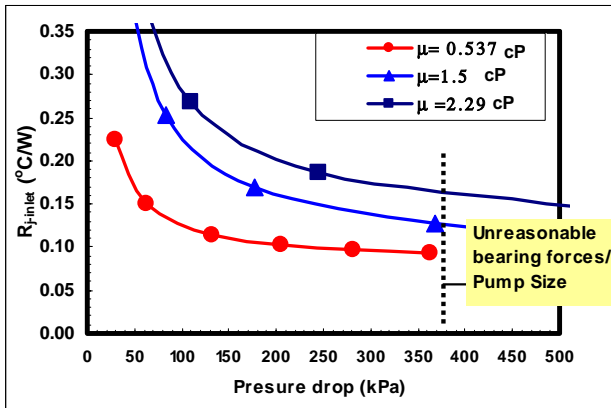


Figure 11: Thermal resistance vs. pressure drop for fluids with different viscosity

Figure 12 shows the schematic of a sleeve bearing. It can be seen that the sleeve bearing relies on maintaining a continuous film between the shaft and the housing. In a simplified way, the fundamental requirement for two surfaces to be lubricated is that the operating thickness of the lubricant between the surfaces must be thicker than the roughness of the surfaces. Based on Sommerfeld numbers [15], the minimum film thickness can be found as a function of rotational speed, radial loading, shaft diameter, length of the shaft in bearing, and the eccentricity of the shaft. Due to the pressure drop across microchannels, the radial forces could have high values, but they are usually less than 10N. A dimensionless parameter (Λ) is then used to determine the regime of lubrication:

$$\Lambda = \frac{h_{min}}{(\sigma_{shaft}^2 + \sigma_{housing}^2)^{1/2}} \tag{11}$$

where σ_{shaft} and $\sigma_{housing}$ are the root mean square roughness for the shaft and the housing surfaces, respectively, and h_{min} is the minimum film thickness of the lubricant. Typically it is considered that hydrodynamic lubrication occurs, when $\Lambda > 5$. This parameter is plotted in Figure 13 as a function of RPM and radial loading (shaft OD = 3 mm; Fluid viscosity of 1.5 cP; Roughness is assumed better than mirror surfaces).

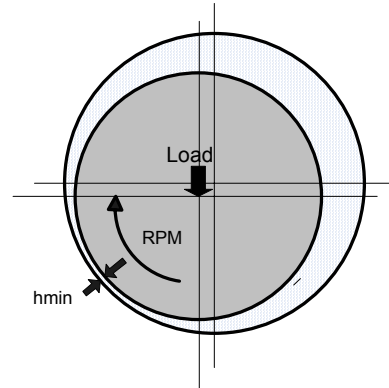


Figure 12: Simplified schematic of Sleeve (Journal) bearing

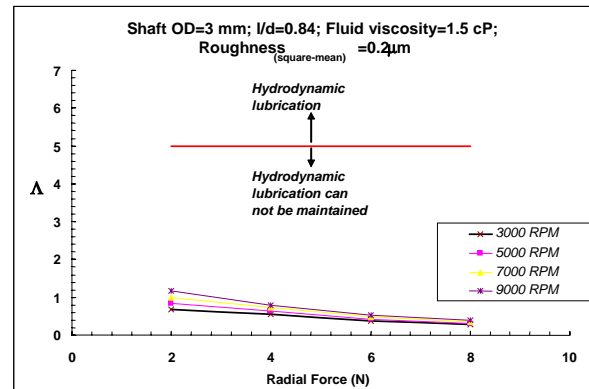


Figure 13: Lubrication regime for pumps using the coolant as lubricant

It can be seen that Λ is significantly smaller than 5 and therefore the hydrodynamic lubrication film can not be maintained under all conditions. This may be a major issue for any cooling device to be used in future package cooling. Although cooling solutions using pumps provide good package cooling, the thermal solution providers should not overlook the bearing life to ensure overall package reliability.

TFTEC

Figure 14 shows a TFTEC attached on the TV. The TFTEC is positioned over the hotspot of the TV. For this

analysis, the main heaters are powered to 100W to establish a background heat flow and the hotspot is powered to 3W. Due to the small size of the hotspot, $400\mu\text{m}\times 400\mu\text{m}$, the hotspot heat flux is $1875\text{W}/\text{cm}^2$. For this analysis, $R_{\text{TIM1}} = 0.15^\circ\text{C}\cdot\text{cm}^2/\text{W}$. The package in turn was cooled with a heat sink, which provides a Ψ_{ca} (case to ambient thermal resistance) of $0.35^\circ\text{C}/\text{W}$. Both thermal contact resistance and electrical contact resistance are analyzed.

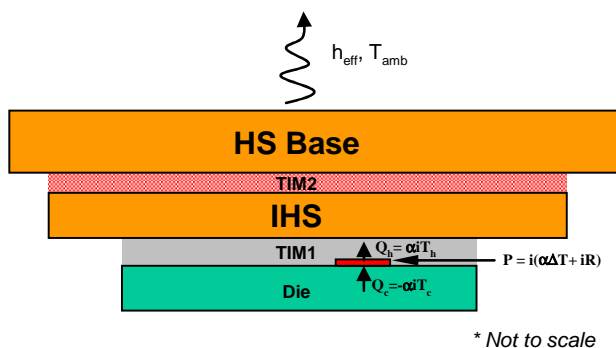


Figure 14: Schematic of the physical model to simulate the performance of TFTEC

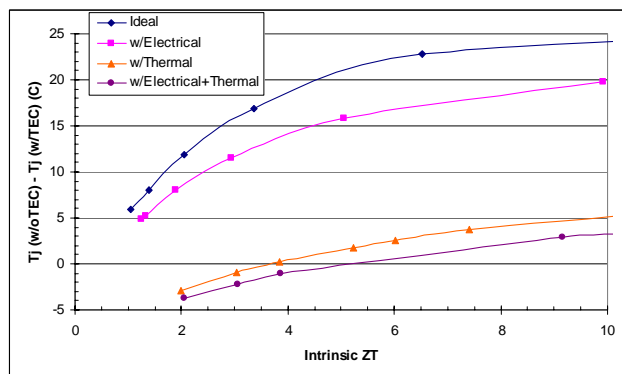


Figure 15: Impact of electrical and thermal contact resistance on the cooling performance of TFTEC

The ideal condition for the TFTEC would be when there are no extra electrical contact resistances and no extra thermal resistances in the TEC. For clarification, consider the electrical and thermal resistance terms separately. The TFTEC is an electrically powered device and so there will be electrical resistance associated with each element in the electrical stack-up. Under normal conditions there will also be a contact resistance associated with each interface between adjoining materials in that stack-up. This extra contact resistance is ideally negligible, but in reality will be non-zero. The value of the electrical contact resistance can be determined by measuring the total electrical resistance of the TEC and then subtracting the electrical

resistance of all the elements in the electrical stack-up. The difference is the electrical contact resistance. In a similar manner the thermal contact resistance can be determined by measuring the thermal resistance of the TFTEC and subtracting the thermal resistance of each of the elements in the thermal stack-up.

The impact of the electrical, thermal, and combined contact resistances on the ability of the TFTEC to suppress the hotspot temperature is presented in Figure 15. The amount of temperature suppression is plotted against the intrinsic ZT, where the intrinsic ZT is the ZT of the thermoelectric material itself and does not include any of the potential loss mechanisms. Temperature suppression is defined as the difference between the hotspot temperature without the TFTEC and the hotspot temperature with the TFTEC in place and powered. As the intrinsic ZT increases, so does the ability of the TFTEC to suppress the hotspot temperature. Four curves are presented in Figure 15. TFTEC performance depends on the current as well as the ZT. Performance increases with increasing current up to a point, and then decreases thereafter. Each point of each curve is therefore the maximum performance for a module with the listed ZT value based on a separate current sensitivity study. The highest curve is the idea case. For this curve the electrical and thermal contact resistances are set to 0 (turned off in the model). Keep in mind that there are still electrical and thermal resistances in the TEC, as there must always be, but that only the contact resistances have been turned off. This represents the best possible performance of the TFTEC. As can be seen, substantial hotspot temperature suppression (greater than 15°C) is possible for intrinsic ZT about 3 and above.

The second highest curve presents the calculated temperature suppression for the case where the electrical contact resistance is used, but the thermal contact resistance is kept at 0. The electrical contact between each layer in the electrical stack-up was set to $1\times 10^{-11}\text{ Ohm}\cdot\text{m}^2$ for this analysis. There is still reasonably good temperature suppression for reasonable values of ZT.

The impact of the thermal contact resistance is presented by the third curve in the figure. The thermal contact resistance value of $5.75^\circ\text{C}/\text{W}$ was determined as described above for an actual TFTEC module. The curve shows a substantial degradation in the ability of the TFTEC to suppress the hotspot temperature. Based on this analysis it is apparent that the thermal contact resistance plays a much larger detrimental role in the performance of TFTEC.

Lastly the combined effect of both contact resistances is plotted. This represents a more real TFTEC module since the two major loss mechanisms are now included. It shows an additional decrease in overall performance.

The lower two curves, both with the thermal contact resistance included, show temperature suppression of less than 0 for low values of the intrinsic ZT. This simply implies that the application of a TFTEC with these properties would actually force the TV to operate at a higher temperature than if the TFTEC were not there at all.

The analysis shows that the thermal contact resistance is an important parameter and needs to be carefully controlled and minimized in order to achieve reasonable hotspot temperature suppression with a TFTEC.

CONCLUSION

Micro and nano technologies have great potential for next-generation electronics cooling; however, there are many fundamental and practical challenges that need to be met for these technologies to become a reality. These challenges have been discussed in the paper:

- 1) An optimum mixture of micro- and nano-sized particles could improve the BLT and thereby reduce the thermal resistance.
- 2) Package-based microchannel technology is demonstrated to offer significant cooling improvement. For single-phase microchannel cooling, the key challenges are the freezing requirement for electronic cooling (-40°C) and the pump reliability due to a dry contact in the bearing. For two-phase microchannel cooling, the fundamental challenge is the huge temperature and pressure fluctuations, leading to flow mal-distribution to the microchannels.
- 3) The TFTEC technology can be fabricated in package to suppress the hotspot temperature in the die. The key challenge is to minimize the parasitic resistances at electric and thermal contacts in the module circuit toward achieving a reasonable thermal benefit.

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REFERENCES

- [1] Watwe, A. and Viswanath, R., "Thermal Implications of Non-Uniform Die Power and CPU Performance," *Paper No. IPACK2003-35044*, presented at InterPack '03, Maui, Hawaii, USA.
- [2] Sauciuc, I., Chrysler, G., Mahajan, R., and Szeleper, M., 2003, "Air-cooling Extension – Performance Limits for Processor Cooling Applications," *Proceedings of the 19th SEMI-THERM Conference*, San Jose, CA, USA.
- [3] Torresola, J., Chrysler, G., Chiu, C., Mahajan, R., Grannes, D., Prasher, R., and Watwe, A., 2005, "Density Factor Approach to Representing Die Power Map on Thermal Management," *IEEE Transactions on Advanced Packaging* (In Press).
- [4] Prasher, R.S., "Thermal Interface Materials: A Historical Perspective, Status and Future Directions," to appear in *Special Issue of IEEE On-Chip Cooling*.
- [5] Prasher R.S., Koning, P., Shipley, J., Prstic, S., and Wang, J.L., 2003, "Thermal Resistance of Particle Laden Polymeric Thermal Interface Materials," *ASME Journal of Heat Transfer*, Vol. 125, No. 6.
- [6] He, Y., 2002, "Rapid Thermal Conductivity Measurement With a Hot Disk Sensor: Part 2. Characterization of Thermal Greases," in *Proceedings of the 30th North American Thermal Analysis Society Conference*, Sept 23-25, 2002, Pittsburgh, PA, USA, pp. 505-510, 2002.
- [7] Zhang, X., 2004, "Constructive Modeling Strategies and Implementation Frameworks for Hierarchical Synthesis," *Ph.D. Thesis*, Purdue University.
- [8] Cahill, D.G., Ford, W.K., Goodson, K.E., Mahan, G.D., Majumdar, A., Maris, H.J., Merlin, R., and Phillpot, S.R., 2003, "Nanoscale Thermal Transport," *Journal of Applied Physics*, Vol. 93, No. 2, pp. 793-818.
- [9] Putnam, S.A., Cahill, D.G., Ash, B.J., and Schadler, L.S., 2003, "High-precision Thermal Conductivity Measurements as a Probe of Polymer/nanoparticle Interfaces," *Journal of Applied Physics*, Vol. 94, No. 10, pp. 6785-6788.
- [10] Prasher, R.S., 2005, "Rheology Based Modeling and Design of Particle Laden Thermal Interface Materials," *IEEE Transactions on Components and Packaging Technology*, Vol. 28, No. 2, p. 230.
- [11] Tuckerman, D.B. and Pease, R.F. W., 1981, "High-Performance Heat Sinking for VLSI," *IEEE Electron Device Letters*, Vol. 2, No. 5, pp. 126-129.
- [12] Chang, J.Y., Prasher, R.S., Chau, D., Myers, A., Dirner, J., Prstic, S., and He, D., 2005, "Convective Performance of Package Based Single Phase Microchannel Heat Exchanger," *Paper No. IPACK2005-73126*, presented at InterPack '05, San Francisco, CA, USA.
- [13] Colgan, E.G., Furman, B., Gaynes, M., Graham, W., LaBianca, N., Polastre, R.J., Rothwell, M.B., Bezama, R.J., Choudhary, R., Marston, K., Toy, H., Wakil, J., Zitz, J., and Schimdt, R., 2005, "A Practical Implementation of Silicon Microchannel Coolers For

High Power Chips,” in *Proceedings of the 21st SEMI-THERM Conference*, San Jose, CA, USA.

- [14] Sobhan, C.B., and Garimella, S.V., 2001, “A Comparative Analysis of Studies on Heat Transfer and Fluid Flow in Microchannels,” *Microscale Thermophysical Engineering*, Vol. 5, 00. pp. 293-311.
- [15] Shigley, J.E., and Mischke, C.R., *Mechanical Engineering Design*, 5th Edition, McGraw Hill, 2002.

APPENDIX: NOMENCLATURE

B	base thickness of silicon die
BAM	Bruggman asymmetric model
BLT	bond line thickness of TIM
c	constant in Equation (10)
d	particle diameter
D	flow width
DF	density factor
g	inlet/outlet hole size
H	channel height
h	lubricant film thickness
L	channel length
P	applied power or pressure
R	thermal impedance under uniform heating condition
r	radius
T	temperature
t	fin thickness
w	channel width

Greek

α	dimensionless parameter defined in Equation (9)
ϕ	volume fraction
μ	viscosity
σ	root mean square of roughness
τ	yield stress
Λ	dimensionless parameter defined in Equation (11)
Ψ	thermal resistance under non-uniform heating condition

Subscript

a	ambient
b	interfaces between filler and matrix materials
c	case
ca	case to ambient
c1, c2	thermal contacts
j	junction
jc	junction to case
j,max	maximum junction
m	matrix
min	minimum
p	particle filler
s, sink	heat sink
si	silicon

spread	heat spreading
TIM	thermal interface material
TIM1	first-level thermal interface material
TIM2	second-level thermal interface material

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