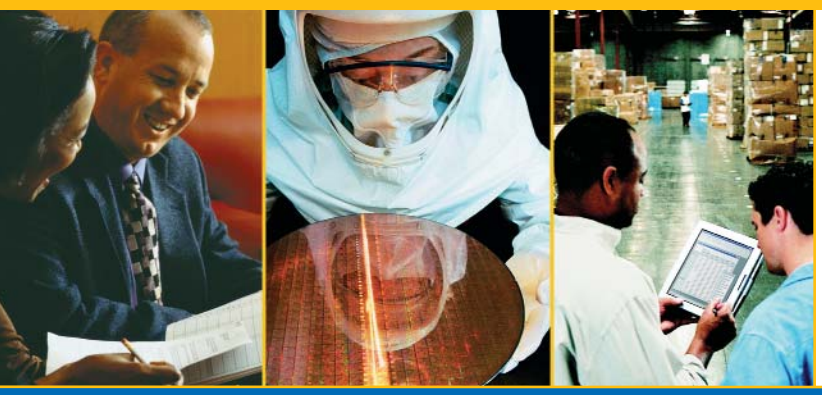
Volume 09 Issue 03 Published, August 3, 2005 ISSN 1535-864X DOI: 10.1535/itj.0903



Intel® Technology Journal

Managing International Supply and Demand at Intel

# Using Capacity Options to Better Enable Our Factory Ramps

More information, including current and past issues of Intel Technology Journal, can be found at:
**http://developer.intel.com/technology/itj/index.htm**

# Using Capacity Options to Better Enable Our Factory Ramps

Viswanath Vaidyanathan, Technology and Manufacturing Group, Intel Corporation
Dave Metcalf, Technology and Manufacturing Group, Intel Corporation
Douglas Martin, Technology and Manufacturing Group, Intel Corporation

Index words: capacity, options, forecasting

## ABSTRACT

Supply-chain management at Intel Corporation is more correctly defined as managing a supply demand network, since supply and demand are treated as equally important in a complex network. Cyclical industry trends, steep ramp curves, and small changes in the electronics industry can drive significant changes to individual semiconductor equipment suppliers as can be seen in Figure 1.

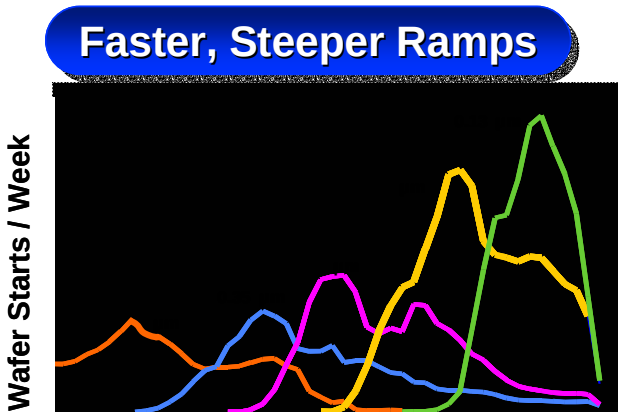



**Figure 1: Typical semiconductor manufacturing ramps**

Capacity planning within the Intel supply demand network is a complex process. Demand forecasts for Intel capital equipment tool sets, especially in lithography, are complicated by the extremely long lead times, expensive tool costs, and high contractual cancellation fees. In addition, changes in quarterly Intel manufacturing factory roadmaps cause considerable changes in the lithography exposure tool requirements. Lithography exposure tool requirements are extremely sensitive to changes in market demand, corporate strategy, equipment productivity, die size, field size, re-use, and product performance-related issues. These changes typically result in the overall lithography exposure tool requirements going up or going down, thereby potentially putting Intel at risk for cancellation fees with lithography equipment suppliers. In this paper, we provide an overview of options that signal a breakthrough for Intel in this field. Options ensure Intel's flexibility to demand changes while at the same time limit Intel's cancellation risk exposure.

## INTRODUCTION

In an ideal world, Intel would maximize revenues while minimizing equipment costs by bringing equipment up to production just in time to support the demand as shown in Figure 2.

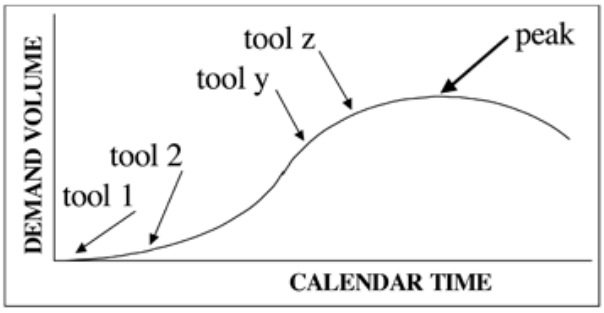



**Figure 2: Just in Time production equipment**

There are at least three key issues affecting this solution.

The first issue is the demand projection. It is difficult to predict what the peak volume of a particular product family will be or precisely when that peak volume will be realized. The risk of purchasing the first few tools of a lithography exposure tool model is small since Intel can control when and at what level production will start. However, purchasing the last few lithography exposure tools carries a higher risk since the market controls the peak height and the position over time. Delivering a lithography exposure tool early or having one that is not needed wastes Intel capital and increases Intel's costs. But on the other hand, not having a tool when it is needed, results in lost or delayed sales. Both cases can result in decreased profits.

The second issue has to do with equipment performance, and, again, predictability is the problem. For tools that

have previously been run in manufacturing at Intel, there is a historical basis upon which to project performance parameters needed to calculate the number of tools required for a specific production volume. With new models there are estimated parameters, but confirmation of performance will not occur until well after the majority of orders are placed. Buying the first few lithography exposure tools carries a low risk since these tools will be needed regardless of their ultimate performance. However, refined tool parameters based on actual performance of the first few tools can easily translate into needing a higher or lower number of tools than originally predicted during the ramp**.**

The third issue concerns equipment suppliers. Given that some of the lithography production equipment is among the most complex and costly ever built, it is not surprising that long lead times and significant cancellation penalties are involved. In addition, once the tool has been built, it must be shipped, installed, and qualified for production which can take several months. Each of these steps has an associated uncertainty in duration, and these uncertainties stack up. Standard payment terms for suppliers in the semiconductor industry are x% of the equipment price 30 days after tool delivery and the remaining y% after the tool is satisfactorily installed at the Intel manufacturing factory. Long before actual payment is due, lithography suppliers are required to make a substantial investment in both research and development and in the pre-purchase of materials to deliver lithography exposure equipment in high volume. Technology Manufacturing Engineering (TME), a group within Intel that primarily deals with equipment development and capital procurement, created a program called “options” with the lithography equipment suppliers. This program provides the suppliers the incentive to pre-purchase high-cost materials and risk-build equipment resulting in shorter lead times for Intel. Shorter lead times and the flexibility of options have helped Intel as well as the supplier to favorably react more quickly to changing market conditions.

## Problem Statement

The semiconductor industry downturn in 2000 left capital equipment suppliers with huge amounts of excess inventory that they had to either write off or sell at a loss. With net profits squeezed the equipment suppliers did not want to take more inventory risks. However, market conditions dictate factory roadmaps that in turn dictate the exact amount of lithography exposure tools needed in the Intel factories. The Intel challenge was to derive innovative solutions to order the right amount of equipment at the right time in an environment of volatile demand and tool performance. The supplier challenge was to work with Intel on alternative capacity-risk-sharing methodologies to enable faster response to market changes and reductions in cycle time. Both Intel and suppliers needed innovative solutions to address these problems. Figure 3 shows the variability in the semiconductor industry.

Due to the inherent uncertainties of forecasting, Intel tends to be conservative in estimating tool capacity parameters. This introduces a buffer into the system at the start of a ramp. However, as the ramp matures and more knowledge is gained on the tool, both the overall requirement forecast and the tool capacity parameters change, which can affect the quantity needed during the ramp and at the end of the ramp. This exposes Intel to higher cancellation fees with the suppliers, which in turn increases pressure on Intel to accurately forecast lithography exposure tool requirements and also motivates Intel to look for innovative ways to reduce overall risk.

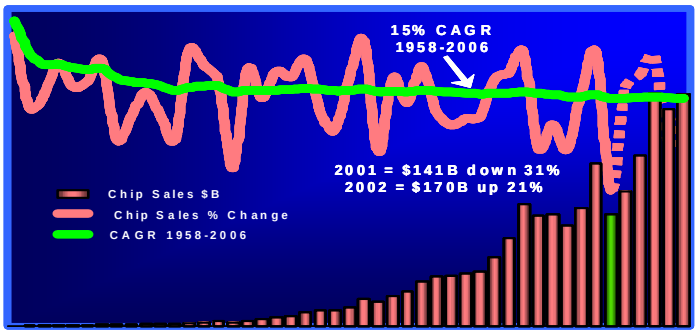



**Figure 3: Forecast variability**

## Problem Resolution Today

Manufacturing equipment capacity needs at Intel are primarily driven by three broad factors:

*Tool performance*: changes to the Model Of Record (MOR) parameters of run rate, utilization, and availability.

*Product requirements*: product performance, die size or process changes which require a different lithography exposure tool type for a given step of the process.

*Total capacity changes*: ramps are increased or decreased resulting in changes to the number of lithography exposure tools required.

By the time that Intel is able to confirm tool performance, product requirements and total capacity requirements, we typically are in one of two scenarios: Intel has too many lithography exposure tools or too few. Until the last few years the market economics were such that if Intel had extra lithography exposure tools, it didn't affect them adversely. New cost pressures have changed capital spending expectations, driving Intel to seek more precise methods to meet our customer needs without spending too much too soon.

Intel's capacity problems are currently resolved through two tactics:

1. Over-forecasting: Subsequent cancellation.
2. Under-forecasting: Tool allocation.

Over-forecasting sets up both the supplier and Intel for excess capacity and cancellation costs. Intel business processes and systems were not proactive enough to prevent this from happening. However, our business realities are such that this has occurred. This situation leads to order cancellations with suppliers, which costs both Intel and the suppliers.

Allocation is the process used by Intel to allocate lithography exposure tool deliveries to the most important requirements based upon process priorities, process margins, and other factors. When forecasts occur inside supplier lead time, lithography exposure tool deliveries are allocated among the requests. This process leaves some needs unmet (tools are too late to meet needs) and requires intense work from Intel and the supplier in order to move tool orders around to best fill the new needs.

These two solutions (cancellations and allocation) are obviously undesirable and they required TME to come up with an innovative way to manage lithography exposure equipment capacity.

## OPTIONS: AN INNOVATIVE CONCEPT

Options give Intel the right to purchase a tool in a reduced lead time at a certain pre-determined price. Intel purchases the options at a certain price from a supplier and must exercise or transfer the option to another tool prior to the expiration date.

Options provide Intel and the supplier with purchase order lead time, cancellation, and payment terms that are different from the standard terms and conditions of the standard corporate purchase agreement. Options provide a strategic approach to manage lithography exposure tool demand changes that are responsive to varying ramp needs but still limit Intel's cancellation liabilities with suppliers.

Options were originally developed for lithography suppliers since lithography tool lead times are long while their demand is subject to multiple changes in product demand. Due to their cost and lead time, lithography exposure tools are the primary ramp constraints at Intel's wafer manufacturing factories.

Conventional lithography tools have a long forecasted lead time plus long Purchase Order (PO) lead times as shown in Figure 4. These long lead times do not allow much flexibility to changes in demand for Intel or the supplier.

Additionally, since lithography suppliers have to invest upfront on the material and labor to build a lithography exposure tool, they inherently have high cancellation fees that increase over time up until the delivery date. Purchasing and exercising options provided Intel the right to procure un-forecasted lithography exposure tools in lead times much shorter than the contractual lead times.

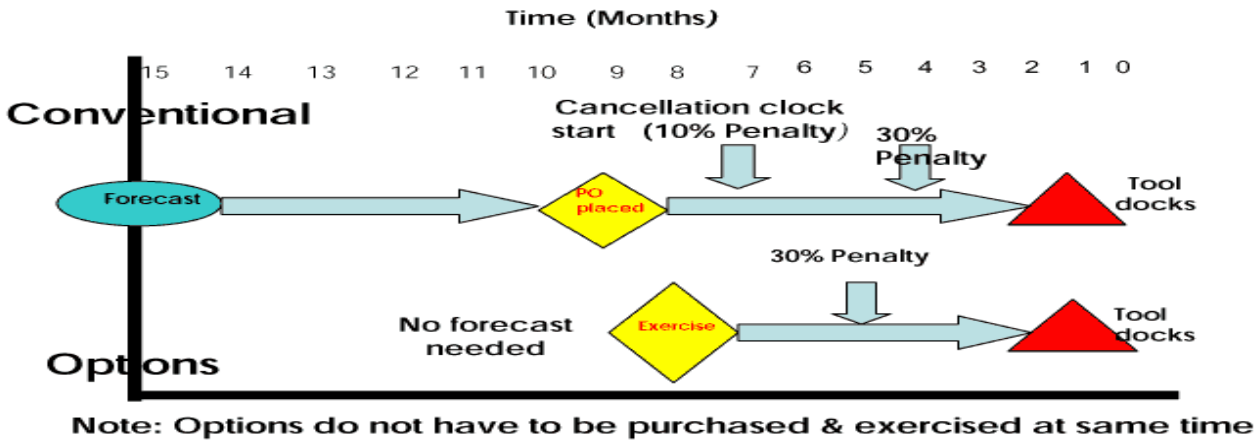



**Figure 4: Illustration of options**

An Intel team, with representation from Capital purchasing and Finance, developed a model to determine a fair option price that Intel would be willing to pay the supplier based on their actual cost of purchasing long lead material.

## OPTIONS: BENEFITS AND RISKS

Options, being the first of its kind in both the semiconductor industry and for Intel capital equipment, has a unique set of benefits and risks that are listed below:

**Intel Benefits**

- Reduced lithography exposure tool lead time to react more quickly to upside demand.
- Additional time to place lithography exposure tool orders while limiting cancellation liability.
- Better management of lithography exposure tool forecast fluctuations due to Long Range Plan (LRP) or MOR changes.
- Limited risk in market downturns due to flexibility of down-payment transfer.

**Supplier Benefits**

- Sharing of long-lead material costs.
- High probability of tool purchase since Intel is motivated not to let the options expire.
- Incentive to risk building tool to meet short lead time.
- Options purchase (down payment) provides cash in hand earlier compared to conventional tool sale (time value of money).
- Competitive advantage (especially where Intel uses dual suppliers).

**Program Risks to Intel**

Options expiration will result in Intel losing the down payment. This could be due to end-of-life of the tool or because of poor management of the options by Intel.

The potential benefits of the options concept made it extremely attractive to one of Intel's new 300 mm manufacturing facilities to pilot and pursue options for its ramp. The Intel wafer manufacturing facility needed to place the POs for the final lithography exposure tools; however, there were several pending changes, which could drive down tool requirements:

- **MOR improvements**: The tool model was new to Intel and a first of its kind for the supplier. All MOR data were based on performance specs against the earlier generation tools; however, the actual performance of the new lithography exposure tools was unknown.
- **Process flow revisions**: The potential removal of two existing process layers would free up existing tools for re-use within Intel.
- **Process capability changes**: Pending process capability changes that impact equipment run rate would have had an impact on the total lithography exposure tool requirements.
- **Long Range Plan (LPR) changes to peak:** An increase or decrease in the LRP and Wafer Starts Per Week (WSPW) would change the quantity of the new tool requirements.

- **Product mix changes:** When a product's die size is shrunk, and changes are made to the die per field, the result is a change in the number of lithography exposure tools required. If the LRP product mix changes to incorporate mostly shrink products, more lithography exposure tools will be required.

Obviously, any of the above could go in the other direction: MOR degradations, tool capability degradations, or a higher volume ramp peak could create uncertainty around placement of the equipment POs. The current capital process dictates that we plan to the official Plan of Record (POR). However, given these uncertainties, Intel could spend millions of dollars on capital that would sit idle (and aging) for up to two quarters until it could be converted for use on the next Fab process startup. Figure 5 shows a typical ramp cycle and where options are being used in the ramp life cycle for lithography exposure tools.

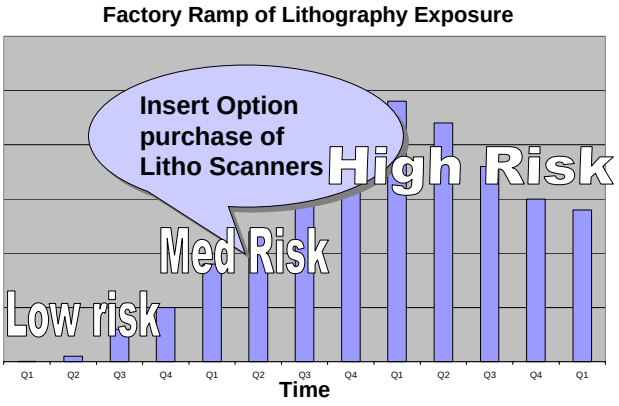



**Figure 5: Intel use of options for ramp peak**

## OPTIONS: INTEL RESULTS

By purchasing options for three lithography exposure tools, Intel was able to delay the decision to place POs as well as delay the onset of cancellation fees by four months. In the semiconductor industry, where the equipment life cycle is 18 months for each technology generation, a four-month savings is significant. The four-month window allowed Intel to have better information on MOR, process flow, process capability, and the LRP and thus make a better purchase decision. The cost of this delay is the time value of money of the options price. The value of this delay is the ability to delay depreciation expense plus avoid installing a lithography exposure tool that is aging and idle.

In real terms, Intel estimated an 80% probability that at least one tool would not be needed and a 40% probability that a second tool would not be needed for the ramp peak at one of their 300 mm factories. On a wafer cost basis, if Intel could avoid the purchase of high-dollar value lithography exposure tools, it would mean a reduction in wafer cost due to reduced capital depreciation. In the past, taking any risk on the purchase of a tool that constitutes a wafer manufacturing facility constraint has not been feasible at Intel. The options program helped the Intel wafer manufacturing facility pursue a cost-savings opportunity for four months without any increased risk to output.

A cross-functional team within Intel, including representation from the Purchasing, Factory Planning, and Finance organizations developed an options management process that is shown in Figure 6. Options are pre-paid assets that have to be very closely monitored through various LPR cycles and are accounted for within our forecasting and accounting systems.

The team recommended purchasing options only if either of the two following conditions exist:

1. If an Intel wafer manufacturing facility has a lithography exposure tool requirement that is within the supplier's forecasted lead time and there is no alternative to get the lithography exposure tool delivered to Intel when needed.
2. If the Intel wafer manufacturing facility expects a decision within lead time that would reduce the number of lithography exposure tools required.

It became apparent that if Intel had a requirement for a new lithography exposure tool that was within the suppliers forecasted lead time and there was no alternative to getting a tool on time, the option's purchase would be a valuable tool.

Managing options is also very important as an expired option results in unforeseen write-offs to Intel.

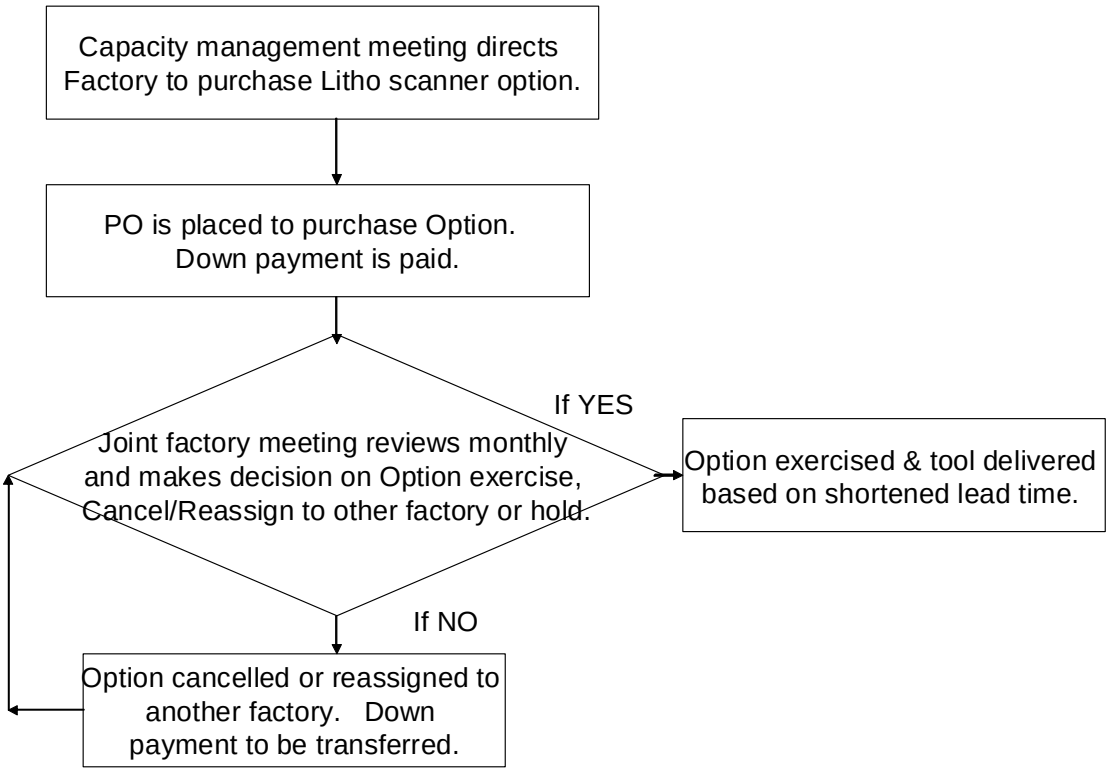



**Figure 6: Options management process**

## CONCLUSION

Managing forecast variation in the Capital Supply Chain can be very complex. Sources of forecast variability are numerous. Tool needs are determined months in advance of peak requirements. Tool performance matures over time. Market drivers change within forecasted windows. Options have given Intel a significant competitive advantage and provided the flexibility to react to future upside or downside market fluctuations while limiting cancellation liability with suppliers.

The focus of this paper has been the use of options for lithography equipment, but the techniques described here can be used for any equipment used in Intel's manufacturing lines. All of the arguments made here are also applicable to the materials purchased to enable manufacturing–spares, piece parts, reticles, to name but a few. Extensions into contracting for transportation, software, and so on will come with time. But perhaps the most important reason to practice and continuously improve these techniques is so that Intel can continually improve in meeting our customers requests.

## ACKNOWLEDGMENTS

The authors acknowledge many valuable discussions with and feedback from Beth Adkison, Bob Bruck, Joan Duemler, Barbara Haney, Karl Kempf, Janice Golda, and Peter Silverman, all of whom have enabled making the options program a success.

## AUTHORS' BIOGRAPHIES

**Viswanath (Vish) Vaidyanathan** has been with Intel since 1994 and is currently a training manager within TMG-Training. He has worked in various capacities at Intel factories and most recently as the capacity manager in the Lithography Capital Equipment Development (LCED) group. He has also been the recipient of an Intel Achievement Award for his work related to ergonomics and safety during his tenure at Fab 9 in New Mexico. Vish holds an MBA degree from the University of New Mexico and an M.S. degree in Industrial Engineering from Wichita State University. His e-mail is viswanath.vaidyanathan at intel.com.

**Dave Metcalf** has been with Intel since 1987 with the majority of his time spent managing numerous capital equipment suppliers across a variety of factory functional areas. Dave's current position is the supplier and business manager within the Components Automation Systems group at Intel. His primary focus is to engage closely with suppliers in helping them perform to expectations and to help enable Intel's technology and cost roadmap. Dave was awarded the Intel Achievement award in 2002 for his work with a supplier to accelerate a critical technology. Dave graduated from Brigham Young University in 1986 with a B.S. degree in Accounting. He received his MBA degree from Arizona State University in 1987. His e-mail is david.r.metcalf at intel.com.

**Douglas V. Martin Jr.** has been with Intel since 1984 and has been a lithography capacity engineer in the LCED group for the past five years. Douglas has had experience in Fab, Sort, Assembly, and Test capacity planning within Intel over the past 20 years. He graduated from San Jose State University in 1983 with a B.S. degree in Industrial Management within the SJSU Industrial Engineering Department. His e-mail is douglas.v.martin.jr at intel.com.

**THIS PAGE INTENTIONALLY LEFT BLANK**

For further information visit:

developer.intel.com/technology/itj/index.htm