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Second-Generation Intel<sup>®</sup> Centrino<sup>™</sup> Mobile Technology

## **Performance and Power Consumption for Mobile Platform Components Under Common Usage Models**

# Performance and Power Consumption for Mobile Platform Components Under Common Usage Models

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## ABSTRACT

The second-generation PC platform built on Intel® Centrino™ mobile technology is the second generation of Intel's mobile technology, designed to address the four vectors of mobility: breakthrough mobile performance, integrated wireless LAN (WLAN) capability, great battery life, and thinner, lighter designs. Many architectural features have been added to improve the performance/watt behavior of the platform as compared to the first generation of the Intel Centrino mobile technology. Some of the new features provide significant performance benefits to the platform with a minimal power increase. Other features have been added to provide platform scalability headroom when running demanding applications under future usage models. Several new power-management techniques have been added to deliver on the Intel Centrino mobile technology goal of great battery life.

This new platform is comprised of the Intel Pentium® M processor, the Intel® 915 Express Chipset Family (GMCH), the Intel® 82801FBM I/O Controller Hub (ICH6-M), and the Intel® PRO/Wireless Connection, which combine to support new technologies such as Intel® High Definition (HD) Audio, Double Data Rate II (DDR2) memory, PCI Express\* (PCIe), and Serial

Advanced Technology Attachment (SATA). Various platform power-savings techniques such as Dynamic Row Power Management for memory and Intel Display Power Savings Technology 2.0 (DPST2.0) reduce the power consumption of the platform to account for the increased power demands the new features bring with them.

In this paper we discuss some of these new features and the impact they have on platform performance and power as observed while executing industry benchmarks. The benchmarks cover a wide range of usage models including typical office productivity, scientific programs, and DVD playback. The intent of the analysis is to give the reader a broad perspective on the next-generation Intel Centrino mobile technology's capabilities across a wide range of usages.

## INTRODUCTION

Intel Centrino mobile technology was introduced in March 2003 in order to address the four vectors of mobility: breakthrough mobile performance, integrated wireless LAN (WLAN) capability, great battery life, and thinner, lighter, designs. Similar to the first Intel Centrino mobile technology, this generation continues with a design emphasis on mobile vectors while introducing many architectural features not present in a mobile platform until now. New interfaces are supported including Serial ATA (SATA) and PCI Express (PCIe) in addition to power-savings techniques, both old and new, including Dynamic Row Power Management for memory and Intel Display Power Savings Technology 2.0 (DPST2.0). Some of the enhancements are made possible in part by advances in process technologies increasing the density of transistors in silicon. Both

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generations of Intel Centrino mobile technology share a similar topology as illustrated in Figure 1.

This platform is comprised of the Intel Pentium M processor, the i915 GMCH, the ICH6-M, and the Intel PRO/Wireless Connection. This paper provides an analysis of the performance benefits and power consumption (which determines the battery life) that are realized through the new features of each component. In each section of the paper we focus on a given feature and discuss the power and/or performance impact of that feature. Our analysis consists of workloads commonly used in the industry for platform evaluation, among which are the following:

- SPEC CPU2000\* (<http://www.spec.org>)
  - SPECint 2000\* (<http://www.spec.org>)
  - SPECfp 2000\* (<http://www.spec.org>)
- SYSmark 2004\* (<http://www.bapco.com>)
- MobileMark 2002\* (<http://www.bapco.com>)

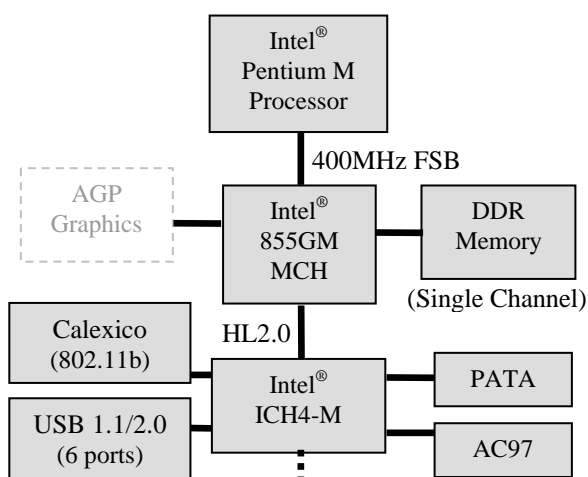
- 3DMark2001\* SE (<http://www.futuremark.com>)
- 3DMark03\* (<http://www.futuremark.com>)
- DVD Playback
- CD Audio Playback
- Windows\* XP\* Idle

Many of these workloads are industry benchmarks frequently used to evaluate platforms. This paper assumes the reader is familiar with these workloads. For further information regarding any of the benchmarks mentioned above, please visit the publishing Web sites listed by their name.

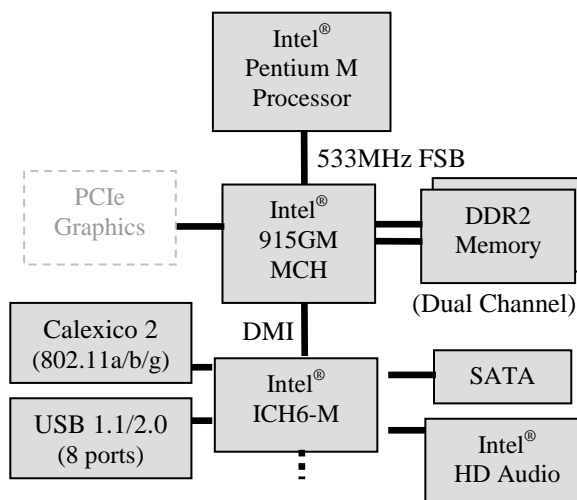
Many acronyms are used in this paper. For the purposes of clarity, we have included an appendix of acronyms at the end of this paper.

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### Previous Generation Platform



### Current Generation Platform



**Figure 1: Comparison of topology for Intel Centrino mobile technology**

In order to determine the power and performance impact of these new features, workloads were executed on an Intel Centrino mobile technology reference design instrumented for power measurements. Instrumented sense resistors allow for measurement of signals with a NetDaq\* data logger. This reference platform follows the Intel specifications that Original Equipment Manufacturers (OEMs) are recommended to follow for notebook designs. Processor C-state residency and performance metrics generated by benchmarks have been included where appropriate. C-state residency is measured using a utility

with a negligible impact on system behavior when running.

All data presented in this paper have been generated on a specific platform configuration that may vary for each set of results. All numbers presented are representative of the platform configuration for only that given set of data. Results will vary based on hardware and software configuration.

## PROCESSOR

The processor for the second-generation Intel Centrino mobile technology is the second-generation Intel Pentium M processor and is manufactured using 90nm process technology. This processor brings with it a number of new features and improvements over its predecessor. The L2 cache has been doubled to 2 MB and is optimized for reduced power consumption. The Front-Side Bus (FSB) has increased from 400 MHz to 533 MHz and the available processor frequencies have been increased. The Enhanced Register Access Manager provides increased performance for legacy scenarios that would normally stall under register renaming procedures. Intelligent branch prediction is made more efficient through the Advanced Tight Loop Execution feature, and security for the platform is increased with the introduction of the Execute Disable Bit (XD). These features and the impact they have on power and performance are discussed in detail.

### 90nm Process Technology

The second-generation Intel Pentium M processor is manufactured with Intel's advanced 90nm process technology entirely on 300 mm wafers. This enables Intel to provide the mobile community with significant performance headroom for tomorrow's usage models within today's thermal envelope. These 300 mm wafers provide twice the capacity of their 200 mm counterparts while the process dimensions double the transistor density. This allows Intel to double its already generous on-die cache to 2 MB. This provides a generous workspace for cache-sensitive workloads, such as imaging applications, while at the same time reducing the average power and maintaining the ability to extract the heat dissipated from periods of peak power. The latter is accomplished by maintaining approximately the same surface area as its predecessor.

This second-generation 90nm lithography produces 50nm gate dimensions (half the diameter of an influenza virus) with 50% faster transistors. Intel also strains N-type and P-type devices, increasing their electrical conduction by enhancing carrier mobility through the Si lattice by 10-20%. This significantly lowers the device voltages, a key ingredient to lower-power operation.

Ultimately the goal of the processor is to accomplish more work per unit time for a given level of power than its predecessor. This requires greater activity levels not only for the switching devices already detailed, but for the transistor interconnect structures as well. Intel has addressed this by providing seven layers of Cu interconnect with low-K dielectric to reduce overall capacitance.

The collective result of these advances supports a high-volume commercial device with 140 million switching devices whose gate oxide is less than five atomic layers thick. This enables the device to draw less than 1 W average power at greater than 10% less Thermal Design Power (TDP), which is at 1.8 GHz as compared to the original Intel Pentium M processor.

### 2 MB Power-Optimized L2 Cache

The L2 cache is one of the most effective business productivity per watt enhancements offered by mobile processors today. The second-generation Intel Pentium M processor offers an unprecedented 2 MB, low-power, low-latency L2 cache to efficiently tackle the growing working sets of present and future applications. The effect of on-die cache is to reduce the number of cycles wasted while waiting on memory. Not surprisingly, the percent performance impact of this grows with increasing processor frequency. When operating at the maximum performance level tasks get done sooner allowing the entire system to return to a low-power state. Power is also conserved while in the adaptive state, a Windows XP Power Management Policy, which allows the processor to switch voltage and frequency dynamically to address processor demand. Maximizing the potential of each intermediate-level performance point reduces the likelihood of crossing the utilization threshold that initiates a jump to the next frequency. This has a linear effect on power, due to frequency, and a square effect due to voltage ( $P \propto cfv^2$ ) and corresponding voltage level, which further reduces power demands.

The performance/power benefits of a larger L2 cache vary depending on the workload. Office productivity usage models (MS Word\*, Excel\*, Virus Scan\*, etc.) typically have large data sets that force lots of off-chip accesses to system memory; a larger L2 cache is definitely a plus in such an application environment.

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## L2 Cache Power and Performance Impact

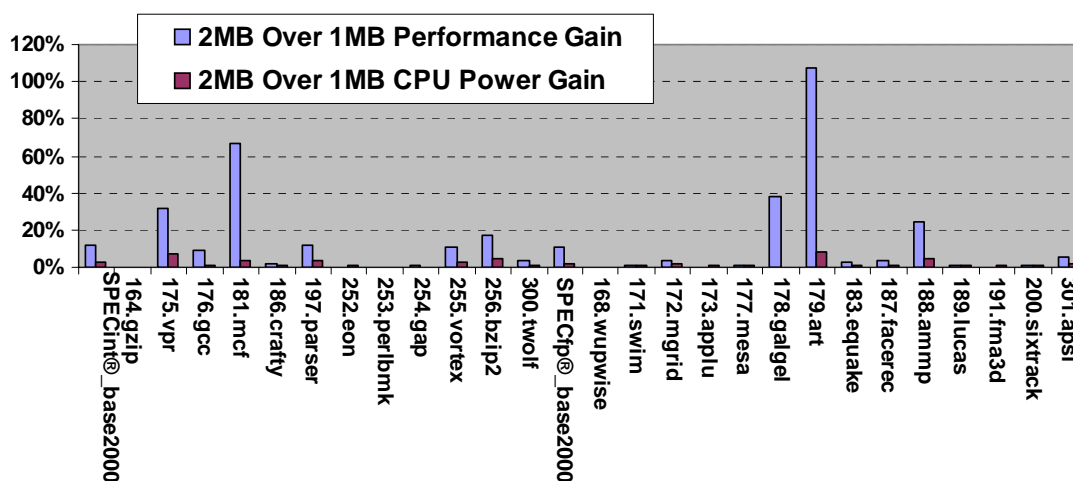


Figure 2: Performance and power comparison of 2 MB vs. 1 MB L2 cache

In a comparison of L2 cache sizes of 2 MB compared to 1 MB when running application-based benchmarks such as MobileMark 2002 and SYSmark 2004, we see ~5-7% performance gains for a 2 MB L2 cache over a 1 MB L2 cache with very little increase in processor power. For scientific-application candidates, we can use SPEC CPU2000 as a good proxy that shows that 2 MB outperforms 1 MB by ~11%, and processor power only increases by ~2-3%. Certain SPEC CPU2000 sub-tests show even larger benefits with a larger 2 MB L2 cache: for e.g., 175.vpr shows a ~30% and 7% performance and processor power increase, respectively with a 2 MB L2 cache; 181.mcf shows a ~65% and 3.5% performance and processor power increase, and a 179.art performance more than doubles for a ~8% processor power increase. These are excellent examples of mobile design tradeoffs that increase performance practically for free.<sup>1</sup> Figure 2 illustrates the performance improvements of the 2 MB cache compared to the increase in power.

An important concept to point out is that any time savings from getting the job done quicker, due to the 2 MB L2 cache, translates into additional platform power savings. This is accomplished by allowing various platform power-management policies to execute sooner, which forces the entire platform to go into its lowest power state. The net

result is a much more energy efficient platform for workloads that benefit from this behavior.

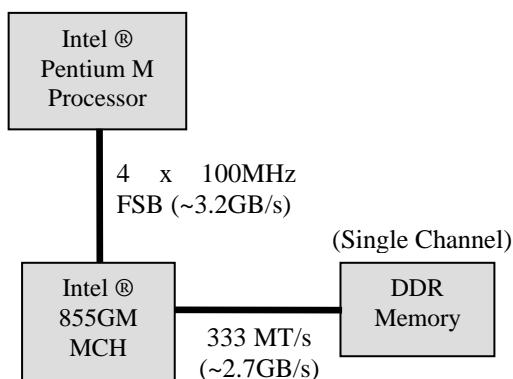
### Faster Front-Side Bus

With the previous platform, both the processor and memory components worked in near synchronous bandwidth levels. For example, traffic between the processor and GMCH runs at ~3.2 GB/s whereas traffic between GMCH and Memory is at ~2.7 GB/s. Note that the previous platform design was bottlenecked by system memory. One of the key bottlenecks that needed to be addressed with the new generation was the increasing gap between the available memory bandwidth and how it was available to the processor.

Two major improvements took place in the memory subsystem design. First, the second-generation DDR DRAM, DDR2, enabled much faster speeds of 533 MT/s (millions of transfers per second) compared to 333 MT/s for DDR. Secondly, the Intel 915GM Express Chipset memory controller provides two channels to simultaneously access system memory. Figure 3 compares this difference in topology. The net result is a significant increase in available bandwidth ( $533 \text{ MT/s} * 8 \text{ bits} * 2 \text{ ch} = \sim 8.4 \text{ GB/s}$ ) for the platform. This allows the FSB to operate at the maximum FSB throughput of 4.2 GB/s ( $533 \text{ MHz} * 8 \text{ bits} = \sim 4.2 \text{ GB/s}$ ). Figure 4 compares a second-generation Intel Pentium M processor at a clock frequency of 2.0 GHz with 400 MHz and 533 MHz FSB under SPEC CPU2000. During these experiments the 533FSB was run with DDR2-533 MT/s memory, and the 400FSB was run with DDR2-400 MT/s memory.

<sup>1</sup> Source: Intel Pentium M Processor 2.26 GHz– Intel 915 Express Chipset, Intel Customer Reference Board, 2x512MB DDR2 533MHz S0-DIMMs, 60GB 7200RPM Hitachi\* Travelstar HTS7260609AT00 HDD

### Previous Platform Topology



### Current Platform Topology

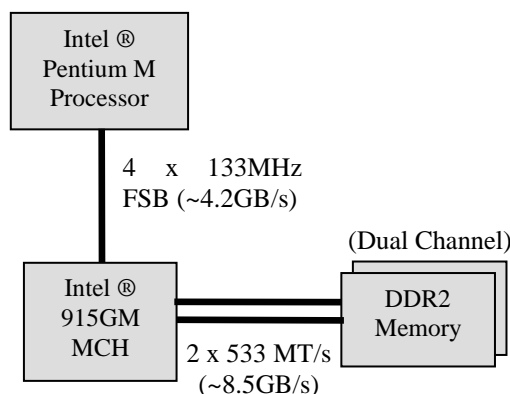


Figure 3: Comparison of memory topology for the previous platform vs. the new platform

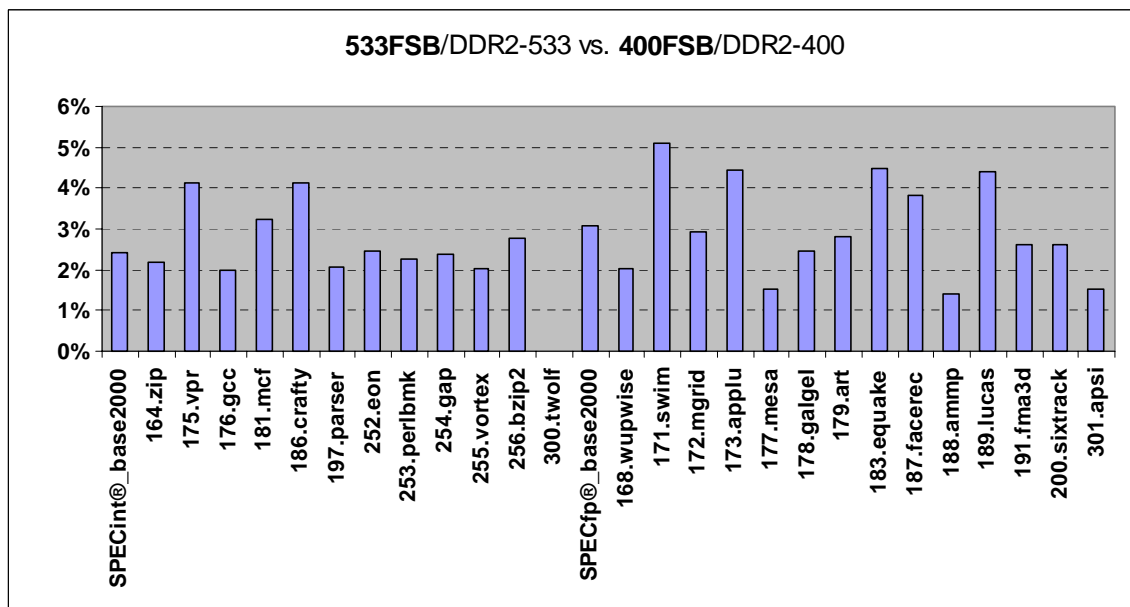


Figure 4: Front-side bus comparisons (533 MHz vs. 400 MHz)<sup>2</sup>

### Enhanced Register Access Manager

The register renaming support provided by the Pentium Pro processor sought to relieve the limited number of eight architectural registers provided by the iA instruction set. It did this by recognizing “false dependencies” within the instruction flow and providing virtually unlimited distinct physical locations for results when said cases were identified. Previous to register renaming the practice of

partial register writes provided relief to certain code that produced changes to a restricted 8- or 16-bit portion of the register.

This older technique adversely impacts the register renaming logic as it forces the renaming of the referenced register to stall until the partial register is written. Thus the throughput of the complementary one or two instructions that reference the alternate portion, or the entire register, is reduced.

<sup>2</sup> Source: Intel Pentium M Processor 2.0 GHz– Intel 915 Express Chipset, Intel Customer Reference Board, 2x256 MB DDR2 533 MHz S0-DIMMs, 60 GB 7200 RPM Hitachi Travelstar\* HTS7260609AT00 HDD

To minimize the impact of such legacy code, the processor defines a “calculate and merge” fused  $\mu$ OP and ALU support that provides for the partial references to be calculated in parallel. This  $\mu$ OP provision removes the stall condition that would otherwise impact the register renaming mechanism, regaining anywhere from 0 to 20% performance on legacy application scenarios.

### **Advanced Tight Loop Execution**

The processor recognizes even the smallest opportunity to apply clever solutions to increase performance while reducing power: for example, when a small well-behaved loop is found to be contained within the Instruction Length Decode Queue, power is conserved by stalling the Instruction Fetch Unit and running code from the Prefetch Buffer. As the loop characteristics are well understood, the Branch Prediction Unit can be powered down saving even more power.

### **Execute Disable Bit Support**

The predominant vulnerability to system attack is from malicious code that is stored as data and later run via an intentional corruption of a return address. The second-generation Intel Pentium M processor provides protection from such mechanisms through support for the Execute Disable (XD) bit functionality. This functionality is enabled when operating in the Physical Address Extension (PAE) mode, and the XD bit is set at the Page Directory and/or Table Entry level. Once set, attempts to execute “instructions” within the sequentially referenced pages of memory will result in a page fault to the OS. This added protection is enabled in Windows XP Service Pack 2 without cost to performance or battery life.

### **Processor Summary**

The second-generation Intel Pentium M processor continues its success in responding to the increasing performance demands of existing and future workloads and continues to effectively reduce power consumption that would inevitably increase if not addressed. Traditional techniques such as increased capacity (2MB L2 cache) and increases in frequency (processor clock and FSB) have been coupled with other novel techniques described to address these concerns. Workload analysis has shown these techniques to be effective in making the new processor a worthy successor to its predecessor.

### **GMCH**

The Intel 915GM Express Chipset is the integrated graphics memory controller hub (GMCH) for the second-generation platform built on Intel Centrino mobile technology. The chipset supports several new/faster interfaces such as a 533 MHz FSB, Double Data Rate II

(DDR2) Dual Channel, a PCI Express-based (PCIe-based) Direct Media Interface (DMI) link to the ICH6-M, and an x16 PCIe bus. There are also several power-management enhancements including C2 Pop-up and Rapid Memory Power Management (RMPM). The GMCH includes support for Pixel Shader 2.0 and DX9, integrated TVout, and improved power and performance techniques such as Intel Display Power Savings Technology 2.0 (DPST2).

### **Frequency Enhancements for GMCH**

The GMCH supports an increase in frequency on the FSB from 400 MHz to 533 MHz. The performance results of this change are covered in detail in the processor section of this paper. In addition to an increase in the FSB frequency, the Intel 915GM Express Chipset now adds support for DDR2 dual-channel memory extending the memory transfer rate to 533 MT/s. Further details of the impact of these new features are discussed in the ICH6-M section.

### **Improved Interfaces for GMCH**

#### **Direct Media Interface**

The Direct Media Interface is discussed in the ICH6-M section.

#### **PCIe Graphics/IO**

The GMCH contains a new universal scalable serial interface with a maximum number of 16 lanes of PCIe for the graphics interface to allow for maximum performance when needed. Different PCIe interfaces are used on other components of the platform as well. The serial interface in ICH uses this interconnect for devices such as Gigabit Ethernet and WLAN. For more details regarding PCIe please refer to the ICH6-M section of this paper.

### **GMCH Power-Savings Techniques**

#### **PCIe Active State Power Management**

PCIe Active State Power Management (ASPM) is provided to reduce the power of the PCIe serial bus links. Although serial bus links provide great performance and bandwidth, they come at a high power cost and must be actively power managed to reduce the power of the controller (GMCH) and the graphics component. Three link states (L0, L0s, L1) are available. Power savings of approximately 1.2 W for the GMCH have been measured when the L0s power-management state is utilized on a x16 PCIe lane for graphics. Further power savings of an additional 0.3 W have been measured if the lower power L1 state is enabled.

## C2 Pop-up

The C2 Pop-up feature was originally implemented to solve the problem when the UHCI USB master prevented entry of the processor to the C3/C4 state. This feature not only effectively addresses this problem but also allows the processor to enter a lower power C3/C4 state for I/O data transfers such as PCIe bus master traffic. Previous platforms only allowed the processor to enter the C3/C4 states when certain periods of inactivity were encountered. The new platform allows entry into C3/C4 and utilizes C2 Pop-up to place the processor into the higher power state only when necessary.

Evidence of power savings is demonstrated with Windows XP Idle. Without C2 Pop-up support C2 residency is ~95% in Idle. With C2 Pop-up support all 95% of the C2 residency in Idle is shifted to C4 residency. This accounts for significant power savings due to the difference in power consumption for the processor at these states. Processor power in C2 Pop-up can be 1.5-6 W higher than processor power in C4. Greater power consumption in C2 Pop-up is due to the increased processor voltage levels when it is entered at higher clock frequencies. This power savings may already be realized with some USB devices that already support selective suspend, which gives a similar result. This feature, however, provides the same benefit to all UHCI-attached USB devices.

## Rapid Memory Power Management (RMPM)

RMPM is a feature in the chipset that saves platform power by checking the processor utilization. When the processor is in C2-C4 states it does not need to access memory, thus allowing memory to enter Self Refresh mode to save power. This also allows the MCH to turn off logic related to reading/writing memory to save power. This feature provides significant power savings due to the degree of clock gating and DLL shutdown on GMCH allowed during this state.

With MobileMark 2002, we see significant power savings due to the high percentage of C3/C4 processor C-state residency during extended periods of Idle built into the workload. Over 90 minutes of MobileMark 2002 GMCH power savings from this feature is ~1 W. Figure 5 illustrates this power savings. Memory power decreases by ~0.3 W as well. This feature along with other power-savings techniques working together saves additional power, as described later. Workloads such as SPEC CPU2000 and 3DMark03 are more processor and memory intense so they spend almost 100% of the time in C0; this means that the RMPM feature would not save power in these other workloads since no time is spent in the C2-C4 states.

## Dynamic Row Power Management

Dynamic Row Power Management (DRPM) is one of the more useful power-savings features of GMCH since it generally saves power under any workload without impacting performance for the investigated workloads. This feature existed in the previous-generation GMCH, but it is particularly highlighted here for its ability to save power on the GMCH and Main Memory regardless of workload. Under MobileMark 2002, this feature alone saves ~0.4 W on GMCH and another ~0.4 W on the memory. Figure 5 illustrates this power savings. It works well with other power-savings features to save more power than each feature independently. Under SPEC CPU2000 and 3DMark03, DRPM saves at least 0.1 W on GMCH and 0.2 W on the memory, without performance degradation. These savings help to increase the battery life of the notebook and do so with no performance impact.

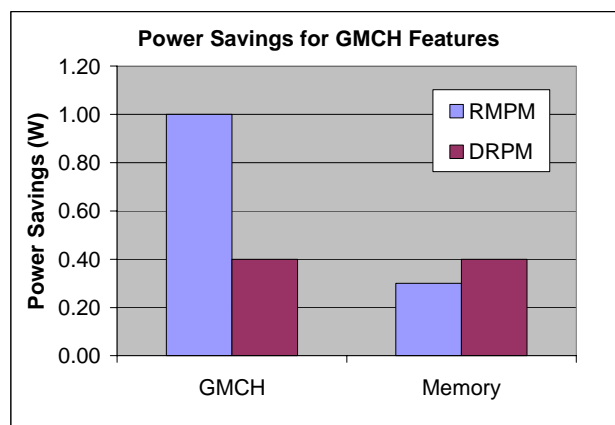


Figure 5: MobileMark 2002 power savings per feature

## Graphics Core Features

So far in this paper, the MCH portion of the Intel 915GM Express Chipset has been our focus; we now briefly describe the graphics portion of the chipset [12]. The feature set for the chipset integrated graphics includes increased core frequency of 200 MHz to 333 MHz, support for DirectX9 over the previous platform support for DirectX7.1, and four pixel pipes over the two in the previous platform. Also new is hardware acceleration for Pixel Shader 2.0 (Shadow Maps, Volumetric Textures, Slope Scale Depth Bias, and Two-Sided Stencils) and software accelerated vertex shaders. These graphics features coupled with DDR2 Dual-Channel support result in improved 3D performance. This is seen in 3D benchmarks including 3DMark2001 SE and 3DMark03. 3DMark2001 SE scores of the GMCH are more than double that of previous-generation GMCHs.

## Intel Display Power Savings Technology 2.0

DPST2.0 has enhancements over the first implementation including a more accurate picture representation. Power savings as before are primarily in the LCD backlight, and levels of savings are dependent on the original brightness and power of the panel, the image displayed, and the aggressiveness level that DPST2.0 is set to. There is no performance impact and no platform power increase due to additional computations. Additional circuitry for this feature is marginal, and 15-25% power savings for the LCD backlight may be achieved. Power savings for MobileMark 2002 with DPST2.0 has been measured at ~0.5 W for low power 14.1" SXGA+ panel at ~60 nits. DVD Playback<sup>3</sup> power savings for DPST2 has been measured at ~1.1 W as well as ~0.8 W savings during 3DMark03 with the same panel and brightness. Figure 6 illustrates these power savings. Power savings depend on the panel power, the panel type, and the LCD brightness so the absolute power savings may be higher even though the percentage savings should be similar.

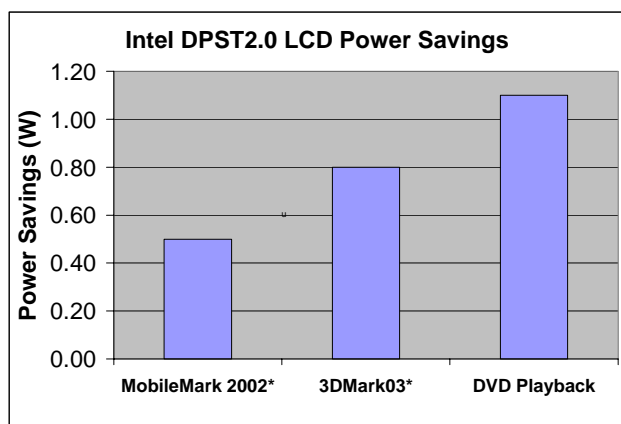


Figure 6: Power savings from DPST2.0

## GMCH Summary

All together the GMCH has enabled several performance features for the platform. These include faster buses to the processor, memory, external graphics, and ICH. They also include an increase in frequencies for the FSB and DDR memory interface. The new performance features are paired with platform power-reduction techniques that not only reduce GMCH power consumption but also impact components such as the processor, memory, and LCD backlight.

<sup>3</sup> DVD playback software used for testing is Intervideo WinDVD Platinum 5

## SYSTEM MEMORY

The new platform supports next-generation memory technology by implementing the DDR2 specification [10], an evolutionary technology that extends DDR [11] (supported on the previous platform). The new platform also introduces a second memory channel to the system memory, effectively doubling the total available memory bandwidth. With dual-channel DDR2 memory support, new platforms based on next-generation Intel Centrino mobile technology have increased peak bandwidth and lower Small Outline Dual Inline Memory Modules (SO-DIMM) power consumption over the previous generation.

## New Feature Support

### DDR2 Support

The DDR2 specification allows increased clock rates over DDR. The new platform supports a peak bandwidth of 4.3 GB/s, a 60% increase over the previous platform having a peak bandwidth of 2.7 GB/s (DDR 333 MT/s). The data path width remains the same so the increased peak bandwidth comes from the increased transfer rate from 333 MT/s to 533 MT/s. The platform also supports a 400 MT/s transfer rate. The DDR2 specification has a maximum transfer rate of 667 MT/s, which is not supported on the second-generation Intel Centrino mobile technology, but may be supported on future platforms.

The other major change in the DDR2 specification is the change to a 1.8 V operating voltage. In the DDR specification, the operating voltage is 2.5 V. This means that memory operations now consume less power on platforms based on next-generation Intel Centrino mobile technology, enabling increased battery life.

### Single-Channel and Dual-Channel Modes

The next-generation platform built on Intel Centrino mobile technology introduces support for dual-channel mode when both SO-DIMM slots are populated (otherwise the platform operates in single-channel mode). This technique is commonly used on desktop systems. In this configuration, the memory controller may access both SO-DIMMs, simultaneously resulting in 8.5 GB/s maximum theoretical aggregate bandwidth.

## Feature-Specific Workload Analysis Data

### System Memory Performance and Power

With the increased memory frequency and dual-channel capability, the new platforms are capable of increased performance over the previous-generation Intel Centrino mobile technology. The amount of performance increase varies depending on the workload. System memory power consumption depends mainly on the memory vendor and to a lesser degree, on frequency. Certain memory vendors

design memory components with lower power consumption than others.

Under a typical business productivity usage model, system memory enters the low-power Self Refresh mode when there is no activity. Under this usage model, a platform based on next-generation Intel Centrino mobile technology consumes approximately 40% less power than a platform based on previous-generation technology<sup>4</sup>.

When the new platform is executing a processor-to-memory intensive workload, increased memory frequency and dual-channel mode result in higher performance for a modest increase in memory power. In this configuration, the processor cannot take full advantage of the second memory channel because of the FSB limitation. Under this workload, a platform based on the next-generation Intel Centrino mobile technology scores approximately 40% higher than a previous generation system with a modest 6% power increase.

## ICH6-M

The Intel 82801FBM I/O Controller Hub (ICH6-M) [6] enables next-generation Intel Centrino mobile technology by introducing support for current and future peripherals:

- PCIe devices
- SATA devices with Advanced Host Controller Interface support.
- Intel HD audio devices.

In addition to these new interfaces, ICH6-M provides support for USB2.0 as on ICH4-M [1] but adds two additional ports. The ICH6-M also provides the interface for the Intel PRO/Wireless 2915ABG wireless module and ExpressCard\* devices.

ICH6-M provides these devices high-speed access to system memory via the DMI, a proprietary PCIe-based high-speed link to the GMCH.

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<sup>4</sup> The next-generation Intel Centrino mobile technology system is configured with 512 MB of 533 MT/s DDR2 memory in dual-channel mode. The system based on previous-generation Intel Centrino mobile technology is configured with 512 MB of 333 MT/s DDR. Though the previous-generation Intel Centrino mobile technology-based platform has both SO-DIMM slots populated, it is not capable of operating in dual-channel mode.

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## New Feature Support

### PCI Express

The ICH6-M supports the PCIe Base Specification, Revision 1.0a [2]. PCIe is a third-generation high-performance general input/output interconnect. Leveraging existing PCI architecture, PCIe introduces a scalable, point-to-point, power-managed, serial interface. Each basic connection is constructed with low-voltage, differential signal pairs.

The ICH6-M implements four PCIe root ports and each x1 port is capable of supporting 250 MB/s bandwidth in a single direction (500 MB/s concurrent). A connection between two PCIe ports is created with a link. An xN Link is built from N Lanes. Each lane is a set of differential signal pairs, one to transmit and the other to receive. For example, the ICH6-M can create a maximum of four x1 Links between itself and other PCIe-compliant devices.

Legacy bus power management states are replaced by new link power management states to account for the new interface. Link states are defined by the power management D-states of connected components or by Active State Power Management (ASPM) protocols. The ICH6-M implements L0, L0s, and L1 Link power management states for PCIe devices.

### Serial ATA and AHCI

The ICH6-M supports the following specifications:

- SATA Specification, Revision 1.0a [3].
- Several optional sections of the SATA II: Extensions to SATA 1.0a Specification, Revision 1.2 [4].

SATA is the next-generation replacement for Parallel ATA (PATA). It is a serial interconnect for mass storage devices utilizing high-speed differential signals. The ICH6-M supports the Intel SATA AHCI Specification, Revision 1.0 [5]. AHCI enables better performance and additional power-management capability over the base SATA specification.

The ICH6-M provides two SATA ports each with a maximum bandwidth of 150 MB/s with independent DMA operation. Coupled with AHCI, functionality is extended to incorporate hardware-assisted native command queuing and aggressive host-initiated device/bus power management. Native command queuing allows multiple commands issued to the device to be internally queued and serviced for better performance [7]. Combined operation with SATA and legacy PATA devices is supported, but AHCI operation must be disabled under certain platform configurations.

### Intel High Definition Audio

The ICH6-M supports the Intel HD Audio, Revision 1.0 [8] and is Universal Audio Architecture compliant. Intel HD Audio can support 192 kHz multi-channel output vs. 96 kHz stereo-channel output with AC'97 [9]. The two architectures are incompatible, and concurrent operation of Intel HD Audio and AC'97 functionality on ICH6-M is not supported.

The ICH6-M Intel HD Audio controller supports up to three external codecs, each of which is configured by software. Codecs are connected to the controller via a serial link, which is shared with the AC'97 controller. Codecs render audio streams when DMA requests are initiated by the controller. Each audio stream may contain one or more channels. Each channel can be dynamically assigned to a single codec converter.

Because Intel HD Audio data stream traffic does not require snooping of the processor cache, it enables processor entry into the C3/C4 state when the system is otherwise idling. This allows for significant power savings from the processor of at least 600 mW for DVD playback and CD audio playback [7].

### Direct Media Interface

To meet the device-to-memory bandwidth requirements of PCIe, SATA, USB 2.0, Intel HD Audio and others, a proprietary serial interface, based on PCIe, was developed, the DMI link. This link connects the ICH6-M and the GMCH. It offers 2 GB/s maximum bandwidth compared to 266 MB/s available with the ICH4-M hub interface. The DMI integrates priority-based servicing to allow concurrent traffic and isochronous data transfer capabilities for Intel HD Audio.

### ICH6-M Summary

The ICH6-M device introduces support for many new interfaces providing enhanced bandwidth for high-bandwidth applications and devices. SATA with AHCI support enables increased disk bandwidth, performance benefits from native command queuing, and more aggressive power management. Furthermore, Intel HD Audio provides better audio support over AC'97 in terms of audio quality, device features, and power management. Finally, the DMI provides high-bandwidth access to system memory.

### WIRELESS LAN

Next-generation Intel Centrino mobile technology carries with it a full range of WLAN support with the Intel PRO/Wireless 2915ABG WLAN solution. This product not only supports 802.11a, 802.11b, and 802.11g, but it also provides the Intel Wireless Coexistence System

(WCS) v.2 that mitigates wireless interference between Bluetooth<sup>Δ</sup> and WLAN. This solution also supports industry-standard wireless security features including WPA2 and Cisco<sup>\*</sup> Compatible Extensions v.3.

Intel PRO/Wireless 2915ABG is capable of providing high-quality streaming video playback. An Intel Centrino mobile technology client containing this card is capable of >99% packet arrival rate<sup>5</sup> with a 5Mbps MPEG2 stream thus producing a high-quality image. Figure 7 demonstrates the difference in video quality that may be observed for a data stream arriving at less than 99% packet arrival.

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<sup>Δ</sup> Bluetooth is a trademark owned by its proprietor and used by Intel Corporation under license.

<sup>\*</sup> Other brands and names are the property of their respective owners.

<sup>5</sup> Source: Intel PRO/Wireless 2915ABG Network Connection; Driver: 9.0.0.60; Software TIC:87406; 802.11A/B/G Access Point: Cisco Aironet 1200 ABG\*, System Firmware v12.2(15)JA3; All Platforms–Intel Pentium M Processor 1.40 GHz–Intel 855PM chipset, IBM\* X31, BIOS: 1.01, 256 MB PC2100 DDR266, ATI\* Mobility\* 9000 w/ graphics driver, ATI\* Mobility\* 9000 6.13.10.6269, LCD Screen: 12.1” TFT 1024x768x32-bit color; IBM\* IC25N04ATCS05-0 TravelStar\* 40 GB hard drive 5400 rpm, Laptop running on AC power, Windows\* XP\* Professional SP1 Build 2600. Chariot\* Console version 5.0 with Chariot\* Endpoint version 4.5. Performance tests and ratings are measured using specific computer systems and/or components and reflect the approximate performance of Intel products as measured by those tests. Any difference in system hardware or software design or configuration may affect actual performance.

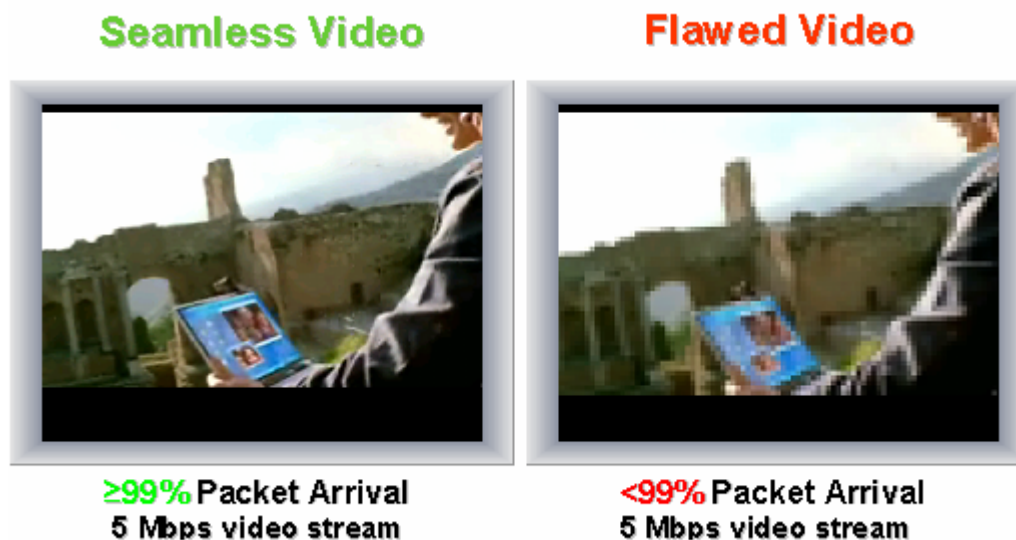


Figure 7: Example of video quality

In addition to quality video streaming, the Intel PRO/Wireless 2915ABG provides support for low-power states when idle. Power consumption is ~100 mW in idle for both associated and unassociated states to the AP. With the radio disabled the device consumes even less power, around 20 mW. Usage models such as Web browsing and e-mail can take advantage of these low-power-consuming states as typical usage in these cases is idle to a large degree.

The WCS v.2 feature allows for coexistence of both Bluetooth and 802.11b/g transmitter/receivers on Intel Centrino mobile technology while mitigating interference problems that result when these two protocols are exercised concurrently. Both 802.11b/g and Bluetooth transmit and receive on the 2.4 GHz base band. Without this feature wireless throughput rates may be significantly reduced.

## CONCLUSION

Collectively, the enhancements in the second-generation PC platform built on Intel Centrino mobile technology deliver generous processing power to the mobile business platform while maintaining robust battery-life levels. When a given performance level is accomplished at less utilization of system resources less platform power is consumed. This power can be applied to additional work or more demanding tasks. While today's benchmarks may not take advantage of the full potential of this platform, this platform can handle the work levels sure to be present in tomorrow's applications and work environment. This paper has illustrated the wide range of usages that the second-generation platform built on Intel Centrino mobile

technology is suited for and the impact of these usage models on system performance and power consumption.

## TABLE OF ACRONYMS

AHCI	Advanced Host Controller Interface
ALU	Arithmetic Logic Unit
ASPM	Active State Power Management
DDR	Double Data Rate
DLL	Delay Lock Loop
DMA	Direct Memory Access
DMI	Direct Media Interface
DPST2	Display Power Savings Technology 2
DRAM	Dynamic Random Access Memory
DRPM	Dynamic Row Power Management
DVD	Digital Versatile Disk
EHCI	Enhanced Host Controller Interface
GMCH	Graphics Memory Controller Hub
ICH	I/O Controller Hub
HD	High Definition
LCD	Liquid Crystal Display
MCH	Memory Controller Hub
OEM	Original Equipment Manufacturer

PAE	Physical Address Extension
PATA	Parallel Advanced Technology Attachment
PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
FSB	Front-Side Bus
SATA	Serial Advanced Technology Attachment
SO-DIMM	Small Outline Dual Inline Memory Modules
SXGA+	Super eXtended Graphics Array Plus
μOP	Micro-Op
USB	Universal Serial Bus
WCS	Wireless Coexistence Solution
WLAN	Wireless Local Area Network
XD	Execute Disable

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