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Fully Integrated CMOS Radios from RF to Millimeter Wave Frequencies

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Fully Integrated CMOS Radios from RF to Millimeter Wave Frequencies

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ABSTRACT

This paper reviews (a) recent CMOS demonstrations of capabilities for Radio Frequency (RF), microwave, and millimeter wave circuits from 1 GHz to 100 GHz, (b) advances in on-die isolation structures for integrating radio's delicate circuits with very noisy general-purpose processors on the same die, and (c) entirely novel design methods for complex RF passive networks on the package substrate by engineering the physical design of the package substrate (no discrete passive components added to the package) that diminish the silicon area requirements for multiband multiprotocol CMOS radios and frees silicon area to host complex digital processing and communication engines. Circuit design techniques are discussed to cope with intrinsic CMOS challenges and technology scaling. Building upon these developments, a vision for CMOS technology and platform direction is proposed.

INTRODUCTION

From 1995 to 2004, CMOS technology has proven its Radio-Frequency (RF), microwave, and millimeter wave capabilities by demonstrations of fully integrated key circuit blocks from 1 GHz to 100 GHz [1-7]. Low Noise Amplifiers (LNAs) with noise figures as low as previously reported for compound semiconductor technology started to be reported for fully integrated CMOS realizations. The intrinsic higher 1/f (flicker) noise corner in CMOS technology compared to bipolar technologies found compensation in novel circuit-level methods.

CMOS scaling enabled the technology to reach for higher GHz frequencies, and the higher speeds offer other opportunities to compensate at the circuit level for intrinsic technology drawbacks.

Only one intrinsic technology problem appeared to be fundamentally unsuited for technology scaling: RF transmission power levels. As CMOS scales, lower voltages are tolerated at the transistor terminals. Circuit-level solutions using power-combining techniques to add the power of parallel Power Amplifiers (PAs) in CMOS have met with success. Power combination of parallel PAs have being used on die [8], and in this paper, we discuss novel power-combining circuits on the package. These power-combining circuits on the package become *en passant* the supporting structure for MIMO or general antenna-diversity/beam-forming-based radios. This last step means the circuits on the package support what can be recognized as power combining on air to cope with CMOS RF power transmission limitations.

Nevertheless, CMOS technology's full potential would not be realized if only standalone radios are fabricated. Integration of delicate radio and general-purpose processors is the next goal. The co-habitation of delicate RF circuits and a very noisy general-purpose processor such as a 1 GHz 55 W Pentium® 4 processor on the same die was shown to be possible by proper circuit techniques, special deep nwell isolation structures, and exploitation of the digital substrate noise spectrum structure [9]. Novel entire designs of complex RF passive networks realized by trace engineering (no

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discrete components added) on the package substrate diminished the silicon area required for multiband multiprotocol radios and freed silicon area for hosting more digital circuits, processing units, and communications system new features [10].

Building on these developments, at the platform level, considering the PC motherboard, we articulate a vision for a new CMOS computing and communication platform. Instead of trying to integrate multiband multiprotocol radio circuits into already densely packed chips like a Pentium processor and its companion chipsets, it might be more promising to re-think the PC motherboard as a multiprocessor platform, where the processor and chipset will make a new ecosystem with two new chips that provide for multiband multiprotocol radios. In other words, a platform which is capable of supporting the variety of current standards and is also able to support always evolving standards is proposed. This new platform can extend its reach to encompass in a modular fashion wireless communications from 700 MHz, over the newly vacant TV bands, all the way to 60 GHz, where 7 GHz of bandwidth enables indoor high data rate omnidirectional wireless links and outdoor line-of-sight (LOS) high data rate backbone links.

The next sections in this paper detail the CMOS technology scaling effects on its RF, microwave, and millimeter wave capabilities; the new developments in package technology and novel CMOS-compatible devices; and further elaborate on the opportunities in the area of platforms for CMOS.

CMOS (EXCESS) THERMAL NOISE.

In the radio receiver front-end, the Low Noise Amplifier (LNA) is the first key component in which CMOS technology needed to prove its adequacy. By the aggressive scaling of CMOS technology, there was always the concern that the high field transport in the channel could produce too large a carrier velocity dispersion, and therefore microwave noise, significantly above thermal noise. That's because apart from not always having consistent definitions in the literature for excess thermal noise, a conductor or semiconductor is only guaranteed to develop thermal noise levels in thermal equilibrium, and will tend to develop noise levels above this equilibrium level whenever a dc current flows through them and more so as the electric field applied to the transport increases [11, 12]. The concern was that the noise level could become progressively higher with scaling in such a way that the gain of the device could not compensate and, in this case, scaling would start to produce higher noise figure transistors at some point.

Fortunately, the opposite has happened so far and even though the product g_mR_o decreases with nanometer scaling, the device transconductance (g_m), with typical RF device loading, still provides higher gain with CMOS scaling to compensate for the additional noise in the channel high field transport. Moreover, carrier transport in the channel of 90 nm CMOS and future nodes may experience a qualitative change in properties that leads to less carrier velocity dispersion due to a diminishment in the likelihood of carrier scattering events in such extremely short channels. If this becomes a new trend it will progressively benefit CMOS technology and will offer unprecedented lower noise figures with scaling at frequencies above 10 GHz. Currently, minimum noise figure (NF_{min}) numbers for CMOS transistors in 0.18 µm and 90 nm are respectively 1 dB and 0.5 dB at 5.5 GHz. These are at par with the best numbers offered by SiGe and other compound semiconductor technologies at these frequencies.

In reality, CMOS transistors are becoming virtually "noiseless" for practical purposes below 10 GHz. That completely shifted the design and optimization procedures for LNAs to include noise contribution from passives. A circuit-level method was developed by one of the authors to globally optimize the noise figure of LNAs, taking into account noise contributions from both passive and active devices. It became an extension of S-parameter methods used in traditional microwave methods and was named the "*backing-off*" method [6].

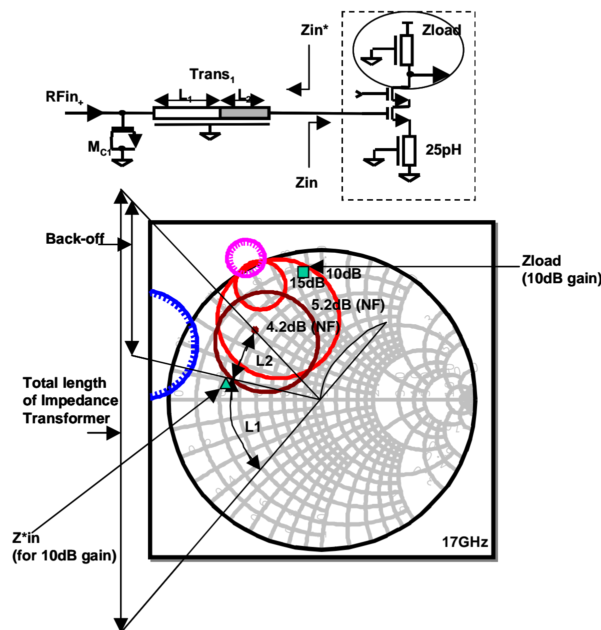

Figure 1: *Backing off* from active device's NF_{min}: length of impedance transformer's transmission line is shortened to diminish the noise contributions from lossy passives at the expense of a small increase in the contribution from the active devices, but still producing a lower noise figure for the final LNA

Traditional microwave design approaches assume high-quality passives. Thus, low noise amplifier designs primarily seek the transistor's NF_{min} and implement its optimum source (driving) impedance, so far as this does not compromise unacceptably the gain of the amplifier or its input match [13]. In contrast, when passives are implemented on a CMOS die, because of geometric constraints (more on geometric implications for on-die realizations later), their low Q makes such an approach sub-optimal. In effect, low noise amplifiers are optimally designed if backing off from the active device's NF_{min} is used. This new approach minimizes the final noise figure of the LNA by trading off a small increase in transistor noise for a much lower noise contribution from the lossy passives.

Figure 1 illustrates how the backing-off approach is applied to the definition of transmission line length of the impedance transformer ($Trans_1$) in the Input Matching Network (IMN) of the amplifier. Constant gain circles (15 dB and 10 dB gain, Z_{load} referred) and constant noise figure circles (Z_{in}^* referred) for a cascode structure with inductive source degeneracy is depicted. Note that if the design of the input matching network was done with high-quality passives the length of the impedance transformer would have been as close to L_1+L_2 (note *"L"* stands for length rather then inductance in this discussion) as an acceptable input mismatch would allow. However, once low-*Q* passives are used, making the length of $Trans_1$ be shortened to L_1, despite an increase in the cascode structure's noise, leads to smaller noise figures for the final LNA. Moreover, the pair Z_{load} and $Z_{in}*$ for 10 dB gain, identified in Figure 1, stresses that backing off can lead not only to a lower noise figure but can also lead to minimal mismatch at the input port of the amplifier. In general, the amount of back off is a function of how low the *Q* of the passives is and how slowly the active devices' noise figure changes as their driving source move away from their optimum (i.e., how small the active device's noise parameter R_n is). The disposition of constant gain circles, constant noise circles, and stability circles in the Smith-chart will change with transistor size, amount of source inductive degeneracy, and frequency of operation of the LNA. In the designs presented in this paper, for every step in the optimization process, backing off is always checked around every design point iteration.

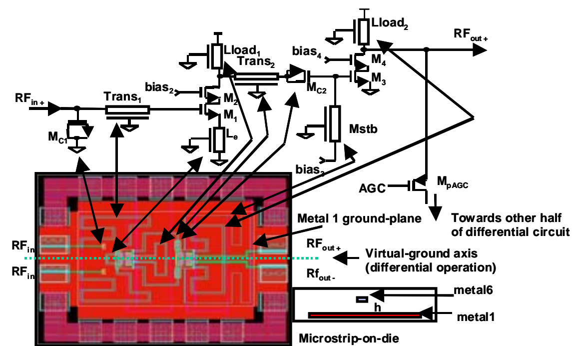

Figure 2: Schematic and corresponding layout for a 17 GHz LNA in 0.18 µm CMOS

Even though the procedure was illustrated for 17 GHz and 24 GHz LNAs, and on-die microstrip segments were used for the passives, the method is readily applicable to both lower and higher frequencies, with the only visual effect of using lumped passive components (spiral inductors) at lower GHz frequencies and distributed passive components (microstrips) at higher frequencies.

Figure 2 shows the simplified schematics and the corresponding layout for a 17 GHz LNA in 0.18 µm CMOS.

Figure 3 shows die photos of both 17 GHz and 24 GHz LNAs in 0.18 µm. These designs weren't the most compact designs possible since they also aimed at proving abrupt curves make for only minimal affect in microstrip performance on-die, and that on-die

transmission lines can be used for robust design of inductance as small as 25 pH. These 17 GHz and 24 GHz LNAs delivered final noise figures below 6 dB (world record in 0.18 μm). LNA designs at 2.4 GHz and 5.2 GHz using backing-off method delivered under 3 dB noise figures even with input matching network realized on-die, also a world record for 0.18 μm. These results qualify CMOS for 802.16 applications with a healthy margin. [14].

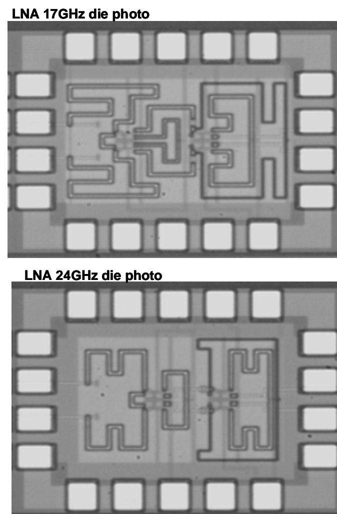

Figure 3: Die photos of 17 GHz and 24 GHz LNAs in 0.18 μm CMOS. Noise figures below 6 dB (world record) at these frequencies include input matching network (IMN) on die. At 2.4 GHz and 5.2 GHz noise figures are below 3 dB, IMN included, for the same CMOS technology.

Both 17 GHz and 24 GHz LNA designs were successful at first trial. They were designed using S-parameter measurements from laid out CMOS transistors on wafer. No CMOS modeling was used, and device sizing was still retained as a designer's degree of freedom. Larger or smaller devices could have their S-parameter calculated on the computer straightforwardly since larger devices are just smaller ones in parallel. All the microstrips on the die were electromagnetic field solved, and their S-parameter behavior was determined as well. Again, no modeling of these passives to their constitutive components was necessary. All this indicates CMOS RF and microwave designs will benefit from seamlessly merging methods and techniques from both VLSI and microwave domains, and this is discussed later in this paper.

CMOS 1/F (FLICKER) NOISE

Due to the very nature of carrier transport in CMOS transistors taking place at the interface between SiO_2 and Si, the 1/f corner frequency in CMOS transistors is much higher than the corner frequency for bipolar transistors.

At the intrinsic device level, therefore, CMOS suffers from a physically-based drawback. And, the introduction of new high-κ dielectric material in the gate of future CMOS technology nodes will tend to increase the 1/f noise levels of CMOS transistors.

RF CMOS designers have worked successfully through mitigation procedures. First, whenever fast enough, PMOS transistors are used instead of NMOS transistors as the device for oscillators and Voltage Controlled Oscillators (VCOs). It was already noted that the CMOS drawback of typically 10 dB in 1/f noise in comparison to bipolar devices could be compensated for by (a not always desirable) 4X increase in power dissipation in the final oscillator and VCO designs in CMOS. That stemmed from the experiment of paralleling four identical coupled oscillators to produce a single oscillator signal. Since the individual oscillators' signals add in amplitude, and the uncorrelated noise from the identical oscillators add in power, paralleling oscillators yield lower phase noise oscillations for the final assembly [15].

More importantly however, new understanding of the manifestation of the upconversion of 1/f noise as close in phase-noise in oscillators and VCOs opened the perspective of more sophisticated circuit-level approaches to low noise oscillators and VCO designs in CMOS [16-22]. First of all, contrary to the assumption of many designers, an assumption encouraged by Leeson's formula [15, 22], the 1/f corner frequency of the CMOS transistors will **not** be the first corner frequency of the oscillator phase noise spectrum [18-20]. Actually, experimental results have frequently indicated the incorrectness of this assumption [22]. In reality, circuit-level considerations of topological and current drive symmetry can push the oscillator phase noise first corner to within kHz frequencies from the carrier's frequency, thus yielding very low noise oscillations, even in CMOS technology where the 1/f corner can be in the hundreds of MHz frequencies. This new appreciation of phase noise readily led to a demonstration of unprecedented low-phase noise oscillators and VCO designs in CMOS, without the need to increase unduly the power consumption.

On top of that, VCOs are used in PLL- or DLL-based synthesizers in radio designs. This allows for another level of circuit design techniques to be used for further diminishing phase noise. The idea is to make the loop force the internal VCO to follow the much lower-phase

noise oscillations of an external reference source. The larger the loop gain and the loop bandwidth, the lower the phase noise for the synthesizer output signal. The loop bandwidth of PLL and DLL designs is typically 10% of the lowest frequency into the phase detector, which is normally the reference source signal. In integer-N synthesizer architecture, the source frequency (or a suitable division of that reference frequency) is defined by the finesse of the separation between the wireless channels, which might conflict with the intention of having a higher frequency for the source reference signal (for larger loop bandwidths). A solution to this conflict is found in the ever more popular Fractional-N synthesizer architecture, where the source reference frequency is allowed to be much higher and the finesse of channel separation is attended by periodically or randomly (sigma-delta synthesizers) alternating the division used in the PLL or DLL loop [15,22].

Other non-linear techniques have been proposed for low-noise synthesizers in CMOS, with ever larger loop bandwidth [16], and all these new techniques only help the case for CMOS to prove its intrinsic higher 1/f noise is no impediment to the use of this technology in radio frequency designs and systems.

Another benefit comes straight from CMOS scaling, however. Higher Q passive components can be achieved at higher GHz frequencies, since for the same geometry available for passives, Q increases with the square root of the frequency [23, 24]. Once CMOS scaling enables oscillator and VCO designs at higher frequencies, lower-phase noise operation is achieved by the use of these higher Q components, since thermal noise from passives also affects phase noise as well as the transistor's 1/f noise. Finally, dividing the output of these high-frequency oscillators, VCOs, and PLLs to get the actually used final lower frequency will also allow for another decrease in phase noise. And, as a beneficial side effect, starting with higher frequency oscillators and VCOs may result in significant savings in foot print in the silicon die, since passives at higher frequencies are smaller. Therefore, having higher frequency capabilities enabled from CMOS scaling does lead to improvements in designs, even for radios operating at much lower GHz frequencies than the frequency limits for a given CMOS technology.

CMOS RF STABILITY, MODELS AND METHODOLOGY

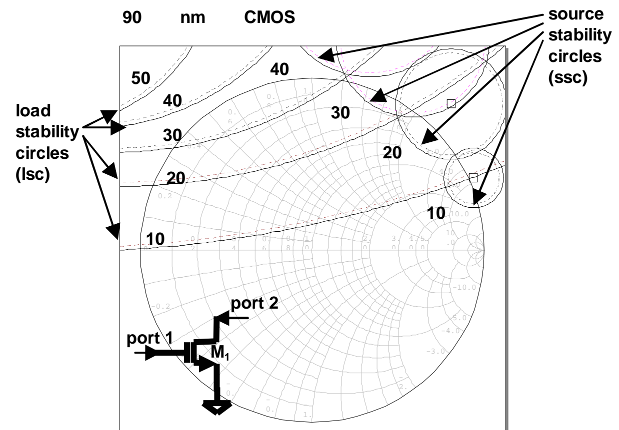

Figure 4: 90 nm CMOS stability circles: unconditional stability only after 40 GHz

As can be seen in Figure 4, a typical 90 nm CMOS transistor is only unconditionally stable above 40 GHz. As CMOS scales, the unconditionally stability region will only start at higher and higher frequencies. This doesn't necessarily preclude future RF designs at 2.4 GHz and lower frequencies necessarily, but it does require RF designers to pay close attention to the source and load impedances they use in their circuit designs when they move to use more advanced CMOS technology nodes. Not being careful will lead to oscillatory behavior in amplifiers and failure in other active circuits. As multiband radios spanning from 700 MHz to 60 GHz may be fabricated in the same CMOS process, it is very unlikely that CMOS modeling, using detailed network representations of transistors traditionally used in VLSI design, will accurately represent the devices behavior across such a large span of frequencies. Since accurate RF/microwave behavior and noise performance parameters are required, merging VLSI and microwave methods holds more promise. CMOS models plus full disclosure of S-parameter/Noise-parameter data and other relevant experimental results, will mark the new methodology to be followed by CMOS foundries and the CMOS-based industry.

This change is more pressing still when, counting on the expected CMOS scaling, some companies release transistor models with "forward-looking" adjustments that do not agree with current silicon behavior. These companies borrow from traditional VLSI methods that expect the performance of silicon transistors to always improve with time. Thus, they release CMOS models they think will be correct some time in the future when the designers eventually tape out their designs. That is not a methodology suited for RF and microwave design, which

depend on much more accurate representations of the devices used. A simple compromising change in the methods is to make these companies fully disclose the current silicon data, S-parameter, and Noise-parameter companion to any "forward-looking" CMOS model release. This way even if present silicon data and futuristic models do not agree, designers have full knowledge of this "gap" and are able to assess how significantly this gap affects their designs.

Designers on their side should be equally proficient at designing from CMOS models, experimental S-parameter and Noise-parameter data. These are complementary sets of information. Each one is useful for different aspects of the design and frequency of operation.

RF passive design also experiments with similar methodological changes. Electromagnetic field solvers have become commonly present amongst the set of CAD tools used in both silicon and package RF design to the extent of almost dispensing with detailed lump element models of silicon and package interconnects.

In the next section, designs at 64 GHz and 100 GHz are not only based on S-parameter measurements (not CMOS modeling), but they also extrapolate these measurements to both larger device sizes and much higher frequencies prior to design. That accurate representation of transistors' behavior led to success at first try, despite it being a design of completely uncharted and unprecedented high millimeter wave frequencies for CMOS.

Millimeter Wave Capabilities: 64 GHz and 100 GHz VCOs in CMOS

In order to demonstrate CMOS technology capabilities well above 10 GHz, and establish the technology potential for the full 802.16 standard, voltage-controlled oscillators were designed and demonstrated for operations at 64 GHz and 100 GHz. These were frequencies close to CMOS transistors' f_{max}. It was therefore not only a CMOS technology intrinsic capabilities demonstration, but also a circuit-level design advance in concept and methods that renders itself very well in CMOS. The transistors used were thicker gate, no-strained CMOS that exhibited f_{max} ~ 110 GHz (Figure 5).

The *unconditional* stability above 40 GHz in 90 nm CMOS technology (see Figure 4) is exploited in these novel designs. Since the device is unconditionally stable above that frequency, it allows the use of simultaneous complex conjugate matching at input and output ports of every transistor in the VCO. This matching pumps energy from the active device to the passive network optimally, *optimum pumping,* which is essential at frequencies close to f_{max}, where transistors offer little gain.

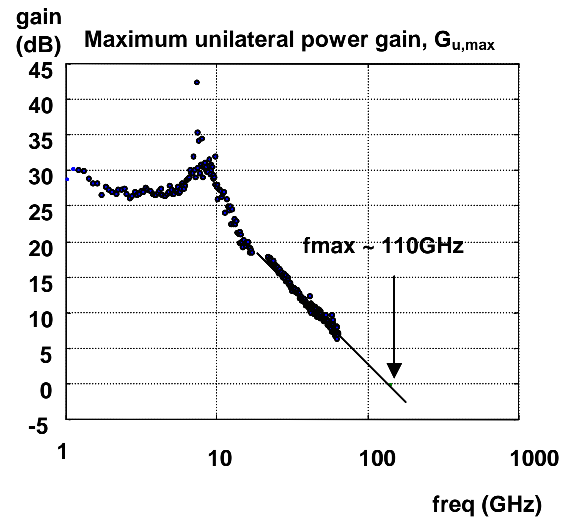

Figure 5: Maximum unilateral power gain and f_{max} of a thick gate non-strained 90 nm CMOS technology used in 64 GHz and 100 GHz VCO designs

In a typical negative-Gm LC oscillator/VCO (Figure 6a), it is required that the negative resistance, R_{in}, appearing at terminals "a" and "b" (Figure 6b) be smaller than the parallel resistance of the tank network [15]. No consideration is given to an optimum value for R_{in}. Nevertheless, optimum pumping is accomplished by considering the generalization of the LC oscillator network and its equivalent unraveled version shown in Figure 6b. A signal entering transistor M_1's gate (node "a"), appears at M_1's drain and travels through the general passive network to reach the gate of transistor M_2. This signal enters the gate of M_2, appears at its drain, travels through the general passive network and re-appears back at point "a." After this whole cycle, this signal will have experienced the same change in phase and amplitude as if it had traveled along the equivalent unraveled infinite network shown in Figure 6b from its node "a" to its node "a*."

Every single transistor in the unraveled infinite network can now be thought of as part of a chain of amplifiers. Since the transistors are *unconditionally* stable at frequencies close to f_{max}, the required Z_G^* and Z_L for simultaneous conjugate matching is promptly calculated from their reflection coefficients (Figure 6) [13,23,24]. Hence the general network (Figure 6c) transforms the impedance at the gate of each transistor, Z_G, into the required load impedance, Z_L, at the drain of the transistor of the preceding stage. In a lossless passive network, this impedance transformation preserves the coefficient of mismatching, M_S, along the unraveled chain (Figure 6c) [13], which makes this oscillator topology a physically realizable one.

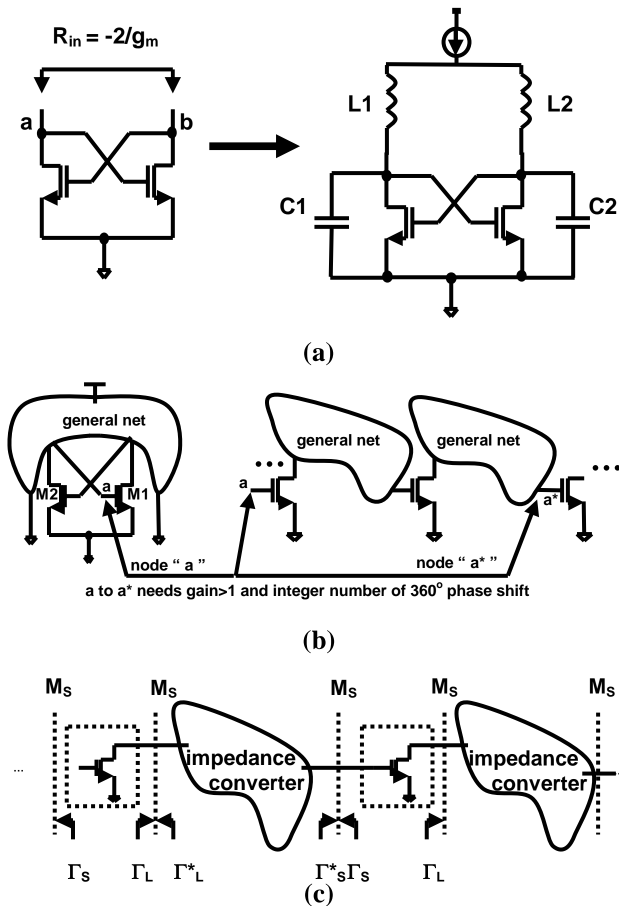

Figure 6: From negative-g_m to optimum pumping

Depending on the transistor technology, the number of stages required for a multiple-of-360° phase shift in the signal may be awkwardly high. Figure 7 shows how delay lines are added in one of the three possible general cases for the optimum pair Γ_s and Γ_L [7]. The impedance transformation along these distributed networks crosses the horizontal-axis (real impedance axis) of the Smith-chart along one of its transmission lines. At this cross, a lossless transmission line segment of characteristic impedance defined by the point of cross can be added to the VCO's passive network without disturbing the optimum-pumping impedance transformation. The length (delay) added depends on the number of stages desired for the final VCO. It is important to note the optimum-pumping method exploits the unconditional stability of the transistor whereas the standard microwave approach exploits the device instability for oscillator design [13,23,24].

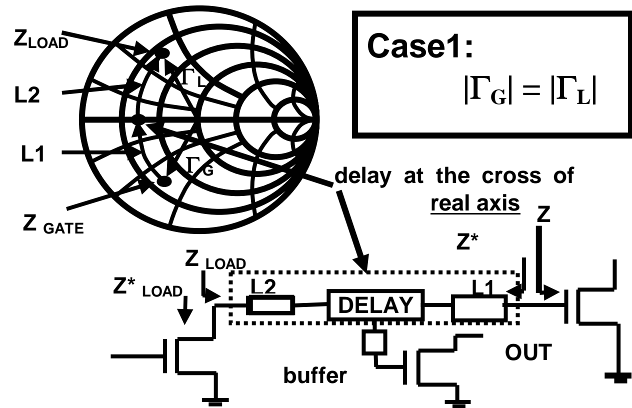

Figure 7: Strategic delay element introduction: "L1" and "L2" are lengths of transmission lines

In this work, no commercial CMOS model was used. 90 nm logic CMOS transistors were laid out and characterized by S-parameter measurements up to 50 GHz. The transistor S-parameters were extrapolated to 64 GHz and 100 GHz. The distributed passive networks were realized using microstrip-on-die, with ground plane in metal-1 and traces in metal-7 layers. These passive networks were Electromagnetic Field solved using a commercial program [25]. Ground plane in metal-1 isolated the passive networks from silicon substrate losses.

Figure 8 shows the photo die with a description of the components of both 64 GHz and 100 GHz VCOs. Signals were taped from the VCO's core at its lowest impedance (lowest swing) with a high-impedance tap for minimum disturbance of oscillations.

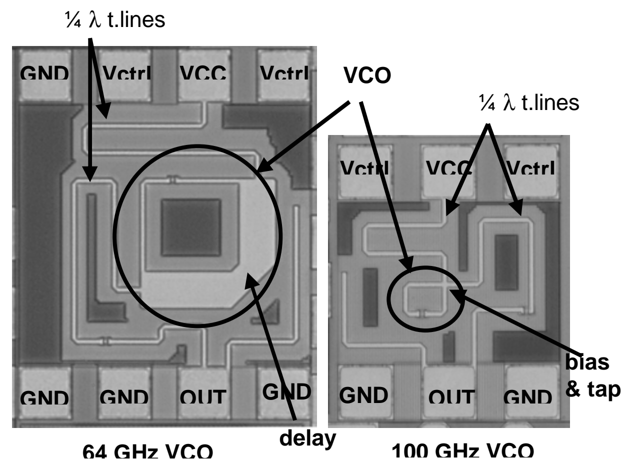

Figure 8: 64 GHz and 100 GHz VCOs: single-transistor core die photo

The ¼-wavelength-transmission-line tap from the VCO core to the transistor buffer further diminished the signal to be measured. The pads are part of the output network of the buffer; microstrip stubs were added to properly

tune the pad impedance to maximum buffer gain (Figure 8).

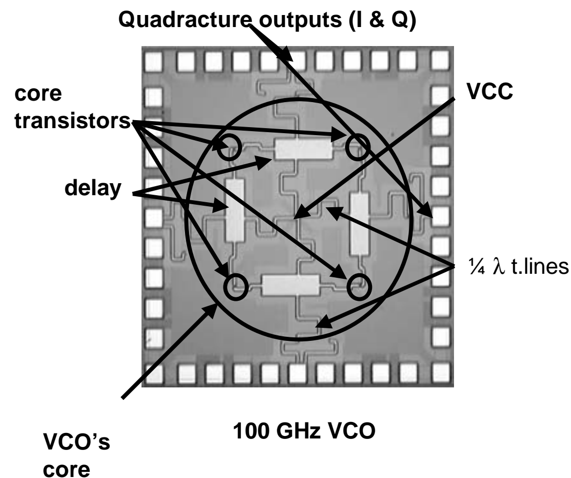

Figure 9: 100 GHz VCO: 4-transistor-core die photo

The 64 GHz and 100 GHz VCO signals were measured to be centered at 63.6 GHz and 103.9 GHz. This was calculated by simulating that the measured signal for both 64 GHz and 100 GHz meant a 0.4 Vp-p swing at the VCOs' cores at their largest swing point. Both VCOs used a 1.0 V power supply and drew 20 mA (64 GHz) and 30 mA (100 GHz) of current. Both VCOs were completely functional from -50°C to 110°C. Center frequency changed approximately 5 GHz (100 GHz) and 3 GHz (64 GHz) in this temperature range, because of the relatively small temperature dependence of the phase shift contribution from the passive network in the VCO core. Consistently, the gains for both VCOs were in the range of 2 GHz/V, either through body bias or supply voltage control. These were successful designs at first try that firmly established CMOS capabilities well into millimeter wave frequencies.

Figure 9 shows a 100 GHz 4-transistor core oscillator that was designed by adjusting the delay elements. In this topology quadracture output signals are produced.

RF AND DIGITAL PROCESSOR IN THE SAME DIE

Once CMOS technology capabilities for RF applications is established even to extreme 100 GHz frequencies, the next step is to go beyond standalone radio design. Communications and computing have synergies that can be exploited in RF and digital processor integrations in the same die.

In order to demonstrate that such an integration is possible even in the extreme case of a very noisy digital processor with clock frequencies in the GHz range and delicate RF circuits typically sensitive to at least -76 dBm signals from the antenna, we started by measuring how noisy the substrate of a Pentium 4 is.

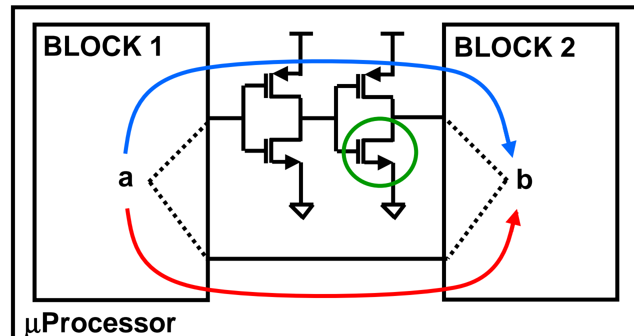

Figure 10: Redundant logic delay chains: unused transistors engineered into noise sensors

Intel processors are taped out with extra logic delay chains for pre-product investigations (Figure 10). These extra transistors are left in the commercial microprocessors without doing any work. These redundant transistors were engineered as substrate noise sensors by Focused Ion Beam (FIB) work from the back of the die. These transistors were unconnected from the rest of the microprocessor circuits and their terminals were brought externally onto the back of the wafer (Figure 11). Substrate activity (noise), which modulates the body bias of these transistors, is displayed by the spectrum analyzer (Figure 12). Figure 11 shows the layout as seen from the back of the die, and it shows the vias and wires for connecting the source, drain, and gate of a test transistor. 1.2 mVrms noise measured at the drain of a 5 µm-wide noise sensor located at the center of the die translates (by the noise sensor transfer function) to 100 mVrms noise on the substrate. These measurements corresponded to 15 W power dissipation produced by the excitation of the 1 GHz clock grid as can be seen by the noise spectrum developed. Assuming substrate noise power is directly related to the microprocessor (dynamic) power dissipation [26], the same microprocessor dissipates 55 W and thus produces 190 mVrms substrate noise at full operation. Because of a typical activity of 10% (for the logic gates), this additional substrate noise on an actual application of this microprocessor, is concentrated from dc to 150 MHz.

The fundamental insight guiding this research is that high-performance microprocessors, with clocks at GHz frequencies, develop substrate noise with a spectrum structure that can be exploited to place RF narrow-band signals in valleys of low-substrate noise levels in the frequency spectrum. This can be achieved by placing and retrieving feeble bandwidth-limited RF information

signals between the harmonics of the clock, and away from the intense substrate noise's components generated by the random logic gate activity (Figure 13). A commercial 1.5 V 55 watts 1 GHz 104-million-transistor (Pentium 4) digital microprocessor and a 50 MHz-bandwidth-76 dBm-sensitivity wireless receiver with a carrier frequency at 2.4 GHz and 5.2 GHz FCC's ISM bands is analyzed for possible integration on the same die. For simplicity, but without loss of generality, a direct-conversion architecture is assumed for the RF receiver. A band-selective LNA amplifies the feeble RF signals from the antenna to bring their level sufficiently above the (attenuated by isolation) substrate noise upon downconversion to baseband (Figure 13). Isolation requirements for Signal-to-substrate Noise-Ratio (SsNR) higher than 20 dB (BER<10^{-9}) are derived, and an isolation scheme with only minimal technology addition (deep nwell structures) is presented. The measured high frequency performance of 140 nm logic CMOS (f_{max} and f_t at 100 GHz and 60 GHz, respectively) is not significantly affected by placing them in the required deep nwell structure.

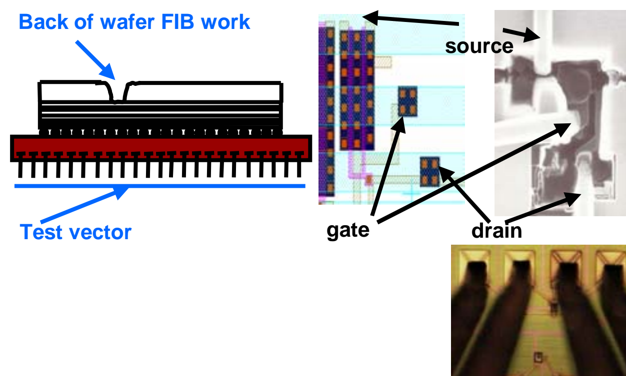

Figure 11: Focused ion beam (FIB) work: transistor-noise-sensor is accessible from the back of the packaged processor. The processor is excited by standard test vectors.

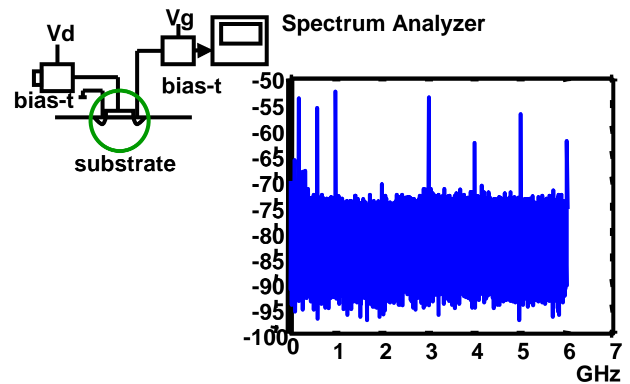

Figure 12: Pentium 4 substrate noise spectrum

The isolation for wireless receiver integration needs at the very least to guarantee that the substrate noise (both in-band and out-of-band frequency components) does not disturb the bias voltages used in the wireless receiver front-end. Gate overdrive in MOS transistors used in the RF front-end, are typically around 200 mV, and a 10% disturbance in these voltages means isolation should provide 20 dB (|20log(20 mV/190 mV)|) across the entire relevant spectrum. There are, however, much more strict requirements for isolation, as will be seen next. The typical 10% activity factor on the logic gates makes the random logic activity develop only a 0.0025 fraction of its substrate noise power over the 50 MHz bandwidth on the 2.4 GHz ISM band and only a 0.0014 fraction over a similar 50 MHz bandwidth on the 5.2 GHz ISM band, (Table 1) [9].

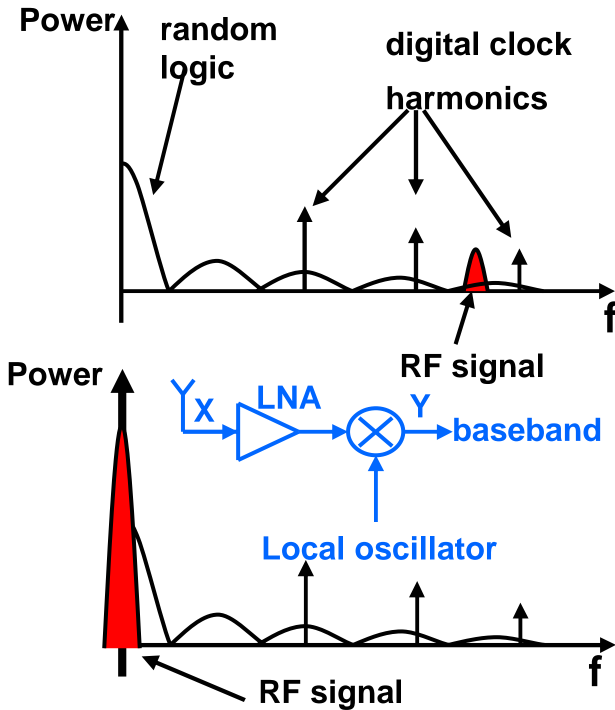

Figure 13: Exploiting substrate noise spectrum structure: feeble RF signals are placed at valleys of low noise levels

Table 1: Substrate noise power

Total substrate noise at die center	Substrate noise from 1GHz clock grid	Substrate noise from digital logic (10% activity relative to clock frequency)	2.4GHz in-band substrate noise from logic (50MHz bandwidth)	5.2GHz in-band substrate noise from logic (50MHz bandwidth)
190.0mV$_{rms}$	109.7mV$_{rms}$	155.1mV$_{rms}$	7.76mV$_{rms}$	5.80mV$_{rms}$

Table 2: Isolation and LNA gain tradeoff

Goal:	SsNR>20dB after down-conversion inside 25MHz of base-band bandwidth (direct conversion RF receiver assumed for both 2.4GHz and 5.2GHz ISM bands)					
LNA gain	isolation	2.4GHz in-band SNR (from logic activity at LNA input after isolation)*	5.2GHz in-band SNR (from logic activi-ty at LNA input after isolation)*	Base-band substrate noise from logic (25MHz band-width after isolation)†	2.4 GHz transceiver 25MHz Base-band SsNR, (after down-conversion to base-band)‡	5.2GHz transceiver 25MHz Base-band SsNR (after down-conversion to base-band)‡
10dB	80dB	36dB	39dB	2.5µV$_{rms}$	30dB	31dB
20dB	70dB	26dB	29dB	7.8µV$_{rms}$	24dB	26dB
30dB	60dB	16dB	19dB	25µV$_{rms}$	15dB	18dB

Since the 50 µV (-76 dBm) RF signal from the antenna needs to be amplified enough before being downconverted to baseband (where it will face the low-frequency components of the substrate noise produced by the random activity of the logic gates), combinations of LNA's gain and isolation levels are presented with the final SsNR achieved in Table 2 [9].

As an enabling requirement, SsNR>20 dB aims for a healthy margin for achieving system Bit Error Rate (BER) better than 10^{-9}. Hence, LNA's gain of 20 dB and its isolation level of 70 dB are the borderline enabling values for integration. Note that the out-of-band components of the substrate noise are not amplified by the band-selective LNAs, and any mixing of out-of-band substrate noise and the RF signal will be attenuated by the conversion loss of the operating non-linearity [9]. Note also that the 50 MHz bandwidth at RF frequencies becomes 25 MHz bandwidth at the baseband, diminishing the amount of substrate noise captured at the baseband. As mentioned, the final 70 dB isolation requirement for integration is much stricter than the requirements for merely not disturbing the bias voltages in the RF front-end. As will be seen next, this total of 70 dB isolation will be partitioned into on-die isolation and layout- and circuit-level isolation. We achieve the 50 dB of on-die isolation by use of a deep nwell, and therefore we guarantee that the bias voltages of the RF front-end are not disturbed by the substrate noise from the digital circuits.

70 dB substrate noise isolation between integrated subsystems is realized by adding isolations from on-die implanted deep nwell structures (>50 dB) to isolations from layout and fully differential circuit topology (20 dB). An on-die isolation higher than 50 dB is realized by implanted double deep nwell structures using two circuit-level methods: substrate noise trapping and floating deep nwell, shown in Figure 14.

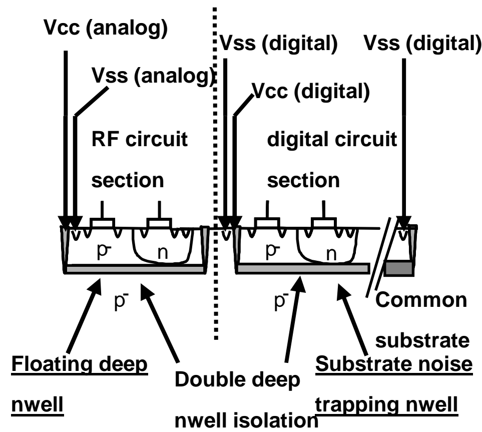

Figure 14: Deep nwell hook ups and biasing

The deep nwell covering the digital circuit section attenuates the substrate noise passing through the deep nwell's walls towards the common substrate (substrate noise trapping). Once into the common substrate, the attenuated substrate noise will proceed towards the deep nwell protecting the RF circuit section, making that whole deep nwell change its electric potential uniformly (floating deep nwell). These two mechanisms are more effective the more conductive is the deep nwell implant in relation to the substrate, and the smaller the area of the floating deep nwell.

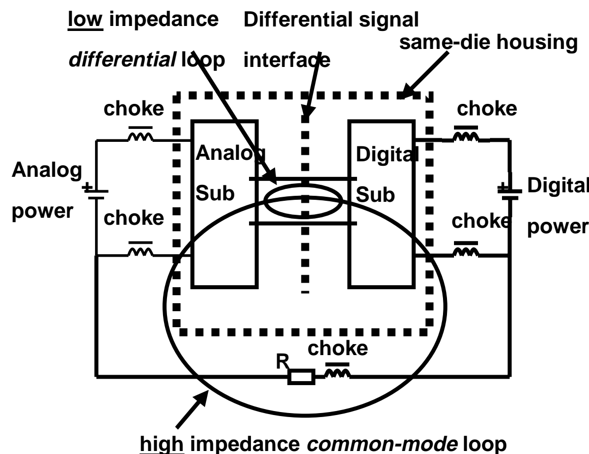

Figure 15: Differential signaling between analog and digital subsystems

In order to realize these two effects, the power supply for the subcircuits sections and signaling between the two sections follows the description in Figure 14 and 15. Note both Vcc and Vss power supply connections for both subcircuits are kept independent and never connected on-die. Moreover, the signaling between the two subsections is differential. This differential signaling leaves the analog and digital subsystems to "fluctuate" relative to each other.

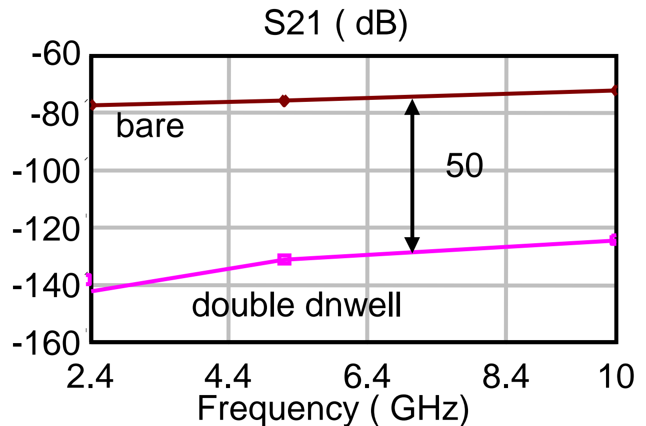

Figure 16: Double deep nwell isolation (aggressor and victim surrounded by nwell) vs. no deep nwell isolation

The differential interface defines a preferred path for signals from one subsystem to another. Substrate noise from the digital subsystem will travel towards the analog subsystem through the common mode loop. Since this common mode loop has several choke inductors along its path, it will present a high impedance for currents (Figure 15) and will strongly attenuate the substrate noise sensed in the analog subsystem. This on-die isolation was analyzed using a commercial electromagnetic field solver. Isolation between subcircuits reaches 50 dB even for highly conductive (lossy) substrate ($1x10^3$ S/m) with no epi-layer, and separation between analog and digital subcircuits as small as 200 µm. On-die isolation exceeds 50 dB if an epi-layer (5-125 S/m conductivity) is added in the field solver simulations, thus benefiting the state-of-art technology of high-performance logic CMOS technology.

Figure 16 shows results for 50 µm-thick deep nwell lateral walls, which is appropriate for subsystem isolation (not for individual transistor isolation). The 50 dB isolation levels for thick-wall double-deep nwell isolation (both aggressor and victim covered by deep nwells) and frequency characteristics agree with experimental results obtained by CMOS foundries later [27].

For the additional layout- and circuit-level isolation, RF circuits are fully differential with layout of matched devices based on a common centroid. Transistors sized with W=250 µm-460 µm (common in 2.4 GHz/5.2 GHz RF designs with 140 nm CMOS technology) V_t and L_{min} mismatches lead to g_m mismatches smaller than 10%, which imply >20 dB common-mode rejection. Once

substrate activity passes to the circuit signal lines with some attenuation, layout- and circuit-level isolation combined reaches above 20 dB as desired. An additional "vertical grid" was simulated in the electromagnetic field solver to minimize coupling between on-die metal traces, which imposes also an isolation higher than 70 dB for this path. This vertical grid was connected to the digital Vss and finally completed the total isolation enabling RF-digital processor integration.

Table 3: Body bias and RF performance

Vg (V)	Vd (V)	Vb (V)	Id (mA)	|S21| @ 5.2 GHz	Fmin @ 5.2 GHz (dB)
0.7	0.7	-0.5	30.02	3.253	1.05
0.7	0.7	-0.25	35.36	3.248	1.07
0.7	0.7	+0.25	49.82	3.122	1.14
0.7	0.7	+0.50	60.58	2.979	1.20

Due to the introduction of deep nwells, body biasing becomes an additional degree of freedom for both digital and RF circuits. Reverse and forward body bias, respectively, diminishes and augments the current driving capability (hence g_m) of the devices as can be seen by the change in Ids with Vb in Table 3. However, as the current driving capability increases, the drain junction capacitance also increases as that junction becomes less reverse biased, and the overall effect is a diminishment in the RF performance with forward bias as represented by the measured |S21| in Table 3. That is a clear departure from the effect of body bias in digital circuitry where the capacitances at the output of logical gates are dominated by the gate capacitance of the following gate, and any increase in current-driving capability implies a gain in performance. Note also that, as expected, there is no apparent effect of body bias on the carrier heating (drain current excess thermal noise) by the high horizontal electric field in the channel as F_{min} merely tracks variations in the device gain (|S21|) – higher |S21| (Table 3). Table 4 compares the behavior of identical transistors inside and outside the deep nwell. A small but perceptible increase in channel resistance diminishes the driving current capability, diminishes the RF performance (|S21|), augments F_{min}, and augments Rn (the device in the deep nwell departs from the optimum noise performance faster with source impedance than the identical device outside the well). Nevertheless, these are not compromising effects. Similarly, from 25°C to 110°C the device performance inside and outside the deep nwell showed a less than 10% variation in RF and noise parameters.

Table 4: Transistor inside vs. outside deep nwell

Ids (mA)	Ids (dnwell) (mA)	|S21| @5.2 GHz	|S21| @5.2 GHz (dnwell)	Fmin @5.2 GHz (dB)	Fmin @5.2 GHz (dnwell) (dB)	Rn/50 @5.2 GHz (dB)	Rn/50 @5.2 GHz (dnwell) (dB)
48.0	46.3	3.338	3.036	1.15	1.71	0.22	0.35

Mixed-signal integration for high-performance System-on-a-Chip (SoC) is thus enabled with minimal technology modification, by adding deep nwell structures. By exploring the spectrum structure of the substrate noise of a high-performance microprocessor (1 GHz 55 W) with a clock at GHz frequencies, and placing the feeble RF signals (for a 50 MHz, –76 dBm-sensitivity receiver) received from the antenna between harmonics of the clock, we have shown that 70 dB of isolation is sufficient to enable RF-high-performance digital processor integration.

Note that this was an extreme case of RF and digital processor integration in the same die. RF delicate circuits are more likely to be integrated with sub 2 W digital circuits or processors, instead of 55 W and above digital processors. Therefore, less isolation between digital and RF circuits is likely to be the typical case and deep nwell structures might be only seldom used. Our investigation, accordingly, supported the feasibility of RF and digital processor integration in the same die with comfortable margins.

CMOS SYSTEM ON A PACKAGE (SOP)

After digital substrate noise is successfully handled, silicon area availability is the next and final road block to be cleared in the path to RF and digital processor integration in the same die. Multiband radios do require a large number of passive components that take considerable area on-die and are also non-scaling components. This area road block will be adequately cleared in this section as a side effect of a creating high-performance wireless SoP.

Higher performance RF and microwave transceivers require high-performance active devices and high-quality passives. On the silicon die, only the former is available. Integrated passives have poor quality factors (Q), typically around 5 or 7 at low GHz frequencies. A significant improvement in such a scenario is found when passives are implemented on the package substrate. That's because Q is a ratio of energy accumulated in the component to its losses per cycle of the operating frequency. Therefore, since energy is associated with the **volume** occupied by the electric and magnetic fields of

the passive component and the losses are predominantly associated with the **surface** of the conductors used in those passives at low GHz frequencies, just by being able to use more volume leads to higher quality passives. In this sense, the height from the bottom metal layer to the top metal layers in the silicon back-end is around 5 µm, whereas the metal layer separation on the package substrate is around 30 µm. Then, a 6X improvement in quality for the passives could be expected by moving a passive component from the silicon die to the low-cost package substrate. Unfortunately, dielectric losses on the package substrate (which uses organic materials) is significantly higher than the SiO_2-based interlayer dielectric used on the die, and final quality factor improvement, though still realizable, is somehow lower than 6X [10].

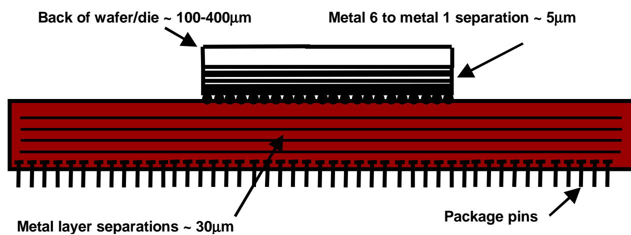

Figure 17: Die and package metal stacking and dielectric separations

It is interesting to realize that despite being higher than on-die, the still relatively modest Qs of passives on the package warrant optimization of the final LNA design by backing off, explained earlier. In order to better appreciate this, Figure 18 shows that depending on the Q being 5 or 10 for inductors in the IMN, a floor of 1 dB noise figure for the LNA is already established if too-high inductor values are placed in that IMN. This means that transistors in the LNA need to be properly sized with the minimization of inductance in the IMN included. Note that according to Figure 18, for instance, for an LNA at 2.4 GHz it is necessary to use inductor values below 8.5 nH in the Q=10 curve, to have any chance of making a 1 dB noise figure LNA, even if the rest of the LNA is completely noiseless.

Similar benefits are accrued by other RF key components. Oscillators and VCOs also develop less phase noise if higher quality passive components are used, since all the noise contributors (not only transistor's 1/f noise) influence phase noise, as was discussed in the 1/f section of this paper.

In RF Power Amplifiers (PAs), the moving of passives from the die to the package is not just a benefit but actually an enabling development. As CMOS transistors scale, less voltage swing is tolerated at their terminals, and a high quality impedance converter needs to be placed between the antenna and transistors' drain for high-power transmissions. High-quality impedance converters are just not available on-die. Moreover, the impedance converters solve the problem of *high voltage swing* by trading it for *high current handling* capabilities. This means the RF choke used in the PA of Figure 19 needs to carry currents on the 1A peak levels or more at times. For the sake of reliability, such wide metal traces have to be used on die to support these currents that the RF choke becomes plagued with parasitics and then it is useless even at low GHz frequencies. Moving the passives to the package neatly solves the problems of the high-quality impedance converter and the high-current handling capabilities of the RF choke.

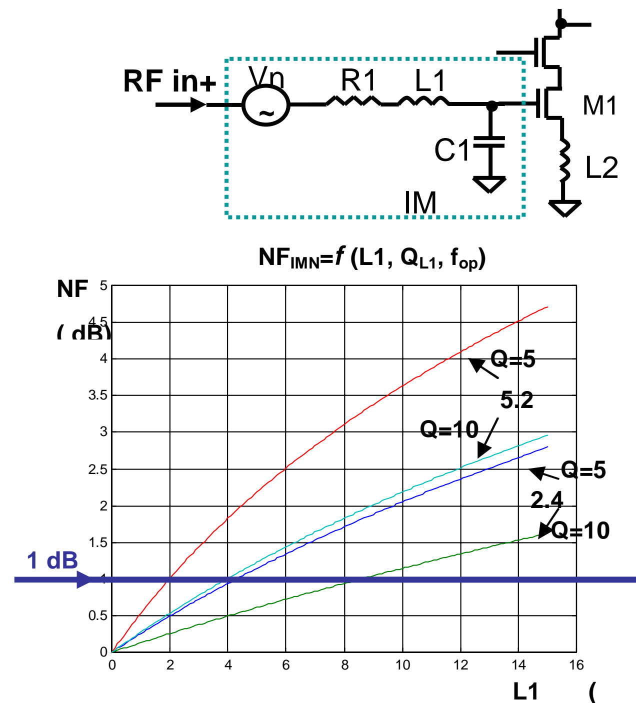

Figure 18: Input-matching-network-limited LNA's noise figure

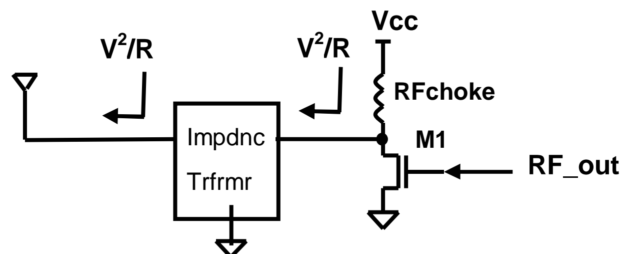

Figure 19: Conceptual description of power amplifiers

Figure 20 shows the area of a flip-chip package where passives can be realized by trace engineering (no discrete components added), and a 3D blowup of an example of moving impedance transformers and RF chokes to the package substrate. Figure 21 depicts the 1-to-1 correspondence between schematics and trace layout realization for the PA's network of Figure 20.

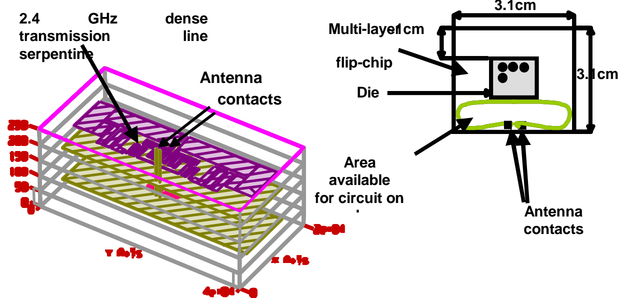

Figure 20: High-quality RF passives realized by trace engineering on the flip-chip package substrate

More compact realizations of the PA's network can be developed, and Figure 22 shows how a power combination of four identical PAs can be realized on-die, occupying a small area. The PA's transmission power in the range of 0.5 W at 5.5 GHz can be readily achieved with low voltage (1.2 V) transistors.

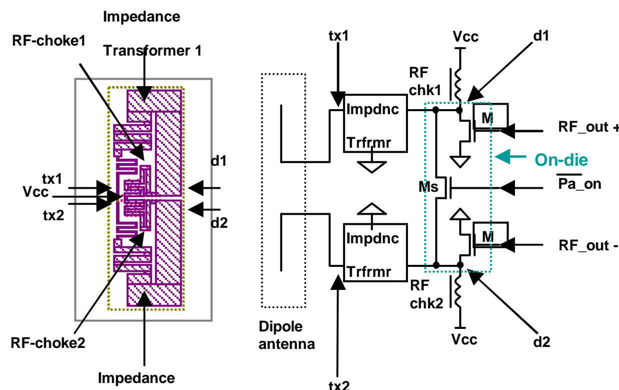

Figure 21: Schematic and trace layout correspondence for a PA with its entire passive network on the package substrate

Moving RF passives to the package substrate can be carried on to the extreme of moving all the big passives out of the silicon die and onto the package. Such a move is supported by the large pin count capability of flip-chip packages and ultimately will lead to leaving only the transistors on-die. Having only the radio's transistors on-die makes the radio occupy only a small area in that die. Figure 23 shows a concept where all the radio's passives are moved to the package surface and the radio becomes a slim area on the north side of the die. The rest of the die is now available to host a digital processor. Note that given the already densely occupied processors and chipset dies, if we are to integrate radios into those dies, the radio needs to be of minimum area. Moving the passives to the package then becomes again an enabling technology.

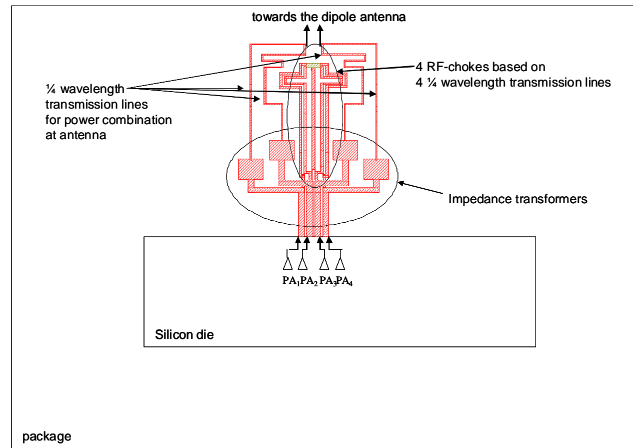

Figure 22: Power combining of 4 PAs on the package: 0.5 W of power transmission with 1.2 V transistors

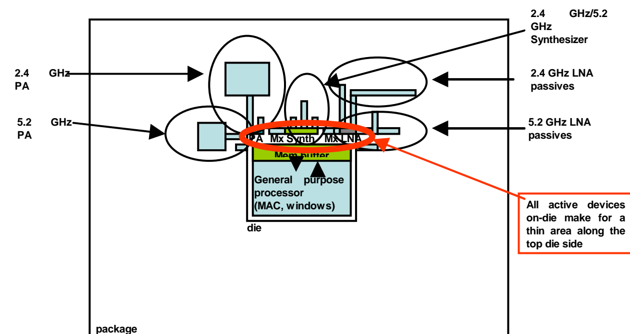

Figure 23: All-passives-on package radio concept. Radio becomes a slim silicon area north of the die, and a general-purpose digital processor is hosted on the same die.

Another path for the SoP with all (or most of) the RF passives moved to the package substrate is explored later in this paper.

SIGMA-DELTA ADCS AND DACS: TRADING VOLTAGE RESOLUTION FOR TIME RESOLUTION

Analog to Digital Converters (ADCs) and Digital to Analog Converters (DACs) are the specialty circuits at the interface between the RF front-end and the digital communication processing circuits. It is important to point out these analog specialty circuits are in fact influenced on the architecture and circuit level by CMOS scaling and the new requirements of high performance CMOS radios.

As CMOS scales, lower voltages and integrated components variations (mismatches) become higher and higher barriers for voltage resolution. Fortunately, scaling delivers higher and higher speeds in the circuits and enables large oversampling ratios for both ADCs and DACs operations. Large oversampling ratios allow for a directly proportional diminishment in (kT/C)-limited (thermal noise limited) capacitor sizes used in switching circuits [28, 29]. Clever high oversampling circuit techniques can make systematic offset produced by mismatch in the components show up as high-frequency noise, which can be readily filtered in order to achieve a high number of bits resolution. Oversampling also alleviates the anti-aliasing analog filtering order prior to the ADC blocks, and quantization noise can be shaped so that its frequency content is higher away from the frequencies of interest for the information being processed [30].

More importantly, radio signals are bandpass in nature. Before downconversion to baseband, those signals are made of a narrow band information signal on a higher frequency carrier. These signals can appropriately be tackled with sigma-delta ADCs and DACs, in particular the bandpass version of these, where all the benefits mentioned above for trading off voltage resolution for time resolution are at the core of these converter concepts. Oversampling ratios can reach values well above 50 (bandpass signal width to sampling frequency) [28, 29].

It is important to relate this change in gears for ADC and DAC converters due to CMOS scaling to a disruptive effect in radio transceiver architecture: these new ADCs and DACs allow for simplified RF front-ends and synthesizers in multiband multiprotocol radios. That is because the RF front-end will not, for instance, chase the narrow channels anymore during communications as defined by 802.16. Chasing narrow channels is now moved to the digital domain, since high-speed ADCs support a much larger bandwidth to be processed in the receiver, and high-speed DACs allow for offsetting signals for proper channelization prior to sending them to the RF transmitter.

Flexible Radios: a Practical Vision

The CMOS-based computer industry takes full advantage of CMOS scaling to produce always changing ever more powerful computing platforms. This was thought to be in fundamentally stark contrast to the standards-driven communications industry.

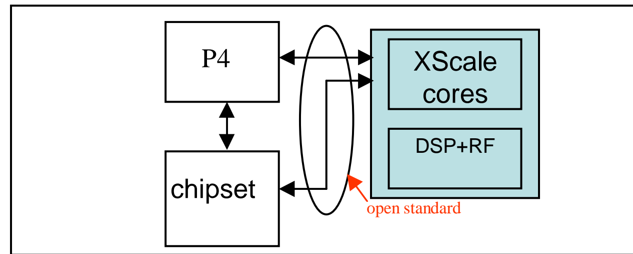

Figure 24: Flexible radios: a PC platform for merging computing and communications under always-evolving communication standards

Despite that, the reality of recent years and plans for the foreseeable future appear to show a path for further integration of computing and communications. The apparent paradox disappears when one considers communication standards are always evolving documents.

The standards themselves generate new standards and addenda to standards are always being made. Standards serve as guidelines for products, and these products at a given time only attend to a limited subset of recommendations in the standards to warrant a compatibility stamp like "Wi-Fi" or "WiMAX." Other parts of the standards are left for future implementation. In such a state of affairs, computing and communications do share the always-evolving aspects that are the spirit of the CMOS business model.

At the implementation level, multiband, multiprotocol radio for always-evolving communication standards is too complex a system to fit in a Pentium or chipset die. It would be probably better to start thinking that the PC motherboard will be a multiprocessor platform whose ecosystem will be populated by new chips besides the Pentium and chipset.

Figure 24 illustrates in a highly simplified abstraction the addition of a flexible radio to a multiprocessor PC platform. Note the suggestion that Intel® XScale® technology should become the general-purpose processor to handle all aspects of reprogrammability and hardware switchability of the flexible radio. XScale would be also in charge of a software-MAC (for easy reprogrammability) and all network layers of operation for the radio.

Figure 25 depicts a flexible radio concept and its realization as one package and two silicon chips. This concept exploits all the CMOS technology and package

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advancements discussed in this paper. Note that the two chips on the same package is only a suggestion, not the only possible solution. Nevertheless, this particular configuration allows for more surfaces on the package onto which the RF passives can be realized.

Note the addition of an Ethernet interface in die 1 of this flexible radio realization (Figure 25) allows for easy access and reprogramability/reconfigurability in case this flexible radio is taken out of the multi-processor PC platform and placed as a stand alone core component of radio base stations.

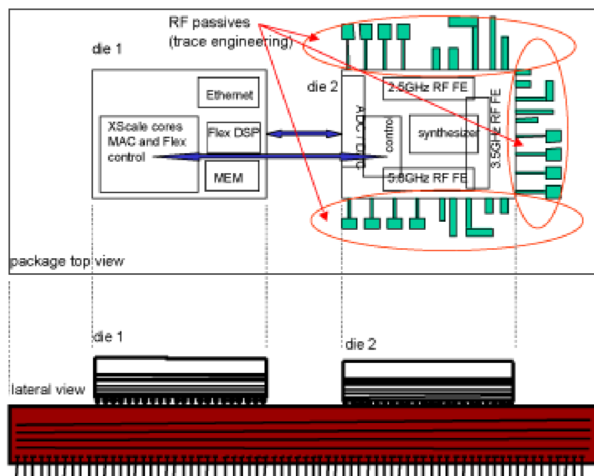

Figure 25: A flexible radio realization: top and lateral view of a realization with two dies and one package. More package surface for the RF passive network.

CONCLUSION

CMOS radio capabilities were demonstrated from RF circuits at 1 GHz in 1995 to millimeter wave circuits at 100 GHz in 2004. Intrinsic CMOS transistors' physical deficiencies have found adequate compensation in innovative circuit-level solutions. These solutions exploit and advance the understanding of fundamental mechanisms behind excess thermal noise and 1/f noise processes in semiconductor devices and how it affects circuit performance. Exploitation of digital substrate noise spectrums and advances in CMOS packaging enabled superior performance for CMOS-based wireless SoP solutions.

Building on these developments, a practical flexible radio concept can be realized. This concept recognizes the always-evolving nature of communications standards as akin to the constantly evolving computer industry. This concept supports the seamless merging of computing and communications, and CMOS is very well posed to be the technology to enable this merging.

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