White Paper

Intel is Leading the Way in Designing Energy-Efficient Platforms

Introduction

The last quarter century has seen enormous progress in the performance and capabilities of servers, desktop computers, laptops, and handheld devices. These gains have only increased the hunger for faster operation, greater functionality, lower prices, and smaller, more portable form factors. The exponential growth in data all around us is also playing a key role. It is creating demand in mainstream computing for high-end applications, and this in turn can drive up the energy used by computing systems. Designing for energy-efficient performance is key to ensuring that new systems can support high-end applications without dramatically increasing energy consumption. This requires a fundamental rethinking on how to deliver new levels of performance within a given power envelope.

Intel has continually led the way in delivering superior solutions that have ignited each new leap in performance. Similarly, Intel has a long history of leadership in improving the overall energy efficiency of computing. At the same time demand is growing for new and more powerful computing applications, customers are also increasingly concerned about energy efficiency. Energy costs are increasing around the world, and society is becoming increasingly aware of the environmental impacts of energy generation and consumption.

Expertise in developing the highest-performing chips and a history of innovation in power management technologies put Intel in the ideal position to drive the next generation of more powerful, yet more energy efficient, computing and communications devices. The current generations of desktop, laptop, and mainstream server processors based on Intel® Core™ microarchitecture are the most energy efficient Intel has ever produced—and some of the most powerful. And Intel is researching to push the energy-efficient performance of future products even further by developing silicon and platform technologies and enabling highly threaded software, with a goal to deliver platforms using processors with tens or even hundreds of cores in the coming decade.[1]

In order to deliver such energy-efficient platforms, a holistic effort is required across all common platform components—processors, hard drives, power supplies, graphics cards, fans, displays, and more. Intel was the first company to see the need for a holistic approach to energy efficiency and has been successfully employing this holistic approach in designing platforms for many years. As a result of Intel's leadership, high-end computing systems have made tremendous gains in energy efficiency in recent years. Today Intel's solutions to energy efficiency and the accompanying thermal issues are an important part of the transition to multi-core platforms that utilize many of its core technology advances. These include Intel's advanced power-efficient microarchitectures, industry-leading silicon technologies, and manufacturing expertise, world-class research, power-aware technologies, and unmatched ecosystem-building capabilities. The commitment to greater energy efficiency also builds on the well-established Intel tradition of being an industry leader in environmental issues.

Intel® multi-core platforms will offer new capabilities and enhanced user benefits across mobile, desktop, and server segments. These include:

- Higher performance blade servers with smaller footprints that deliver lower operating costs through greater energy efficiency
- Smaller, thinner form factors and extended battery life for mobile devices
- Better application responsiveness in multi-tasking environments
- High-performance computing (HPC) technology for new applications

Energy Efficiency and the Shift to Multi-Core Platforms

Gordon Moore, one of Intel's founders, forecast a doubling in the number of transistors in a given area approximately every two years and that the speed of those transistors would increase—a prediction that came to be known as Moore's Law.

For nearly four decades, Intel has set the pace and driven Moore's Law scaling by continuing to shrink the already miniscule size of silicon devices (Figure 1). Now, Intel researchers face the challenge of working within the physical limits of atomic structure for scaling transistors while still managing both power and heat. (Interestingly enough, Moore raised this prospect of a thermal problem in his original 1965 paper by saying, "Will it be possible to remove the heat generated by tens of thousands of components in a single silicon chip?") In response to these power and thermal challenges, Intel is aggressively pursuing research into both conventional and unconventional technologies. This research includes introducing many new and exciting technologies and innovations in materials, designs, and architectures. Managing power and heat has always been a key factor in Intel's chip design as the company's long history of innovation in this area has shown. This innovation was evident in the Intel® Centrino® mobile platform,

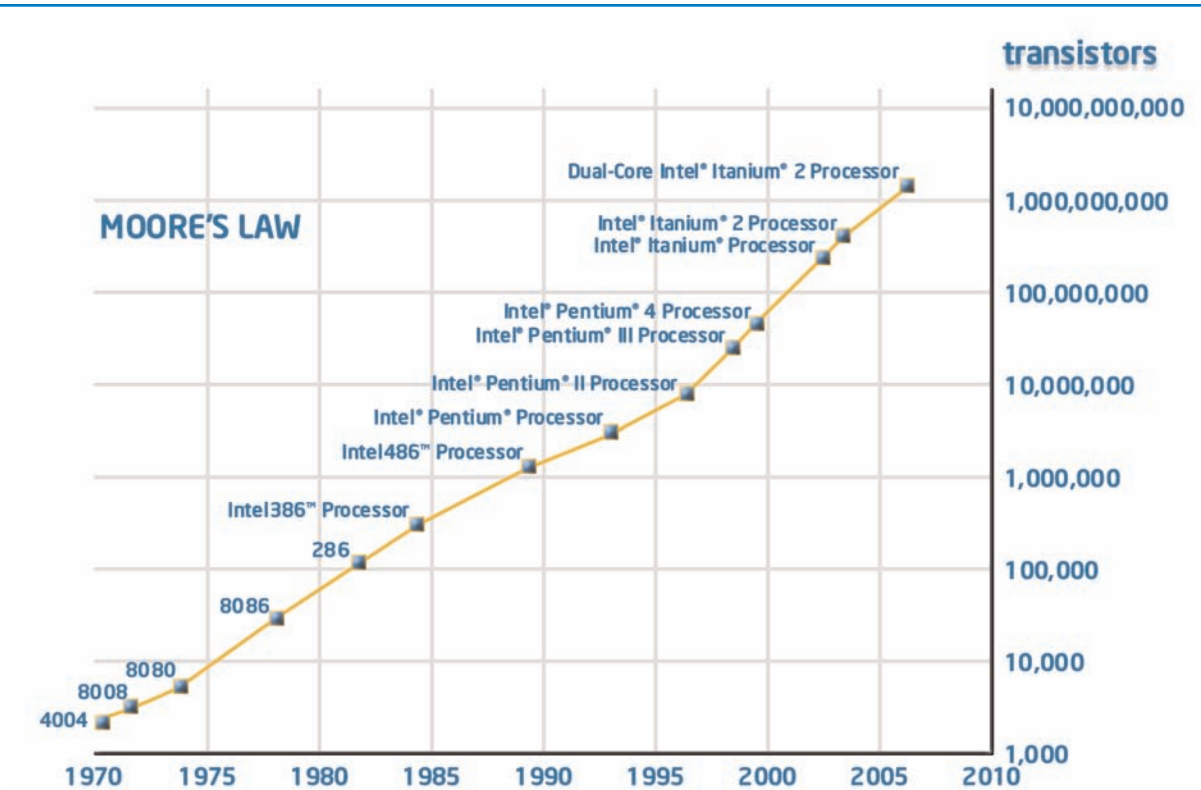

Figure 1: Intel has steadily increased the number of transistors on processors for decades, following the prediction of Moore's Law.

which dramatically extended the battery life of mobile computers. Multi-core processors (multiple execution cores packaged in a single processor) are a key innovation to drive further improvement in support of today's demand for highly complex processors.

Currently, Intel has committed to delivering a new processor architecture approximately every two years alternating with the introduction of a new generation of silicon process technology, and is leading the industry in delivering multi-core processors in high volume across all its platforms. Intel expects at the end of 2006 to be shipping dual- and multi-core processors at a rate of more than 70 percent for desktop and mobile segments and more than 85 percent for servers. In addition, Intel expects by the end of 2007 to be shipping multi-core processors at a rate of more than 90 percent in the desktop and mobile segments and at close to 100 percent for servers. Significant investments in 90-nanometer (nm) and 65nm process technologies and 300mm manufacturing capacity make this fast ramp to multi-core processors possible. Intel® architectures could eventually feature dozens or even hundreds of execution cores on a single processor.

How will multi-core processors help reduce energy consumption? Energy consumption depends on core voltage and operating frequency. With multi-core processors, a slight decrease in individual core voltage can yield a significant reduction in energy consumption without affecting performance. In addition, the extra processing power provided by the dual-core architecture means that more work can be performed for a given amount of energy consumed. This would be analogous to an airplane being able to dramatically improve its speed without increasing its fuel consumption rate—ultimately less energy would be used to reach the destination because the plane would spend less time flying. Intel is using the transition to multi-core platforms to work both on multi-core microarchitectures and on all the other platform components to maximize energy efficiency. This "balanced platform" approach focuses on enhancing all elements in concert so that the integrated features and capabilities all contribute to everything from energy efficiency to the ideal user experience.

Intel Leadership in Developing Power-Efficient Architectures

Intel started early down the road to maximizing performance while minimizing energy consumed on several fronts.

On the process side, Intel initially started with bipolar transistors. We then made transitions to positive-channel metal-oxide semiconductor (PMOS), to negative-channel metal-oxide semiconductor (NMOS), and finally to complementary metal oxide semiconductor (CMOS)—all to better manage energy efficiency.

On the platform side, the aforementioned Intel Centrino mobile technology was Intel's first" from the ground up" example of its platform approach. Intel Centrino mobile technology teamed the Intel® Pentium® M processor—specially designed for energy efficiency—with a compatible Intel® chipset, lightweight mobile form factor, wireless capabilities, and technologies to enable great battery life. The first version of the Intel Pentium M microarchitecture was designed with four innovations to increase performance and reduce energy consumption: advanced branch prediction, micro-op fusion, power-optimized processor system bus, and dedicated stack manager.

The second-generation Pentium M processor utilized Intel's 90nm manufacturing technology and featured faster clock speeds, design enhancements, and more on-die cache memory for better performance. Both these processors include support for Enhanced Intel® SpeedStep® technology, which helps optimize application performance and energy consumption for great battery life. The third-generation dual-core, 65nm Intel Pentium M processor features Intel® Dynamic Power Coordination, a new power management system that synchronizes each core's Enhanced Intel SpeedStep power-saving technologies. This processor, which is part of the next-generation Intel Centrino mobile technology platform, will offer as much as twice the performance and energy efficiency compared to the first-generation Intel Pentium M processor.

Intel's leadership in developing energy-efficient architectures for mobile platforms is now being extended to all segments. Intel® Core™ microarchitecture is a new foundation for Intel architecture–based processors. It is designed to produce multi-core platforms with superior performance while operating at lower power. New desktop, mainstream server and mobile platforms using this architecture began shipping in Q3 2006:

- The new Intel® Core™2 Duo mobile processor provides a greater than 2x processor performance increase and up to a 28 percent power reduction with new Intel Centrino Duo mobile technology laptops as compared to previous-generation Intel® architecture–based laptop processors.[2]
- The new Core 2 Duo processors for desktops are up to 40 percent faster and over 40 percent more energy-efficient as compared to previous-generation Intel desktop processors.[3]
- The new Dual-Core Intel® Xeon® 5100 series processor for servers provides as much as three times the performance and over three times performance-per-watt improvement over earlier single-core Intel Xeon processors.[4]
- The new Dual-Core Intel Xeon processor LV 5148 for blade servers in power-constrained environments has a rated thermal design power (TDP) of 40W (a large improvement over the 110W thermal ceilings of many server chips).[5]

The Platform Approach to Energy Optimization

In line with Intel's platform focus, Intel researchers, scientists, and engineers are working with other industry leaders to find variables in the design, manufacturing, and use of computing and communications devices that influence the energy equation. Their goal is to maximize energy efficiency while simultaneously maintaining or increasing performance. This will be achieved by a combination of improvements in microarchitecture, silicon process technology, software, and platform technologies, as illustrated in Table 1.

65nm Process Technology		Chip			System	
Transistor	**Interconnects**	**Circuit**	**Architecture**	**Packaging**	**Power Delivery and Management**	**Software**
▪ Second-generation strained silicon	▪ Low-k carbon-doped-oxide inter-layer dielectric	▪ Body bias ▪ Dynamic sleep transistor ▪ Demand-based switching ▪ Active Power Reduction ▪ On-die voltage regulation	▪ Multi-core and clustered micro-architectures ▪ Power-optimized micro-architecture - Power Gating - Memory Disambiguation - Macro Fusion	▪ Techniques to reduce package thickness ▪ Heat spreaders and packaging that target "hot spots" ▪ Self-contained liquid cooling	▪ Voltage Regulation Technology ▪ Improved display power specs ▪ Thermal design and engineering, including advanced heat-synch technology ▪ Reference design solutions	▪ Developer tools: - Intel® VTune™ Performance Analyzers - Mobility software guidelines

Table 1: Energy improvements from process technology to system.

Obviously, processor power is an important consideration in the energy equation, but processors are hardly the only component drawing power. Total energy consumption, for example, is also dependent on memory DIMMs, chipsets, fans, hard disk drives, peripherals, power supply efficiency, and other components.

Working with each one of these components can significantly reduce overall energy consumption. For instance, Intel's use of DDR2 memory improves performance up to 11 percent with a 30 percent reduction in memory power consumption. Combining Intel processors with Intel chipsets featuring integrated graphics saves the need for a separate, power-consuming graphics card.

The next-generation Intel Centrino Duo mobile technology[6] platform provides a perfect example of the improvements in energy optimization possible by focusing on the entire platform and combining silicon-based energy savings with energy-efficiency initiatives and mobile-optimized software. On these new platforms, intelligent power capabilities such as Advanced Power Gating allow parts of the processor core to be shut down even during periods of high-performance execution to optimize performance and energy efficiency. Intel® Dynamic Bus Parking enables platform power savings by allowing the chipset to power down with the processor in low-frequency mode states to enable improved battery life. These are examples of improvements across the system, from silicon design to improved platform components. A more complete list of the sources of some of the energy savings can be found in appendix A.

Optimizing Platform Components for Energy Efficiency and Performance

Power-Aware Microarchitecture

Intel's microarchitecture researchers are exploring new architectures that are both "conscious" of power and thermal challenges and able to manage them dynamically while running applications. These architectures include multi-core microprocessors, clustered microarchitectures, and other power-optimized microarchitectures.

Multi-Core, Multithreaded, and Clustered Microarchitectures

Intel is implementing multi-core microarchitectures and examining the concepts of clustered microarchitectures to develop processor cores and clusters that perform optimized load balancing. This is achieved through a combination of software and hardware mechanisms that dynamically examine the utilization, priority, and thermal characteristics of a workload. Optimized load balancing enables each core to run at a different frequency or voltage. Intel is also investigating core-hopping mechanisms where having a stream of calculations jump from one microprocessor to another can be used to spread the power dissipation over a greater area. Some cores could also be dedicated to special purposes to achieve additional energy efficiencies. The goal is to increase overall performance without significant increases in either the baseline frequency of operation or the net energy consumption of the device.

Power-Optimized Microarchitecture

Intel Core microarchitecture will include many new and existing solutions for managing power consumption at the core level. Many of these manage active and idle states. The focus in idle state power management is to keep the vital functionality of a device active while the rest of the device is in "sleep" mode, thereby reducing active power. Intel Core microarchitecture utilizes a number of techniques that vary energy consumption according to demand or utilize low power states as a means of achieving greater energy efficiency. A more complete list of these techniques is included in appendix B.

Intel® Smart Cache Technology

Cache contributes to processor energy consumption. Finding ways to disable it while retaining data integrity and memory coherency can save power. Intel® Smart Cache technology–a smarter and more efficient cache design—will appear first as part of the dual-core Intel Pentium M processor in the next generation of the Intel Centrino mobile technology platform. Intel Smart Cache technology advantages include:

- Both cores fully share L2 cache, minimizing bus traffic by being able to access shared data from the same cache.
- Dynamic cache allocation and centralized control logic enable power optimization and energy savings.
- Dynamic Intel® Smart Cache Flush determines cache requirements (using a hardware-based algorithm) during periods of activity and dynamically adapts cache size based on demand. Cache is gradually flushed to memory, allowing cache to be turned off to save power.

Low-Power Processors for Handhelds and Other Devices

Handhelds and other small-form-factor devices require special consideration. As an example, Intel is working with the industry to design low-power Ultra Mobile PC (UMPC) processor platforms targeted to weigh less than 2 pounds (>1 kilogram) with an initial targeted battery life of 3-5 hours. This new UMPC category offers consumers small, ultra-mobile devices with full PC capabilities, uncompromised Internet access, anytime connectivity, and the ability to recognize and adapt to its environment virtually anytime and anywhere.[7]

Enhanced Intel SpeedStep® Technology and Demand-Based Switching

Two new or enhanced technologies are playing and will continue to play an important role in further improving energy efficiency on Intel® platforms:

- **Enhanced Intel SpeedStep** technology dynamically scales frequency and voltage based on the need for processing power. It significantly reduces the average runtime power used in notebooks and desktops. By reducing power consumption during lower utilization, savings of up to 30 percent in power and cooling can be achieved. In mobile platforms, this technology helps extend battery life.
- **Demand-Based Switching** is a server version of Enhanced Intel SpeedStep technology. This automated power management technology has been shown to reduce platform power consumption by up to approximately 25 percent in typical IT environments. Demand-Based Switching could result in significant savings for large companies with multiple data centers. Improvements in compute density could be achieved by using advanced power prediction and monitoring features that will be available with this technology on Intel server platforms in 2006.

Low-Power Circuit Design

In addition to power-aware microarchitectures, Intel is addressing power challenges at the chip level through innovations in circuit research. As feature sizes decrease, transistors leak, even when they are turned off. Intel is advancing circuit design techniques that help control leakage. Here are some of the low-power circuit design innovations that will be appearing soon in Intel products.

- **Body Biasing.** This involves dynamically adjusting the voltage applied to the body of a transistor (bias) to manipulate the threshold voltage—the voltage at which the transistor turns on. Intel is using a prototype Arithmetic Logical Unit (ALU) to test a number of these techniques. Having localized control of the bias voltage enables the designer to make tradeoffs between the circuit performance and the energy it consumes. This capability can be used to reduce leakage during periods of inactivity or to increase performance during peak use.

- **Dynamic Sleep Transistor.** This solution adds a transistor in series with the power supply. This dynamic sleep transistor can be turned off when a block of logic circuits is in idle mode, thus helping reduce leakage.

Addressing Power at the Transistor Level

Intel is using its world-class expertise in silicon process technology and volume manufacturing to address power by reducing transistor leakage, decreasing interconnect resistance and capacitance, and researching new transistor materials and structures. Many of the most recent breakthroughs will deliver significant energy savings in future Intel products.

New Process Technology

Intel has a long history of introducing leading process technologies on a faster cycle than the industry. A good example is Intel's 65nm process technology, which Intel has ramped into volume production at least a year ahead of the competition. This technology features second-generation strained silicon transistors with a reduced gate length (35nm) that provide the industry's best performance while minimizing a chip's active power. The process uses a low-k dielectric material that increases signal speed inside the chip and reduces chip energy consumption.

Intel now has an ultra-low-power 65nm process technology under development that will enable production of very low-power chipsets for mobile platforms and small-form-factor devices. This process addresses three types of transistor leakage and reduces total leakage by roughly 1,000 times from the standard process while maintaining about 50 percent of the drive current (drive current is directly related to processor frequency). Intel's new ultra-low-power 65nm process will provide additional options in delivering the circuit density, performance, and energy consumption required by users of battery-operated devices. This process uses an improved transistor design to decrease chip energy consumption. This is important because electricity leakage from these microscopic transistors, even when they are in the "off" state, leads to unnecessary energy consumption. Intel's transistor modifications result in significant reductions in the three major sources of transistor leakage: sub-threshold leakage, junction leakage, and gate oxide leakage. The benefits of reduced transistor leakage are lower power and increased battery life. Intel is also well along in developing its next two process generations, 45nm and 32nm.

Transistors and Interconnects

Intel continually researches new power-efficient transistor and interconnect designs and has implemented many of them in current process technologies. Still others are being studied for use in future process technologies.

Examples of recent innovations that are in production today include:

- Intel's proprietary **strained silicon**, now in its second generation. Strained silicon reduces current leakage 5x or more (and thus energy consumption and heat dissipation) without diminishing performance. Alternatively, strained silicon can enable a performance improvement while maintaining constant power.
- Second-generation **carbon-doped-oxide** (CDO). Used in the 65nm process, CDO, when combined with a new etch stop layer, further reduces interconnect capacitance to decrease power.

Other technologies which may be incorporated in future processes include:

- **High-k gate dielectric and metal gate.** Intel has demonstrated that with these materials, leakage can be reduced by over 100x when compared with today's silicon dioxide.
- **Tri-gate transistors.** This novel three-dimensional design improves drive current while reducing sub-threshold leakage.

Intel is also continuing to research longer-range technologies that may have an influence years down the road. For example, Intel is working with researchers from the British company QinetiQ on prototype transistors using indium antimonide (InSb). These transistors show promise for future high-speed, low-power applications and could extend Moore's Law well beyond 2015. Intel is currently researching the integration of these transistors onto the existing silicon platform, consistent with its silicon strategy going forward.

Packaging

Package design has a major impact on device performance and functionality. Today, submicron feature size at the die level is driving package feature size down to the design-rule level of early silicon transistors. At the same time, electronic equipment designers are shrinking their products, increasing complexity, setting higher expectations for performance, and focusing strongly on reducing cost. To meet these demands, Intel researchers are tackling the size challenge through a variety of innovative packaging techniques.

For handheld products, Intel is advancing multi-chip packaging, where two or more chips are put through a thinning process and stacked in a single package. Silicon wafers are thinned by grinding the back of the wafer to remove as much as 90 percent of the silicon. Multiple packages are then stacked to create an integrated solution that delivers more functionality and higher performance in the same or less space.

Intel is also developing innovative heat-sink technologies that provide improved heat-dissipation capabilities for processors as well as other platform components, such as graphics controllers and chipsets. Conventional technologies such as heat spreaders, heat sinks, and heat pipes will continue to support Intel's energy-efficient 65nm process technology, and will be part of the packaging and system cooling solutions for higher performance processors, graphics controllers, and chipsets. Certain markets, such as gaming machines, are driving advanced cooling solutions that may be applicable to other specialty segments in the future.

Platform Components

In addition to improving the energy efficiency of its own products, Intel's innovations and industry leadership have played a large role in driving the IT industry as a whole to greater energy efficiency. Intel has worked through various industry groups and standards organizations to drive initiatives to get more performance with less power from the complete platform, and has been recognized for its leadership by the U.S. Environmental Protection Agency (EPA) and Department of Energy. Some of the more significant impacts include:

High-efficiency power supplies

While under typical operating conditions a microprocessor accounts for a small part of the overall system power, a power supply can consume up to 50 percent of the total system power for a desktop PC. Working with the Natural Resources Defense Council (NRDC), Intel made changes to its power supply design guidelines to encourage the development and adoption of more energy-efficient power supplies, receiving a Special Recognition Award* from the EPA for its efforts. The EPA estimates that the environmental impacts of achieving the recommended targets established in the Intel design guide would result in the following savings in the United Sates alone:

- Annual electricity savings of over 16 billion kilowatt hours
- Reduced carbon emissions of over 10 million tons of CO2 annually
- Cost savings to end users of USD $1.25 billion annually
- A USD $50 reduction in the cost of ownership of a typical desktop PC over 3 years

Intel is currently working on a power supply project that enables feedback on system performance and power needs to the power supply to improve overall efficiency.

Low-power states
Intel worked closely with the EPA to develop the initial Energy Star* standard for computer systems and was recognized for its leadership by being one of 13 companies to receive the EPA's first Energy Star computer award in 1994. In 2000, the EPA recognized Intel with its climate protection award in recognition of its Instantly Available PC Power Management technology, which enabled systems to achieve significantly lower consumption than the original Energy Star standard. The EPA estimates that if all PCs in the United States used this technology, more than USD $300 million in energy costs could be saved each year.

A number of additional techniques used to reduce energy consumption of various platform components are listed in appendix C.

Software

Intel also has a strong focus on leveraging software to drive power savings. For instance, drivers can be designed to be power-conscious and put their devices in a low-power state as often as possible. They can also be tuned to not interfere with a processor's low-power states. Applications can also help by minimizing processor clock cycles and enabling a processor to get back faster to a lower-power wait state after performing a function.

Unfortunately, most software products are not currently power-aware. Intel is working with the industry, particularly independent software vendors (ISVs), to improve software sensitivity to battery power and configuration, as well as to tune for power. This includes developing benchmarks to help spur development of software cooperation with power-conserving devices, as well as making device characteristics and energy savings evaluations part of the operating system vendor (OSV) design discipline.

Intel offers tools to developers to help them make their applications power-aware. For instance, the Intel® VTune™ Performance Analyzer optimizes software code so that it takes less time to execute a given task, thus lowering overall energy consumption. Intel also provides mobility software–enabling collateral that shows developers how to optimize their applications to improve user experiences and extend battery life.

Intel also has developed Intel® Mobile Voltage Positioning (Intel® MVP) and a digital voltmeter to optimize voltage regulation for mobile processors during application use. Intel MVP is a technology that dynamically adjusts processor voltage (VCC) based on processor activity to reduce processor power. It allows higher processor clock speed at a given power consumption or lower consumption at a given clock frequency.

Conclusion

The need for platforms with the right type of compute power and performance will continue to escalate over time. Fifteen years hence, the capabilities that users expect of PCs are certain to accelerate as dramatically as they have in the past 15 years. The phenomenal growth in world data will continue to spur growth in the number of servers and data centers. Already total server numbers have increased by approximately 150x in less than a decade. At the same time, the demand for smaller, more powerful, more versatile mobile devices with longer battery life will continue to grow—especially as the maturation of the wireless infrastructure and available services will further fuel people's desire to carry their computing and communications devices with them wherever they go.

At the same time, worldwide demand for energy will continue to grow as economies expand and living standards rise in developing nations. This increased demand is likely to keep energy prices rising and also raises significant environmental concerns. Clearly, it is important for both environmental and economic reasons that the energy efficiency of computing and information systems needs to improve dramatically as the sheer number of systems and their functionality continue to grow.

All these trends point to the tremendous need to develop power-efficient designs in all market segments. With a long history of leadership on power management solutions and a long-standing reputation as an industry leader on environmental issues, Intel is ideally positioned to lead this charge. By focusing on the entire platform and not just the parts, Intel's holistic approach to energy optimization will lead the industry in finding all the variables in each platform that can maximize energy efficiency, reduce environmental impact, and continue to reap the performance gains predicted by Moore's Law.

Learn more

Visit the following Web sites to discover more:

Energy-efficient performance:
www.intel.com/technology/eep

Intel architecture:
www.intel.com/technology/architecture

Intel silicon technologies:
www.intel.com/technology/silicon

Intel® Software: www.intel.com/software

Intel platforms: www.intel.com/platforms

Intel Technology & Research:
www.intel.com/technology

Energy Star: www.energystar.gov/

Appendix A

Next-Generation Intel® Centrino® Mobile Technology

Sources for energy savings include:

- Improvements in the processor and chipset through silicon-based improvements (65nm process), various circuit techniques (such as a sleep transistor), and microarchitectural improvements
- Initiatives such as the low-power display panel initiative
- Intel® Display Power Savings Technology, which reduces display backlight power by up to 25 percent with minimal visual impact to the end user
- Intel® Dual-Frequency Graphics Technology (Intel® DFGT), which enables power reductions to integrated graphics chipsets
- Intel® Advanced Thermal Manager with Digital Temperature Sensing, which puts digital thermal sensors close to each core's hot spot to enable more precise fan control for energy savings
- Mobile-optimized software designed for mobile life styles and power optimization (more than 250 software applications have been mobile-optimized, including major enterprise applications such as SAP*, PeopleSoft*, SAS*, and UGS-PLM* software)
- PCI Express* Active State Power Management, which uses Link State power management to provide power savings

Appendix B

Power-Optimized Microarchitecture Techniques

Below are some power management technologies and techniques that are being used or will be used in various Intel® processor platforms.

- **Sparse refresh** saves power by using a frame buffer to represent pixels on the display screen and send to the display device only those regions that need to change.
- **Execution Trace Cache** eliminates redundancy at the microarchitecture level by identifying frequent instruction sequences, extensively optimizing them, and storing them for later reuse.
- **Power gating** ensures that devices on the microarchitecture are on only when they need to be on. The result is both a lower thermal design power and a lower average power. Additionally, many buses and arrays are split so that data required in some modes of operation can be put in a low power state when not needed. Sossaman, an upcoming low-power Dual-Core Intel® Xeon® processor, will employ power gating as one of the ways to bring energy consumption down by an estimated factor of three for dense blade and rack configurations.
- **Intel® Dynamic Power Coordination** automatically adjusts the performance and power between the two processing cores on demand.
- **Platform Low-Frequency Mode** comes into play to conserve energy when both cores reach a common low processor performance state.
- **Intel® Enhanced Deeper Sleep** lowers processor voltage below the deeper sleep state found in previous generations of the Intel® Pentium® M processor. When the processor is inactive, the system clears out some of the memory cache to help save additional power.

Appendix C

Reducing the Energy of Platform Components

Below are some power management techniques that are used for reducing the energy consumption of various platform components.

Lowering energy consumption while reducing platform acoustics
Intel's efforts in reducing platform acoustics are also helping to lower energy consumption. Some of these efforts include:

- **BTX form factor.** Intel has collaborated with the desktop computing industry to create an evolutionary step in the desktop computer form factor that enables lower fan speeds, reduced noise, improved thermal environment, and lower cost of power delivery.
- **Enhanced halt state.** This technology significantly reduces the idle-state power of notebooks, desktops, and servers by reducing the clock speed of the processor and then in turn reducing the voltage.
- **Thermally advantaged chassis.** This solution provides more efficient cooling for ATX form factor designs while helping the processor run more reliably and minimize fan noise.

Pconfig and Power Supply Management Interface (PSMI)
These two technologies enable improved ways to manage data center rack density. Using Pconfig, the maximum power load based on the configurations of the systems in the rack can be calculated. Using PSMI, actual energy consumption can be traced in real time using a console manager. Used with power supplies having monitoring capabilities, Pconfig and PSMI can enable IT to track server usage to better control power expended in cooling and provide an additional safety margin.

Enterprise Power and Thermal Manager (EPTM)
This out-of-the-box tool combines the benefits of DBS and Automatic Control of Power Consumption (ACPC) by dynamically allocating power to maximize performance. This tool can be used for managing energy consumption at every level—from the rack to the overall data center. EPTM is especially useful for maximizing the benefits of ACPC by providing an infrastructure for automating this technology, thereby reducing the need for operator involvement. EPTM addresses not only power-management challenges, but also utility and personnel costs (the bulk of data center expenses).

Intel® Power Tools
These tools enable a standardized approach to optimizing rack utilization from the power perspective. An Intel® Power Calculator estimates worst-case system power by using actual system configurations versus nameplate specifications to determine maximum power consumption. This can enable about 50 percent more systems to be installed per rack. An Intel® Power Gauge measures the actual power consumption, allowing further optimization of rack density based on real-time data collection instead of worst-case numbers.

Hypernate
This is a low-power state that could achieve power savings close to the Advanced Configuration and Power Interface (ACPI) "suspend to disk" mode, but with a much lower resume latency (i.e., the system comes back up faster).

New battery technologies

Intel is investing in new battery technologies for the mobile segment that will help increase the amount of energy a given battery cell can store. Intel is investigating fuel cells and other exotic options, and is particularly interested in two existing chemistries—advanced lithium polymer and zinc-alkaline—which have the potential to double battery capacities without significant increases in size or weight.

Power-efficient LCD displays for mobile segments

Intel works with the Mobile PC Extended Battery Life (EBL) Working Group to reduce display panel power consumption and provide power-efficient reference design guides for manufacturers.

Link Power Management

This Intel-driven industry standard allows for increased data transfer rates in the Serial ATA hard drive connection while reducing power consumption.

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1 See the technical bulletin titled "Intel Unveils Tera-Scale Computing Research Program" at the Intel Web site: www.intel.com/pressroom/kits/events/idfspr_2006/IDFSp06-tera-scale-tech-bulletin.pdf

2 www.intel.com/products/centrino/duo

3 www.intel.com/products/processor/core2duo

4 download.intel.com/products/processor/xeon/dc51kprodbrief.pdf

5 www.intel.com/design/intarch/dualcorexeon/5100

6 www.intel.com/products/centrino/duo/description.htm

7 www.intel.com/go/umpc

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