



Intel® Desktop Board D848PMB Specification Update

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Order Number: C59429-005

The Intel® Desktop Board D848PMB may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® desktop board D848PMB may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

| Date of Revision | Version | Description |
|-------------------------|----------------|---|
| December 2003 | -001 | This document is the first Specification Update for the Intel® Desktop Board D848PMB. |
| January 2004 | -002 | Added Specification Change 1. |
| July 2004 | -003 | Added Documentation Change 1. |
| November 2004 | -004 | Added Erratum 1. |
| December 2004 | -005 | Added Documentation Change 2. |

PREFACE

This document is an update to the specifications contained in the *Intel® Desktop Board D848PMB Technical Product Specification* (Order number C53953). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order number 249199) for specification updates concerning the Intel Pentium 4 processor and that may apply to the desktop board D848PMB. Unless otherwise noted in this document, it should be assumed that any processor errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 848P Chipset Specification Update* (Order Number 253642) for specification updates concerning the 82848P GMCH Controller and that may apply to the desktop board D848PMB. Unless otherwise noted in this document, it should be assumed that any MCH errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 82801EB I/O Controller Hub 5 (ICH5) Specification Update* (Order Number 252517) for specification updates concerning the 82801ER I/O Controller Hub and that may apply to the desktop board D848PMB. Unless otherwise noted in this document, it should be assumed that any ICH 5 errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D848PMB's behavior to deviate from published specifications. Hardware and software designed to be used with any given Altered Assembly (AA) and BIOS revision level must assume that all errata documented for that AA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Update for the
Intel® Desktop Board D848PMB**

GENERAL INFORMATION

Basic Desktop Board D848PMB Identification Information

| AA Revision | BIOS Revision | Notes |
|-------------|-----------------------|-------|
| C54332-201 | RC86510A.86A.0024.P09 | 1-5 |
| C54332-202 | RC86510A.86A.0024.P09 | 1-5 |
| C54332-203 | RC86510A.86A.0026.P10 | 1-5 |
| C54332-204 | RC86510A.86A.0036.P14 | 1-5 |
| C54330-201 | RC86510A.86A.0024.P09 | 1-5 |
| C54330-202 | RC86510A.86A.0024.P09 | 1-5 |
| C54330-203 | RC86510A.86A.0026.P10 | 1-5 |
| C54330-204 | RC86510A.86A.0036.P14 | 1-5 |
| C53157-201 | RC86510A.86A.0024.P09 | 1-5 |
| C53157-202 | RC86510A.86A.0024.P09 | 1-5 |
| C53157-203 | RC86510A.86A.0026.P10 | 1-5 |
| C53157-204 | RC86510A.86A.0036.P14 | 1-5 |
| C52649-201 | RC86510A.86A.0024.P09 | 1-5 |
| C52649-202 | RC86510A.86A.0024.P09 | 1-5 |
| C52649-203 | RC86510A.86A.0026.P10 | 1-5 |
| C52649-204 | RC86510A.86A.0036.P14 | 1-5 |

NOTES:

1. The AA number is found on a small label on the component side of the board.
2. The 82848P Chipset kit used on this AA revision consists of two components as follows:

| Device | Stepping | S-Spec Numbers |
|--------------|----------|----------------|
| 82848P MCH | A0 | SL77Y |
| 82801EB ICH5 | A3 | SL73Z |

3. Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order Number 249199) for errata related to the Pentium 4 processor and that may apply to the desktop board D848PMB.
4. Refer to the *Intel® 848P Chipset Specification Update* (Order Number 253642) for errata related to the 82848P GMCH that may apply to the desktop board D848PMB.
5. Refer to the *Intel® 82801EB I/O Controller Hub 5 (ICH5) Specification Update* (Order Number 252517) for errata related to the 82801ER I/O Controller Hub that may apply to the desktop board D848PMB.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the desktop board D848PMB. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

| | |
|-----------|---|
| Doc: | Document change or update that will be implemented. |
| Plan Fix: | This erratum may be fixed in a future revision of the desktop board, driver, or BIOS. |
| Fixed: | This erratum has been previously fixed. |
| No Fix: | There are no plans to fix this erratum. |
| Shaded: | This erratum is either new or modified from the previous version of the document. |

| NO. | PLANS | SPECIFICATION CHANGES |
|-----|----------|--|
| 1 | Doc | Change to description of Section 2.11.1, DC Loading |
| NO. | PLANS | ERRATA |
| 1 | Plan Fix | System may intermittently hang at POST code 75 with SATA hard disk drives attached |
| NO. | PLANS | DOCUMENTATION CHANGES |
| 1 | Doc | Correction of MCH component name |
| 2 | Doc | Change to Section 2.8.2.2, Table 19, Front Panel Audio Connector |

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Intel® Desktop Board D865GBF/D865GLC Technical Product Specification* (Order Number C53953). All Specification Changes will be incorporated into a future version of that specification.

1. *Change to Description of Section 2.11.1, DC Loading*

Table 37, Section 2.11.1, DC Loading, will change in its entirety as follows:

2.11.1 DC LOADING

Table 37 lists the DC loading characteristics of the board.

Table 37. DC Loading Characteristics

| Mode | DC Power | DC Current at: | | | | |
|-----------------|----------|----------------|---------|---------|--------|--------|
| | | +3.3 V | +5 V | +12 V | -12 V | +5 VSB |
| Minimum loading | 190.00 W | 5.00 A | 11.00 A | 9.00 A | 0.03 A | 0.60 A |
| Maximum loading | 310.00 W | 11.00 A | 15.00 A | 15.00 A | 0.10 A | 1.38 A |



ERRATA

1. ***System May Intermittently Hang at POST Code 75 with SATA Hard Disk Drives Attached***

PROBLEM: An intermittent hang at POST code 75 may be observed when SATA Hard Disk Drives are used. This intermittent hang is due to an erroneous circuit race condition in the system clock when spread spectrum is enabled by BIOS.

IMPLICATION: The system hang is exhibited when the system clock's internal circuitry is erroneously enabled when spread spectrum is enabled on PLL1.

WORKAROUND: The user will need to reset the system, which allows the SATA Hard Disk Drives to be reinitialized.

STATUS: This issue may be fixed in a future BIOS revision.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *Intel® Desktop Board D848PMB Technical Product Specification* (Order Number C53953). All Documentation Changes will be incorporated into a future version of that specification.

1. Correction of MCH Component Name

Section 1.7 will change as follows:

1.7 Intel® 848P Chipset

The Intel® 848P chipset consists of the following devices:

- Intel 82848P Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801EB I/O Controller Hub (ICH5) with AHA bus
- Firmware Hub (FWH)

The MCH is a centralized controller for the system bus, the memory bus, and the Accelerated Hub Architecture interface. The ICH5 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS.

| For information about | Refer to |
|-------------------------------|---|
| The Intel 848P chipset | http://developer.intel.com/ |
| Resources used by the chipset | Chapter 2 |

2. Change to Section 2.8.2.2, Table 19, Front Panel Audio Connector

Table 19 in Section 2.8.2.2 will be replaced in its entirety as follows:

Table 19. Front Panel Audio Connector

| Pin | Signal Name | Pin | Signal Name |
|-----|---------------|-----|----------------------|
| 1 | Mono Mic in | 2 | Ground |
| 3 | Mono Mic Bias | 4 | +5 V |
| 5 | RIGHT_OUT | 6 | Right channel return |
| 7 | No connect | 8 | Key |
| 9 | LEFT_OUT | 10 | Left channel return |