



21555 Bridge Reference Design

Schematics

December 2000

Order Number: 278364-001





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DE1B55501 Schematic Directory

SHEET	DESCRIPTION
sht 1	Schematic Directory
sht 2	Block diagram
sht 3	21555 (DrawBridge - 66MHz)
sht 4	21555 Parallel & Serial ROM, latches and MDM
sht 5	Secondary clock generation & hot swap test
sht 6	Pull up resistors for 21555 signals
sht 7	Primary Edge Connector and svio generation
sht 8	System Slot - PICMG or PCI Option
sht 9	PCI Secondary Option slots Middle and Bottom
sht 10	3.3V Voltage regulator and bulk decoupling
sht 11	Mictor Connectors

REVISION		
CHK	CHANGE NO.	REV

EB555 21555 EVALUATION BOARD

Intel

USRA,
FIRST USED ON OPTION/MODEL:

DRN.	DATE	ENG. GWRD	DATE
CHK'D.	DATE	BOARD LOCATION:	

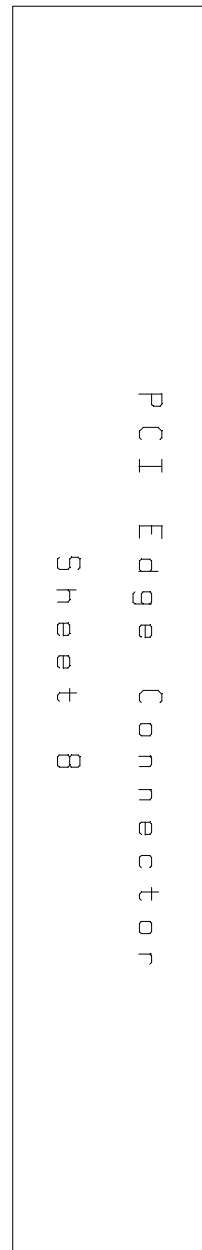
DRN.	DATE	ENG. GWRD	DATE
CHK'D.	DATE	BOARD LOCATION:	

TITLE:		DE1B55501	
SIZE	CODE	NUMBER	REV.

SIZE	CODE	NUMBER	REV.
B			

EB555 Block Diagram

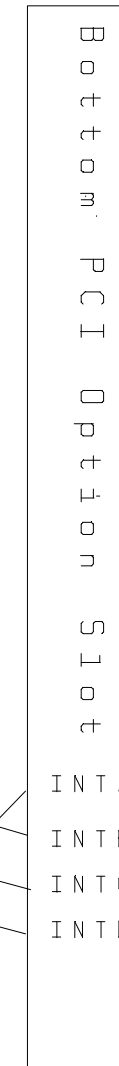
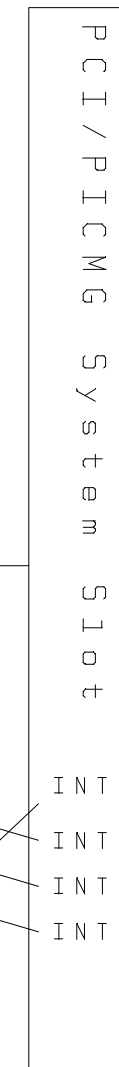
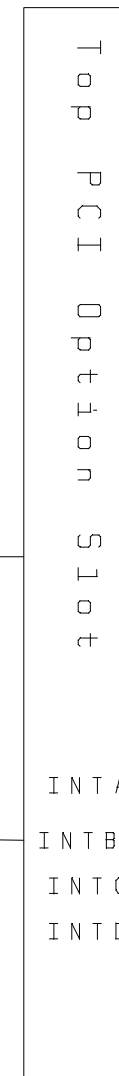
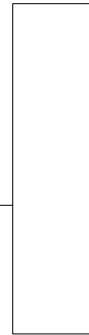
Clock Buffer



Primary Bus



Secondary bus

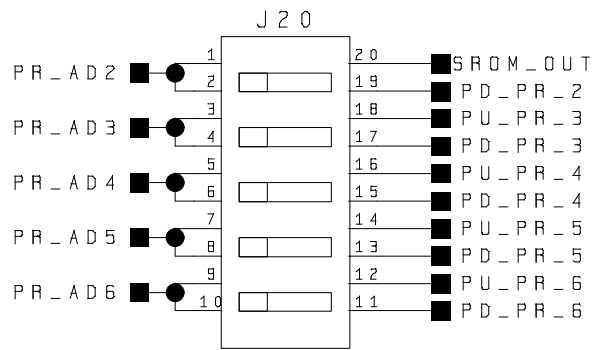


(Not installed)

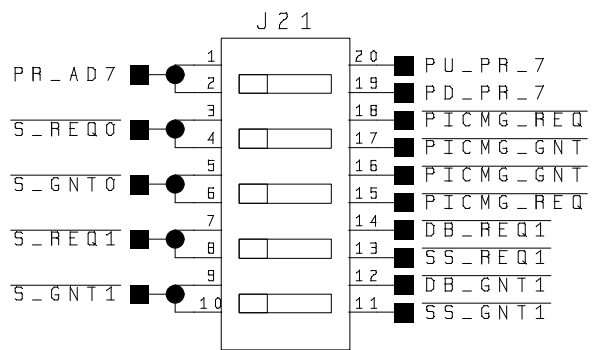
REVISION		
CHK	CHANGE NO.	REV

Intel	DRN.	DATE	ENG.	DATE	TITLE:
	CHK'D.	DATE	BOARD LOCATION:	DF	DE1B55501
USRA:	TOP DOCUMENT NUMBER:			SIZE	CODE
FIRST USED ON OPTION/MODEL:				B	NUMBER
					REV. 2

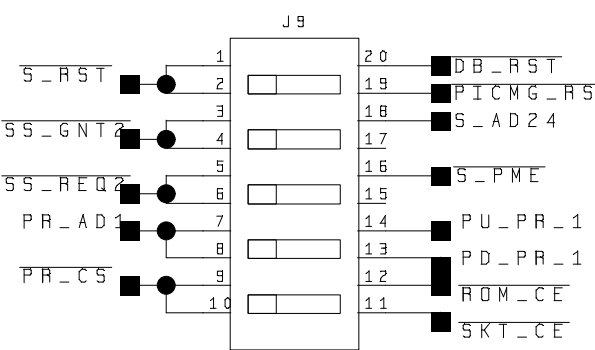
Initialization Selections



J20	DOWN = Pull DOWN	UP = Pull UP
SW1 = pr_2	NO SROM	SROM
SW2 = pr_3	DEBUG - No Lockout	NORMAL - Lockout
SW3 = pr_4	Synch	Async
SW4 = pr_5	DB S_CLK_O DISABLED	DB S_CLK_O ENABLED
SW5 = pr_6	21554 as Central Function	System Slot as Central Function

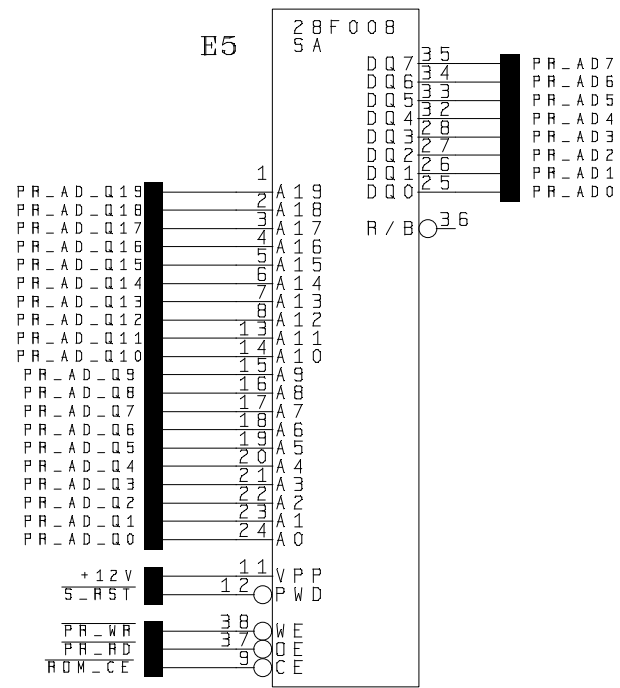


J21	SYSTEM SLOT AS ARBITER	DRAWBRIDGE AS ARBITER
SW1=pr_ad7	DOWN	UP
SW2=DB(s_req0)	DOWN	UP
SW3=DB(s_gnt0)	DOWN	UP
SW4=s_req1	DOWN	UP
SW5=s_gnt1	DOWN	UP

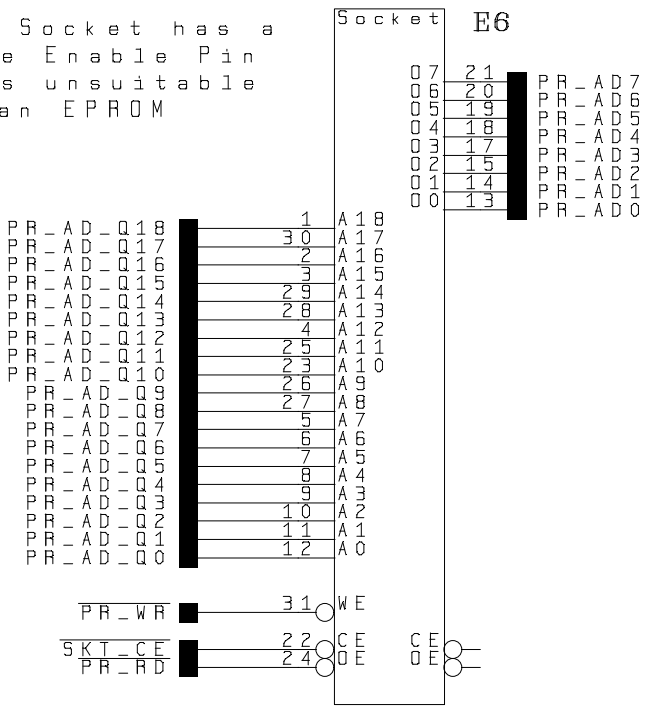


J9	DOWN = Pull DOWN	UP = Pull UP
SW1 = s_rst	PICMG_RST	DB_RST
SW2 = IDSEL	PICMG (top slot)	PCI (top slot)
SW3 = pr_4	PICMG (top slot)	PCI (top slot)
SW4 = pr_5	Enable Prim 64-bit	Disable Prim 64-bit
SW5 = pr_6	ROM Socket	Flash ROM

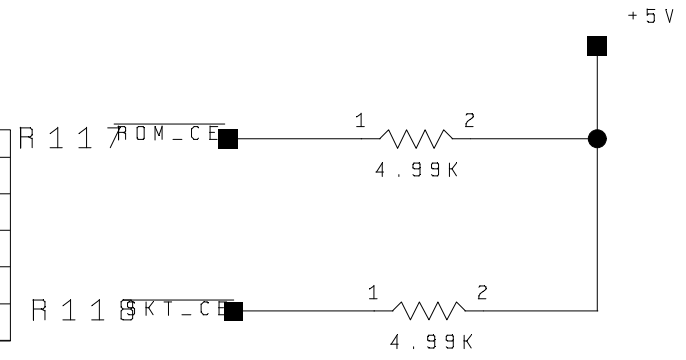
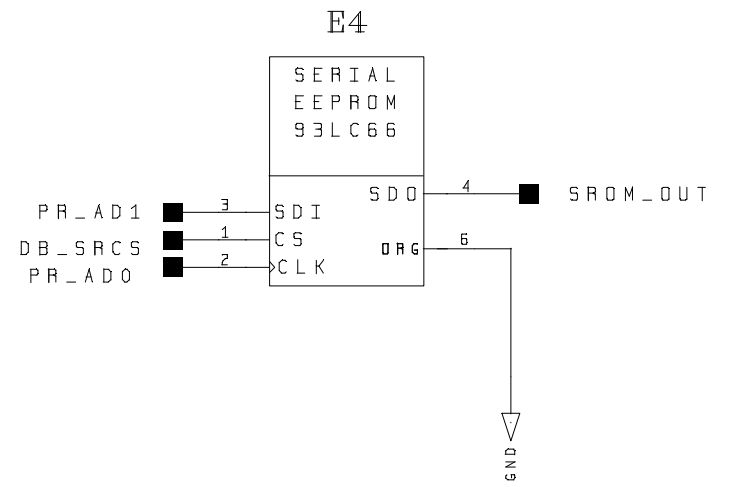
Parallel ROM



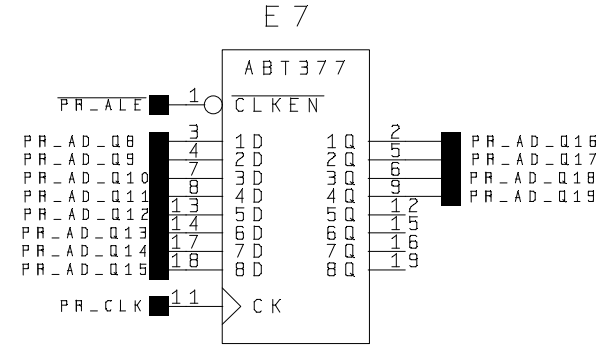
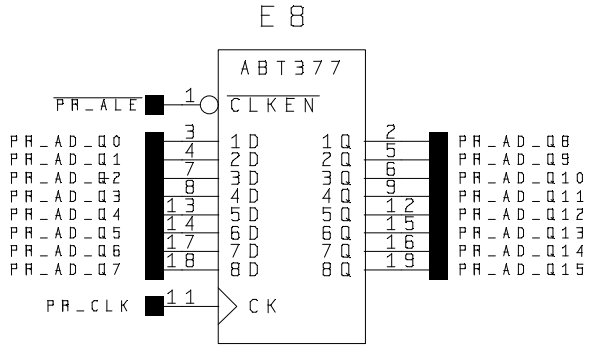
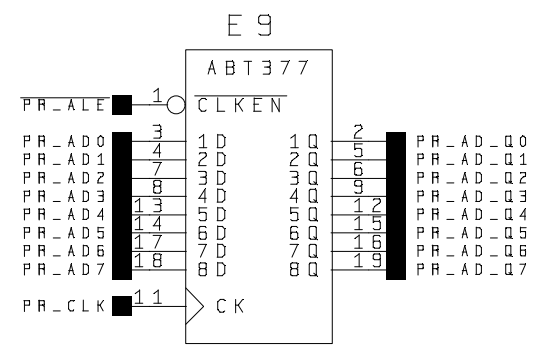
This Socket has a Write Enable Pin So is unsuitable for an EPROM



Serial ROM



Parallel ROM Address Latches



REVISION	DATE	ENG.	DATE	TITLE
CHK CHANGE NO. REV				DE1B55501

Intel

USRA: FIRST USED ON OPTION/MODEL

DRN. DATE ENG. DATE

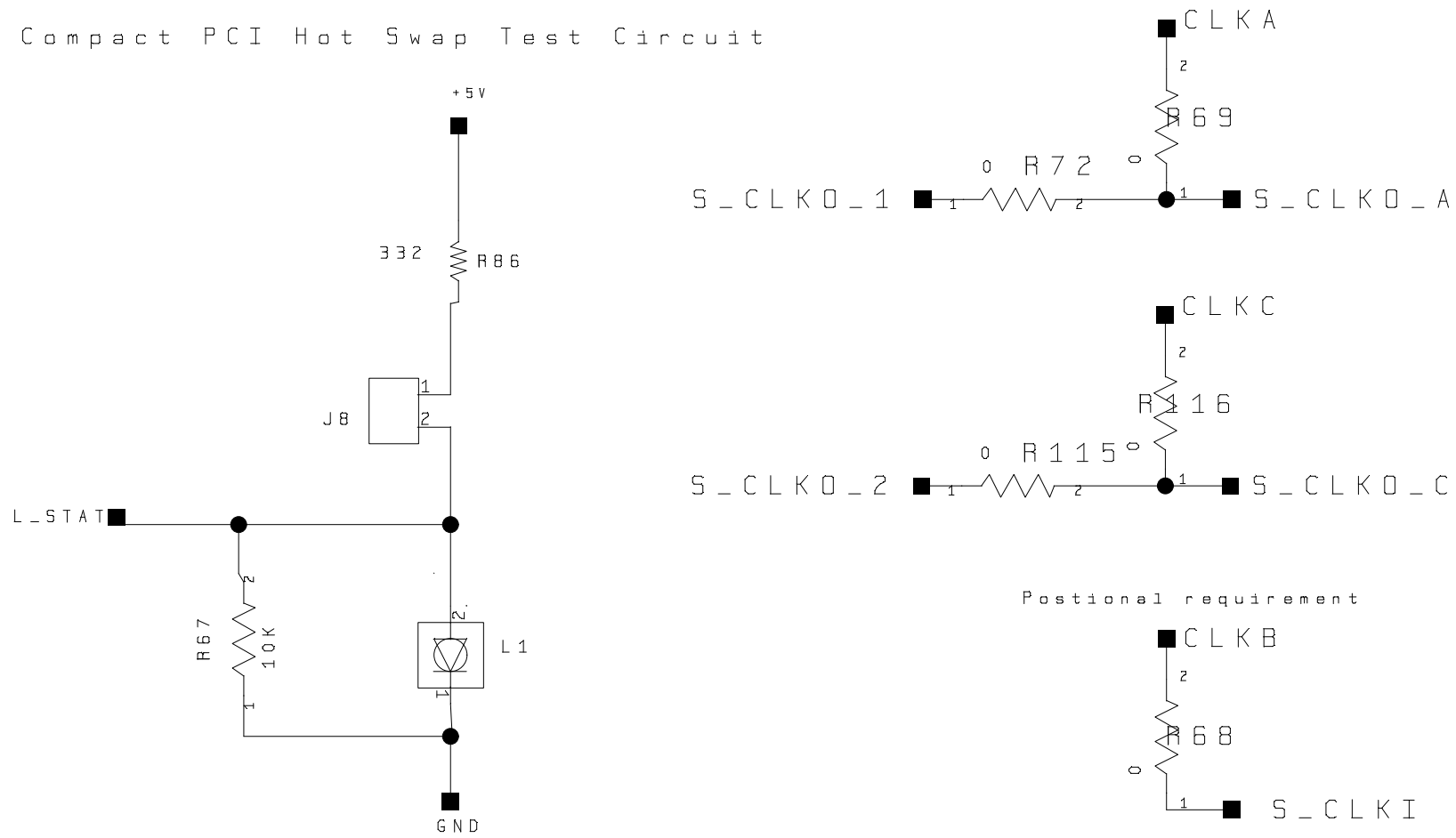
CHK'D. DATE

BOARD LOCATION: SHEET DF

TOP DOCUMENT NUMBER:

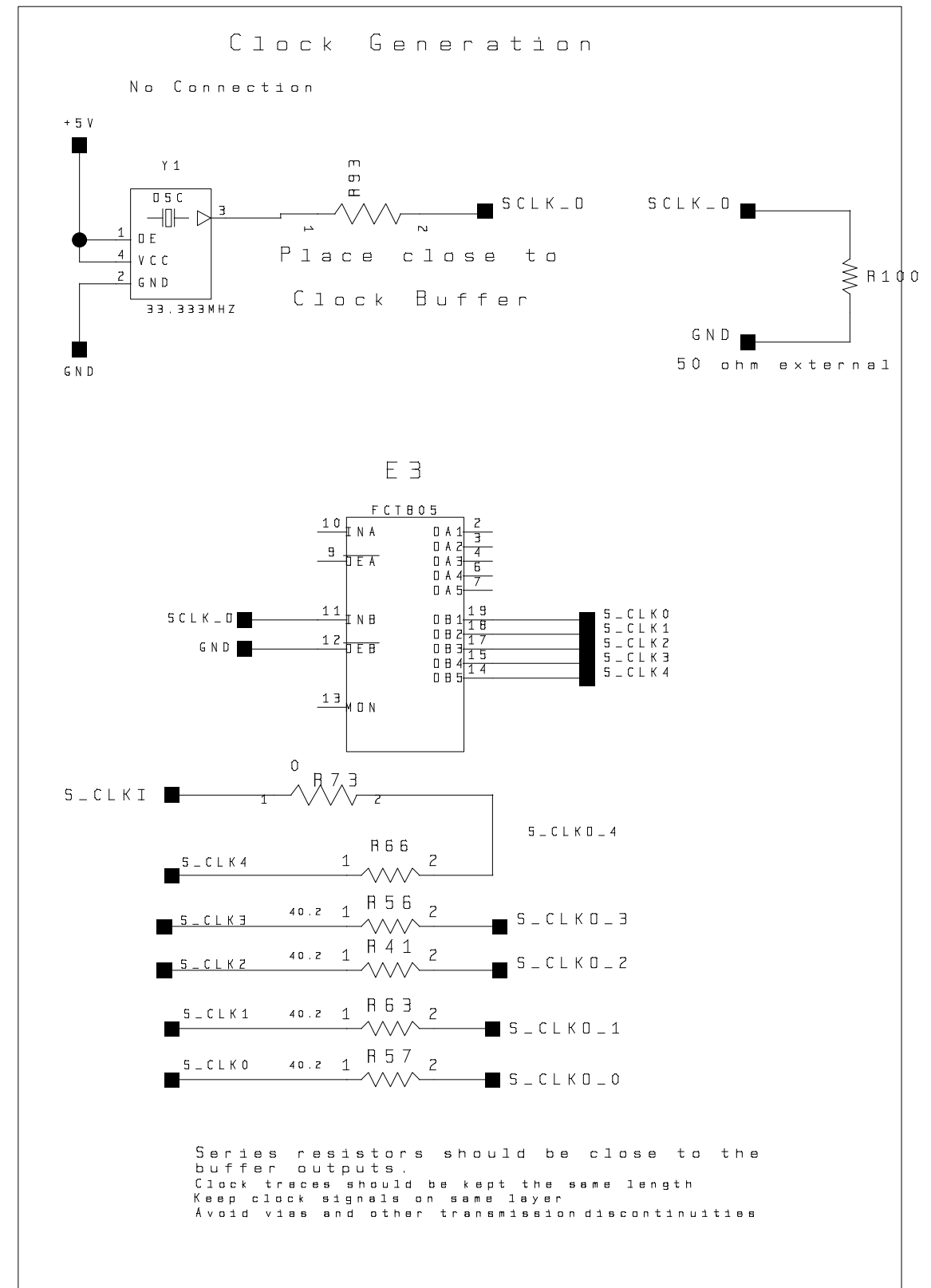
SIZE B CODE NUMBER REV 4

Compact PCI Hot Swap Test Circuit

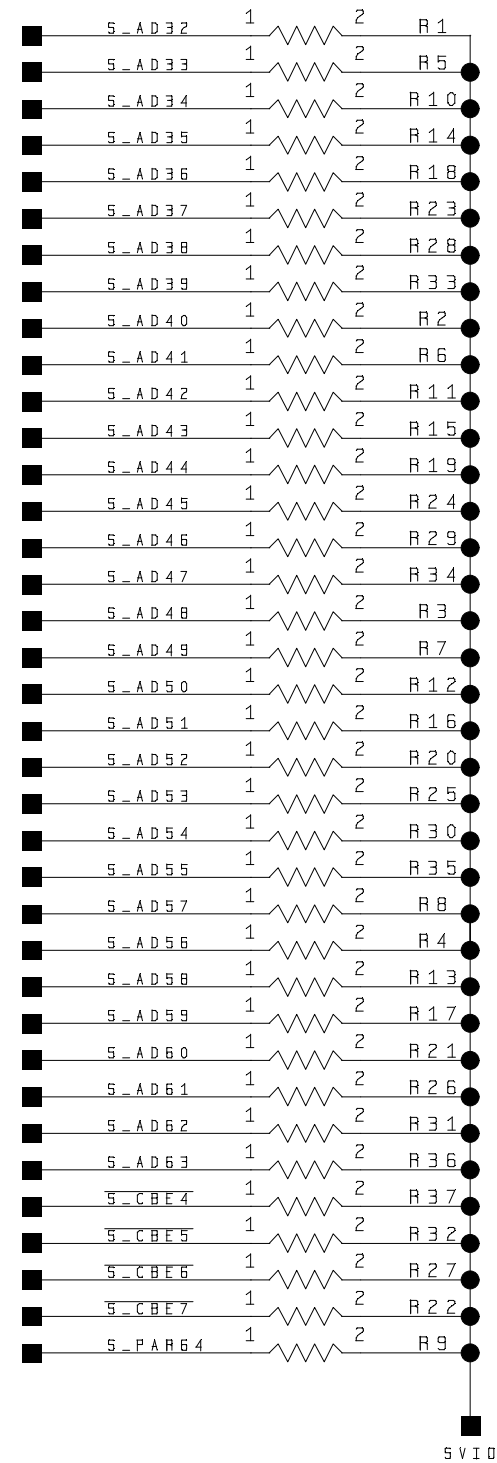


Central Function			
21554		System Slot	
In	Out	In	Out
R65	R68	R68	R65
R72	R69	R69	R72
R91	R92	R92	R73
R115	R116	R116	R91
			R115

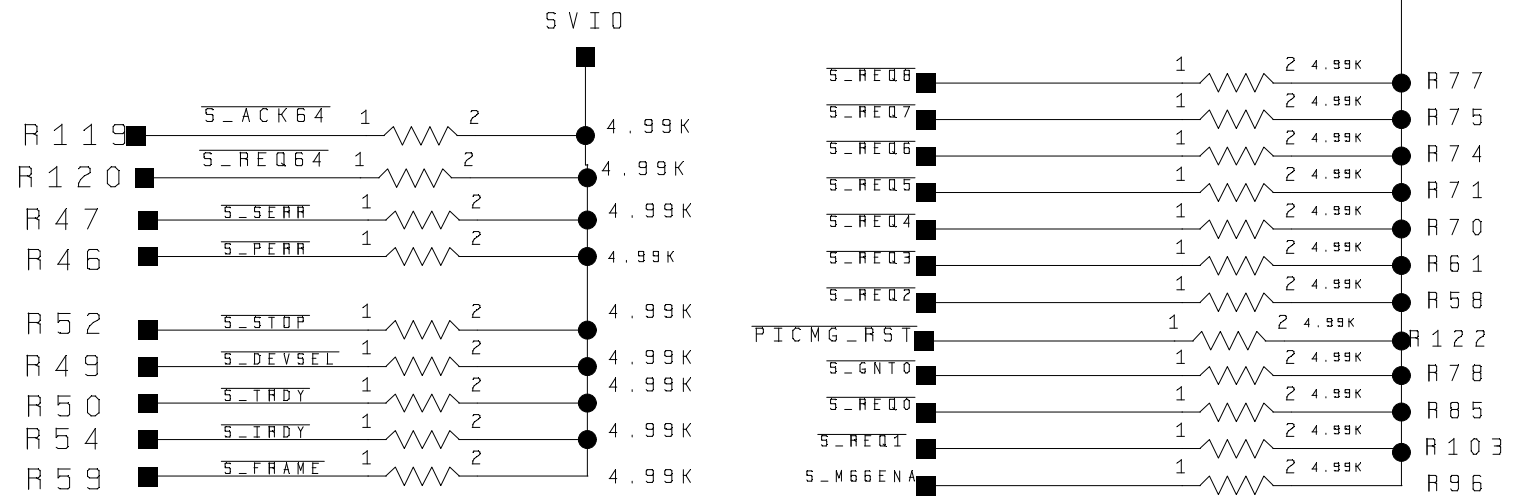
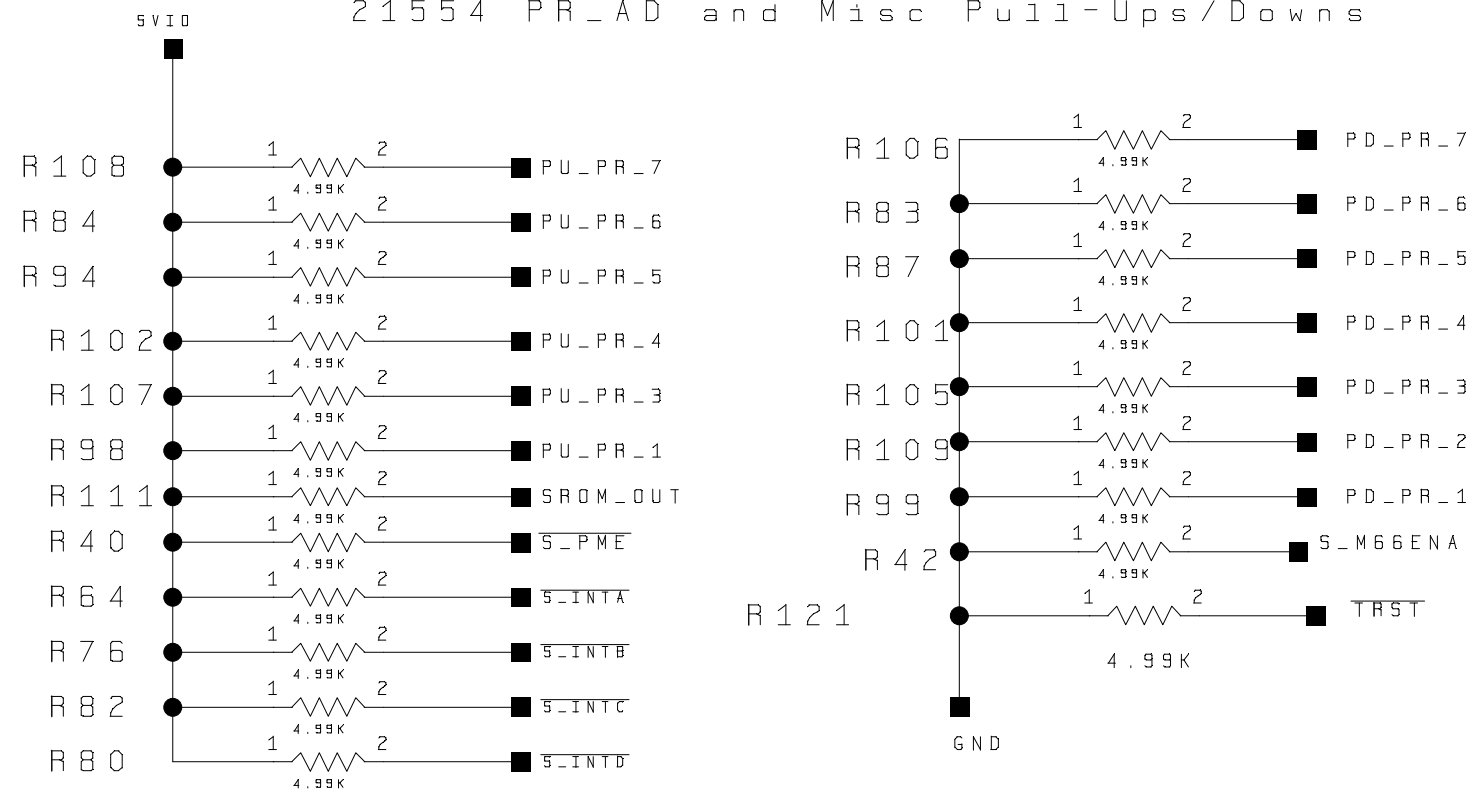
External Oscillator	
In	Out
R93	R65



64-Bit Pull-Ups
R = 4.99K ohms

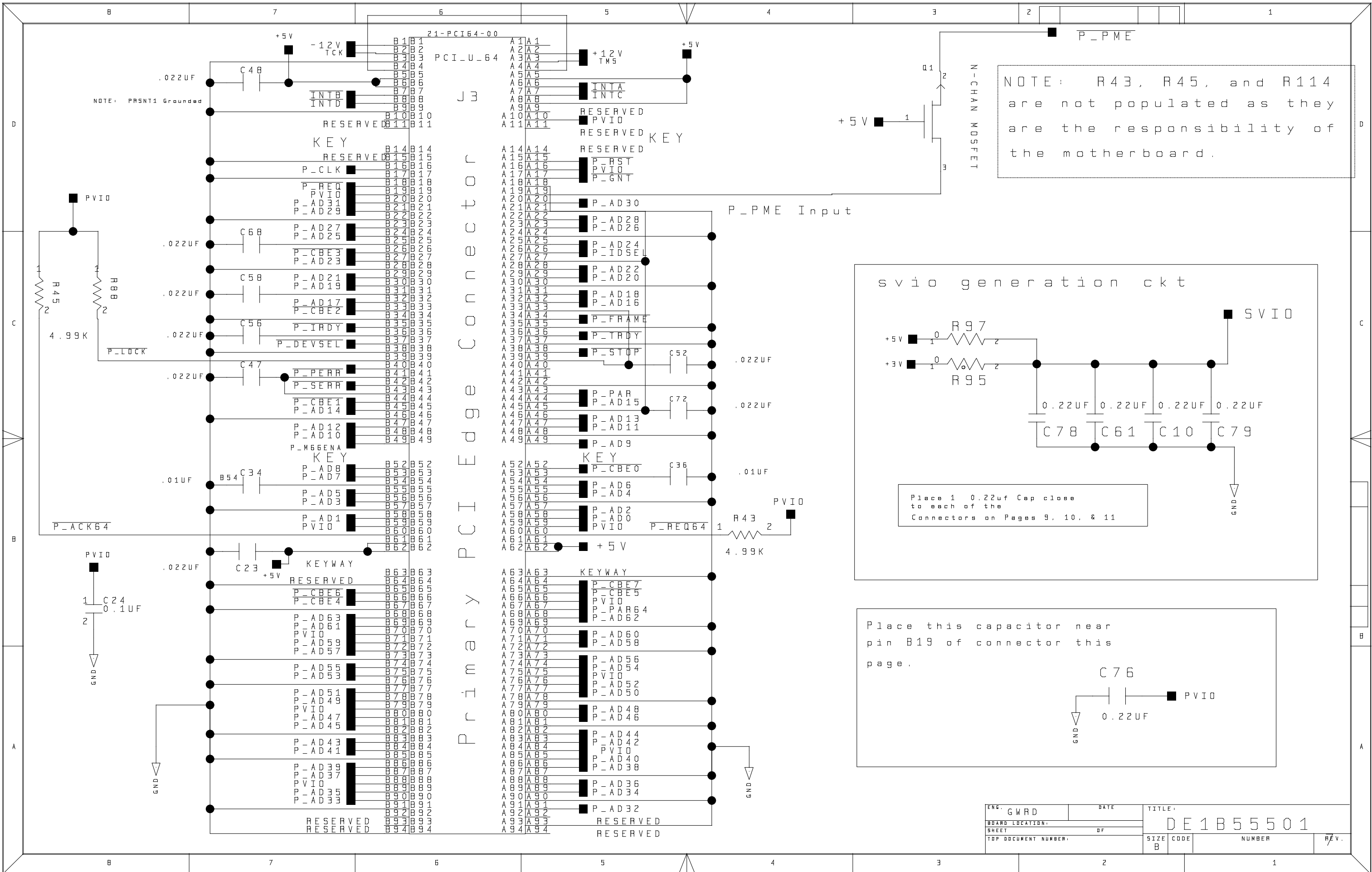


21554 PR_AD and Misc Pull-Ups/Downs

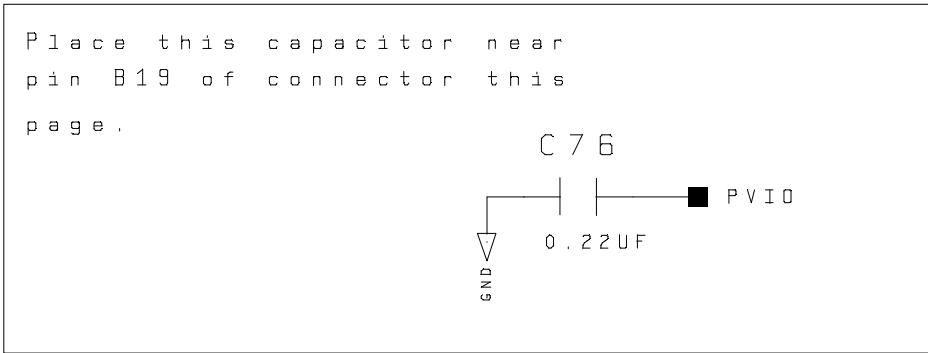
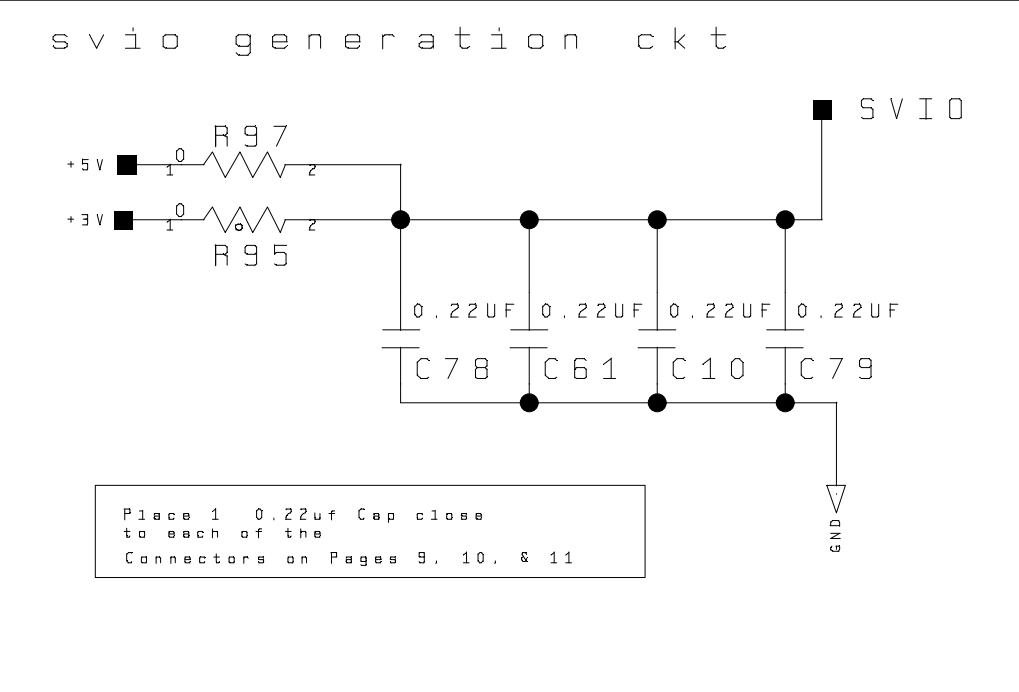


REVISION	
CHK	CHANGE NO. REV

Intel	DRN.	DATE	ENG.	DATE	TITLE		
	CHK'D.	DATE	BOARD LOCATION, SHEET	DF	DE1B55501		
USRA, FIRST USED ON OPTION/MODEL.	TOP DOCUMENT NUMBER.			SIZE	CODE	NUMBER	REV.
				B			



NOTE: R43, R45, and R114 are not populated as they are the responsibility of the motherboard.

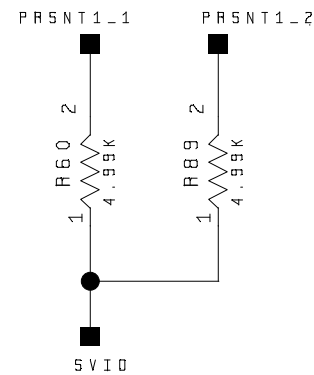


ENG. GWRD	DATE	TITLE:
BOARD LOCATION:		DE1B55501
SHEET	DF	NUMBER
TOP DOCUMENT NUMBER:	SIZE B	CODE
		REV.

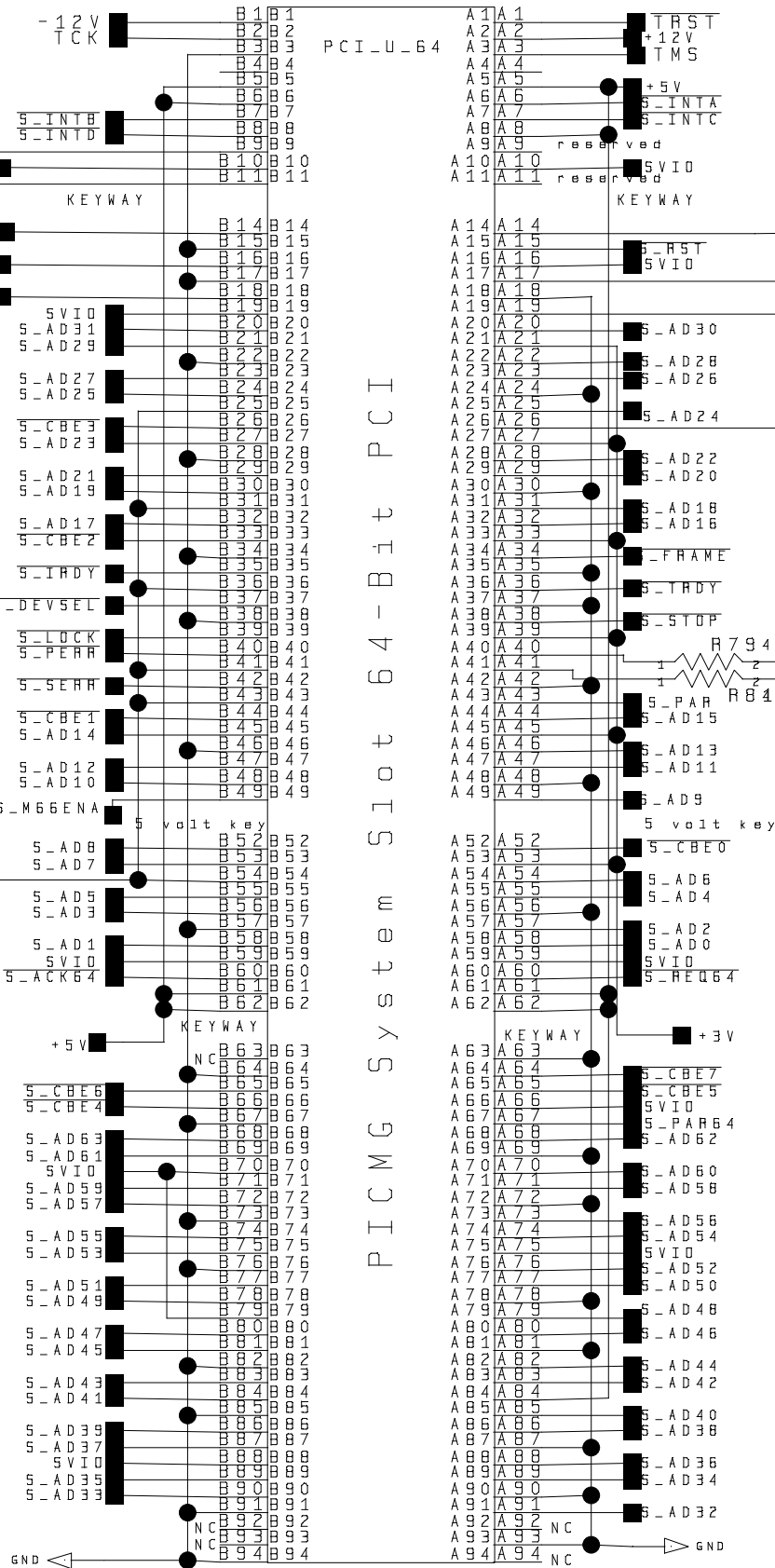
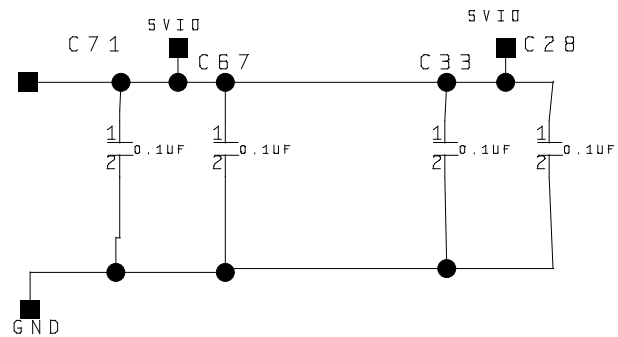
SYSTEM SLOT: 64-BIT PCI

J101
12-39839-19

PCI		PICMG	
B09	PRSENT1-1	F09	KEYWAY
B10	RESERVED	F10	SS_REQ1
B11	PRSENT1-2	F11	KEYWAY
B14	RESERVED	F14	CLKA
B16	CLK	F16	CLKB
B18	REQ#	F18	PICMG_REQ

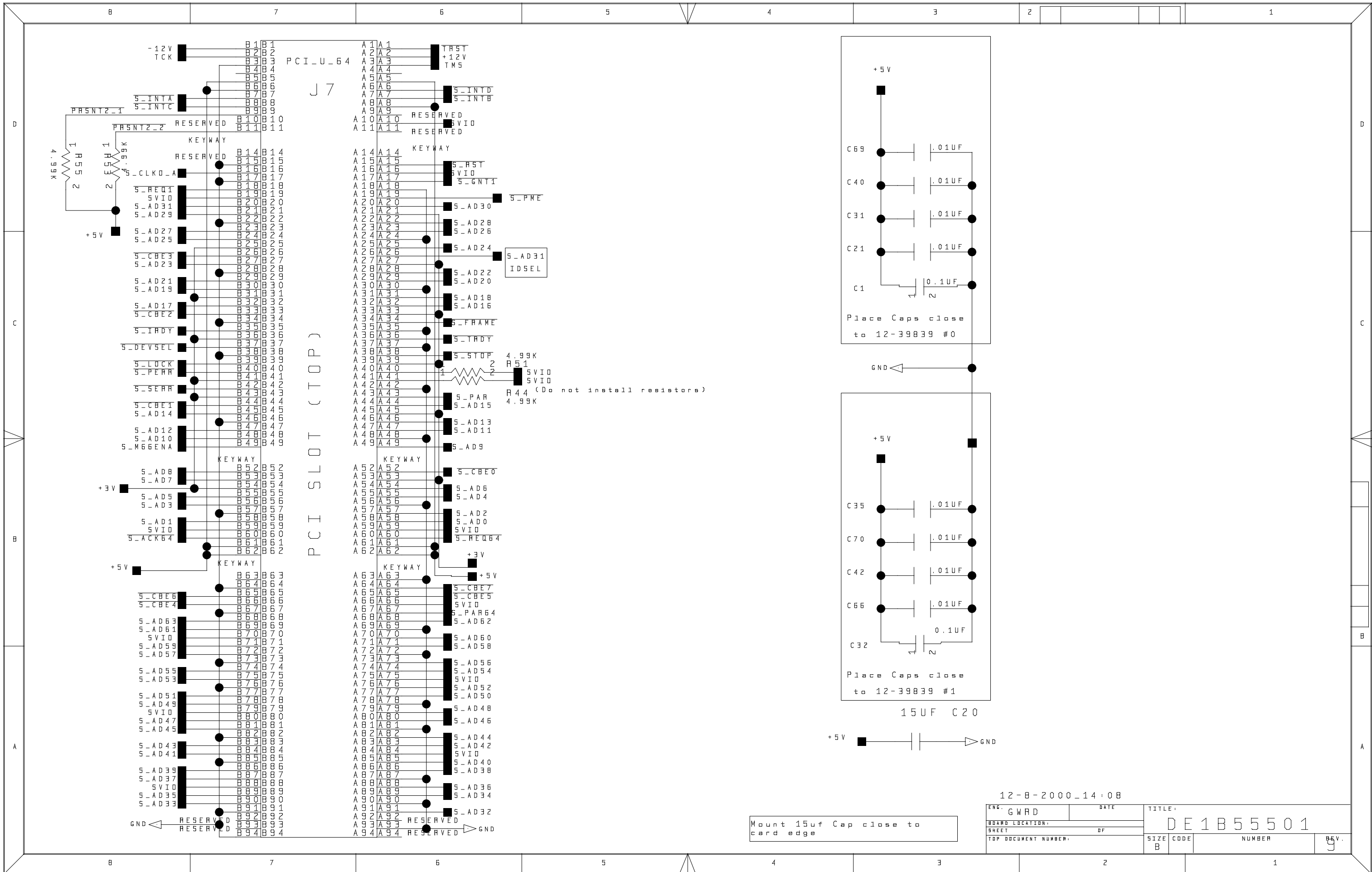


Put two 0.1uF and two 0.22uF close to each of the two connectors



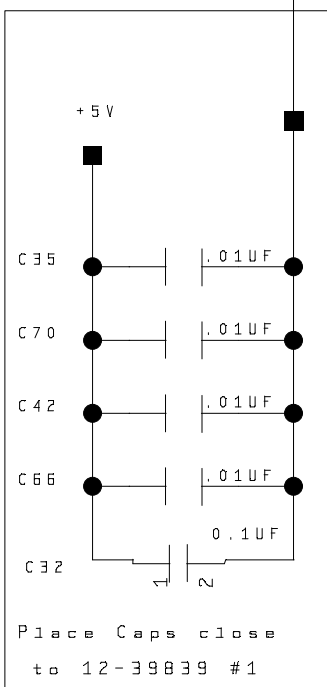
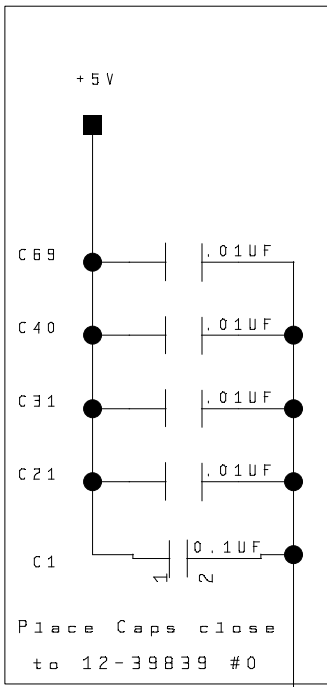
PICMG		PCI	
E09	A09	RESERVED	
E11	A11	RESERVED	
E14	A14	RESERVED	
E17	A17	GNT#	
E19	A19	S_PME	
E26	A26	IDSEL	

PICMG System Slot 64-Bit PCI



J 7

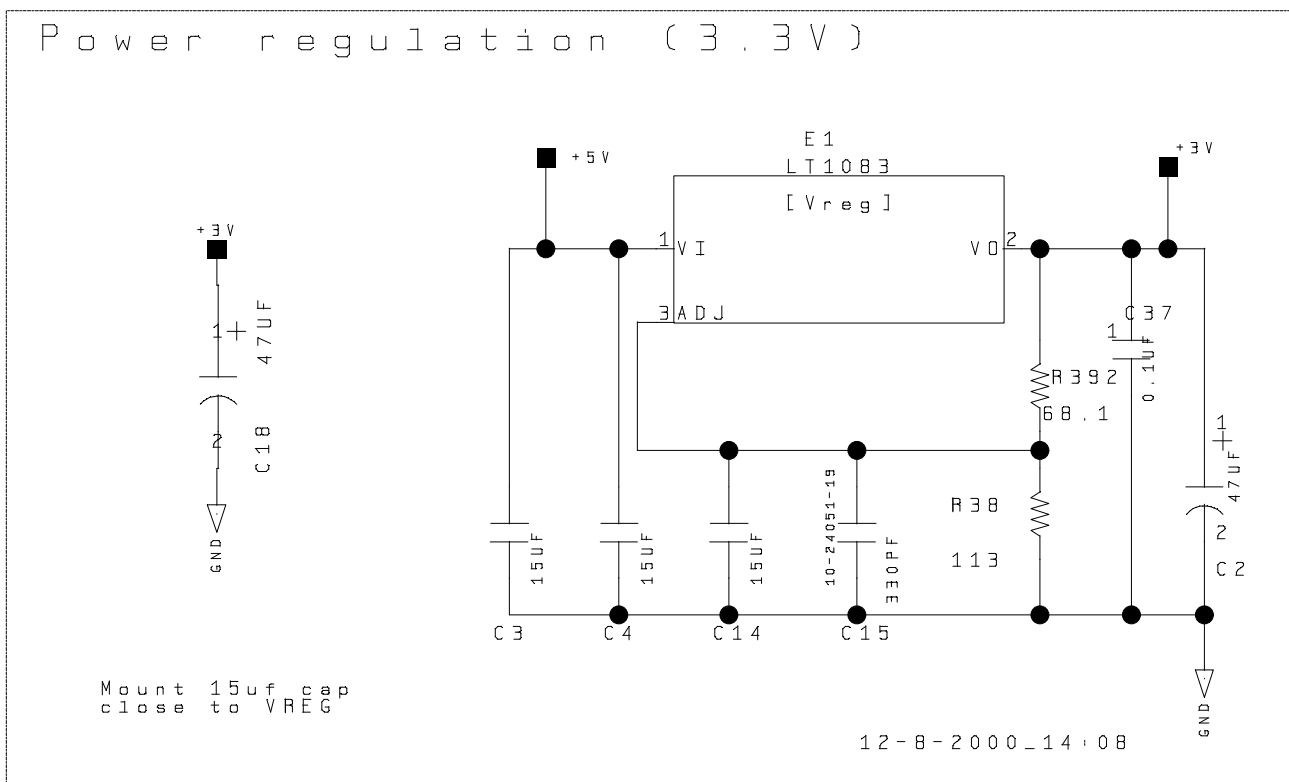
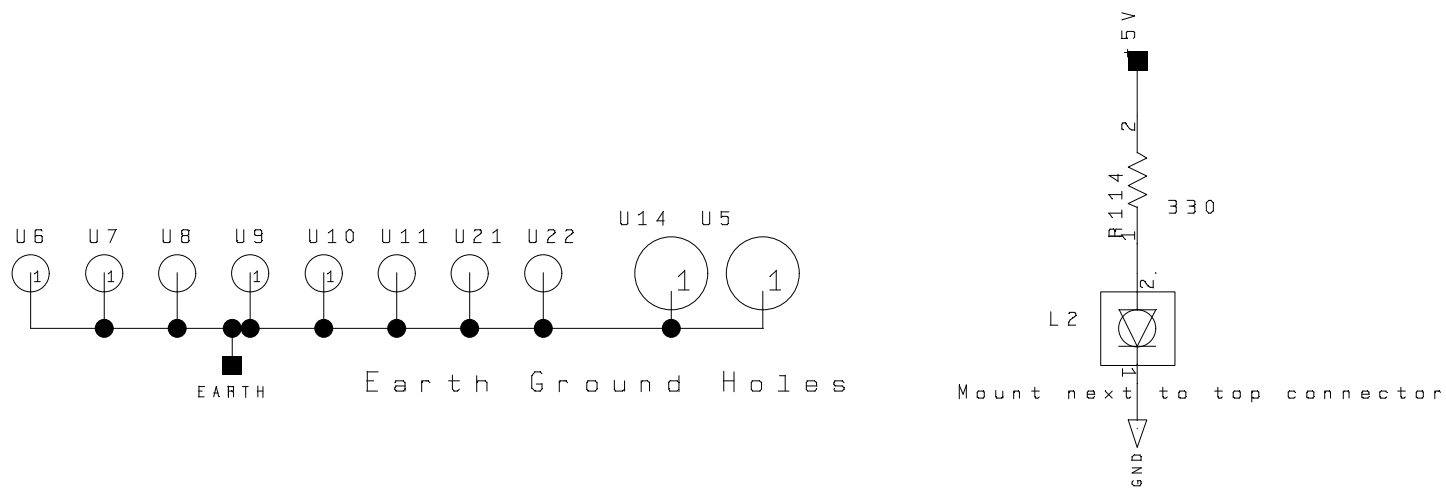
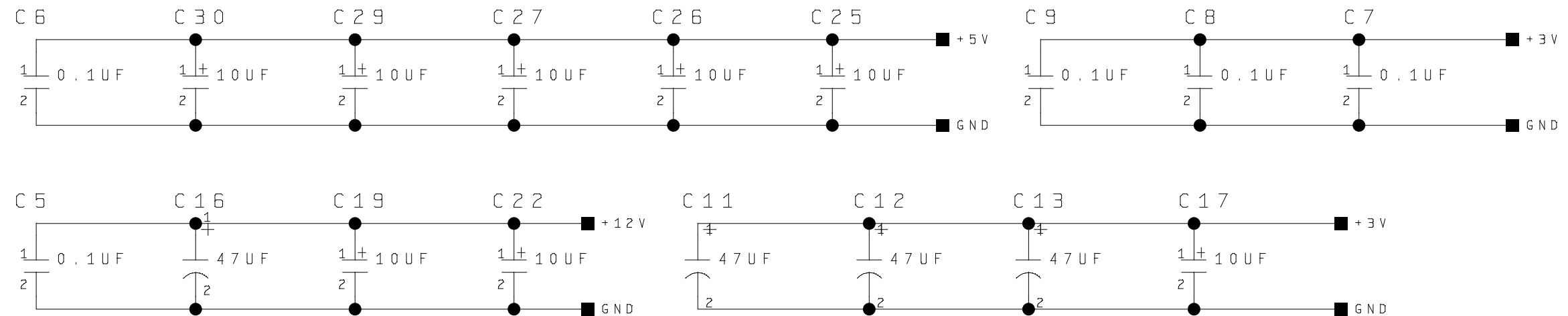
PCI SLOT (TOP)



Mount 15uf Cap close to card edge

12-8-2000_14:08		DATE		TITLE:	
ENG. GWRD		DE 1B55501		REV. 9	
BOARD LOCATION:		SIZE B	CODE	NUMBER	
SHEET	DF				
TOP DOCUMENT NUMBER:					

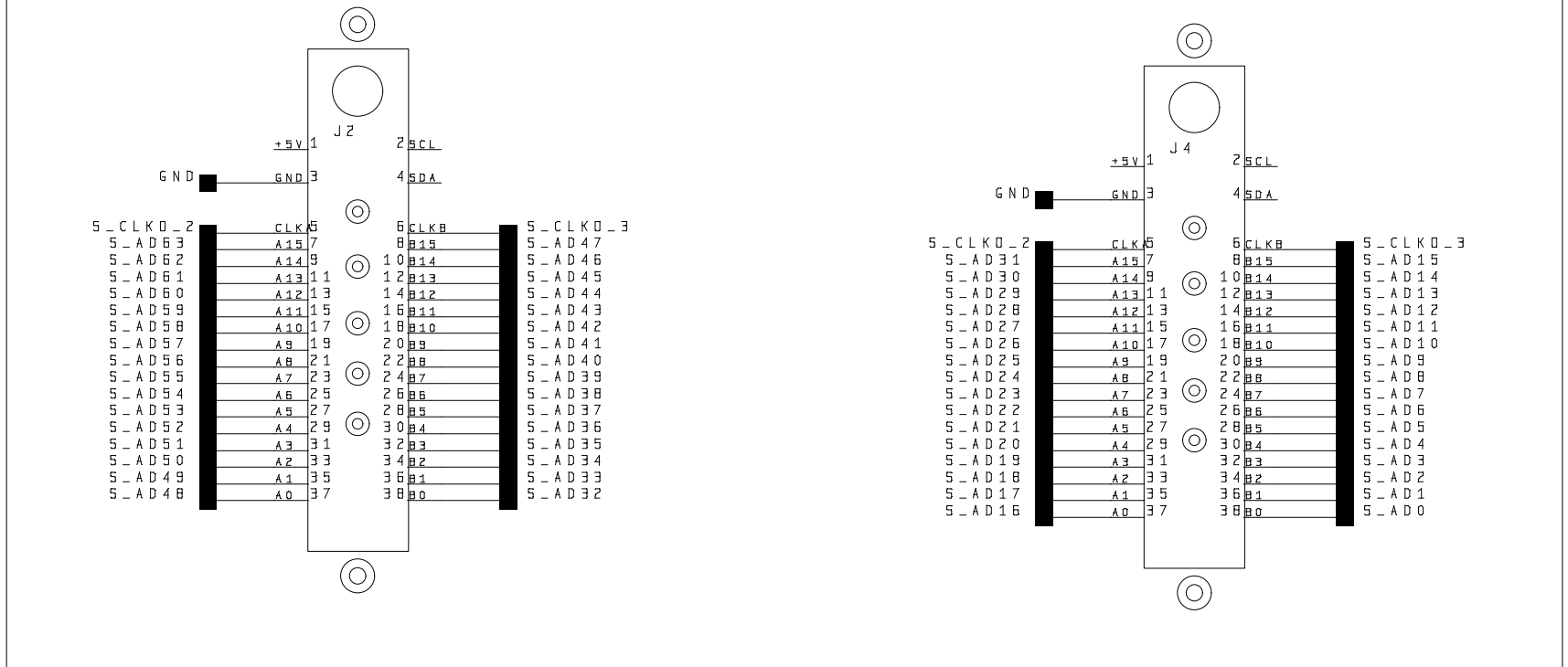
Decoupling; bulk, for all power planes



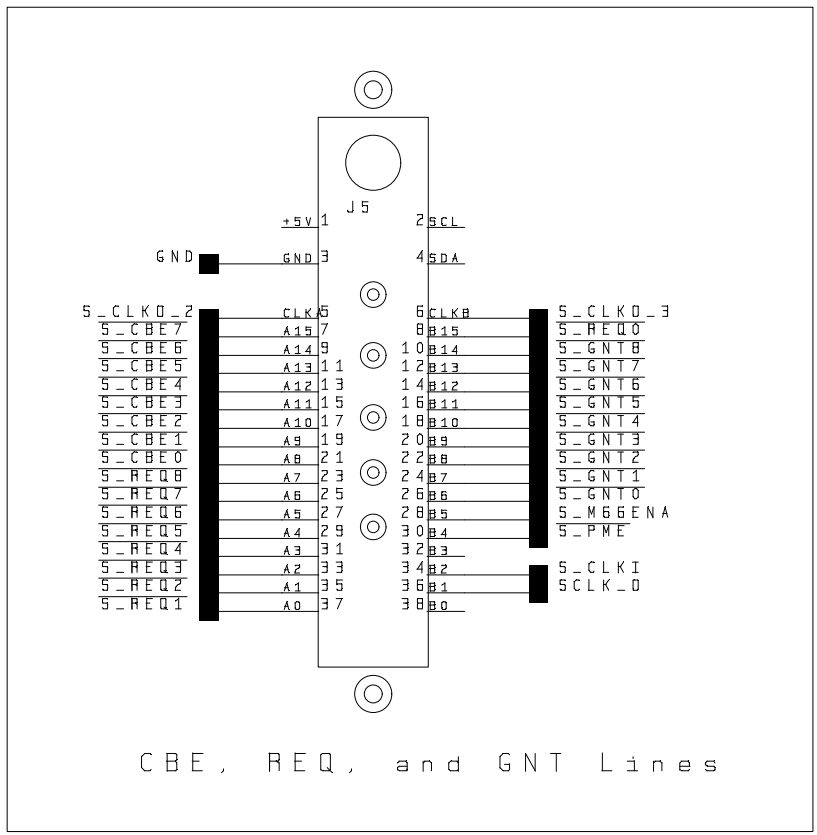
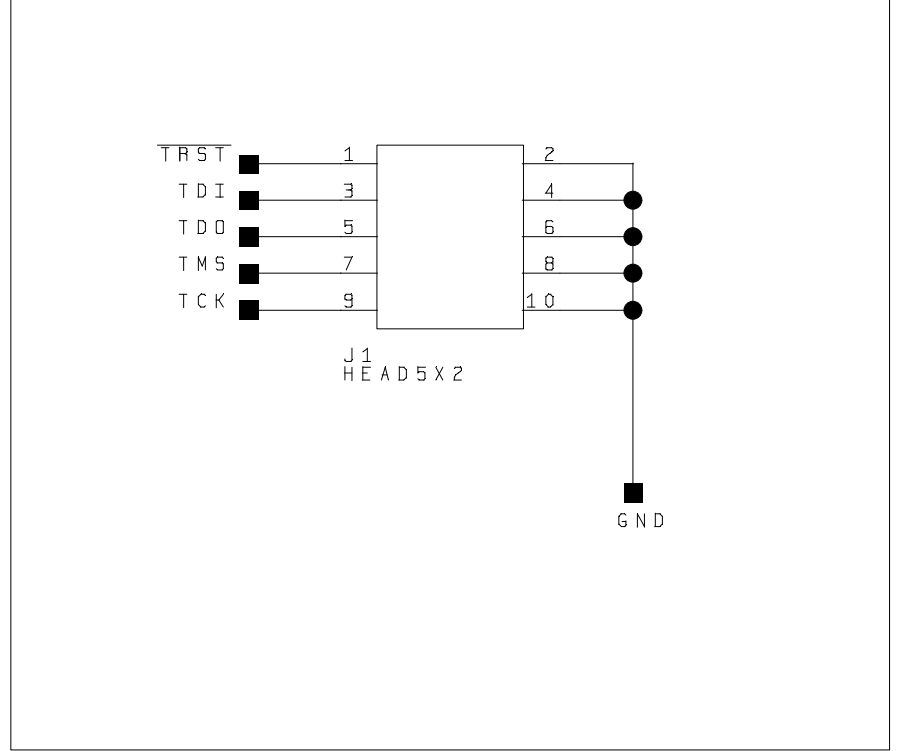
12-8-2000_14_08

ENG. GWRD	DATE	TITLE
BOARD LOCATION	DF	DE1B55501
SHEET	SIZE B	CODE
TOP DOCUMENT NUMBER	NUMBER	1/0

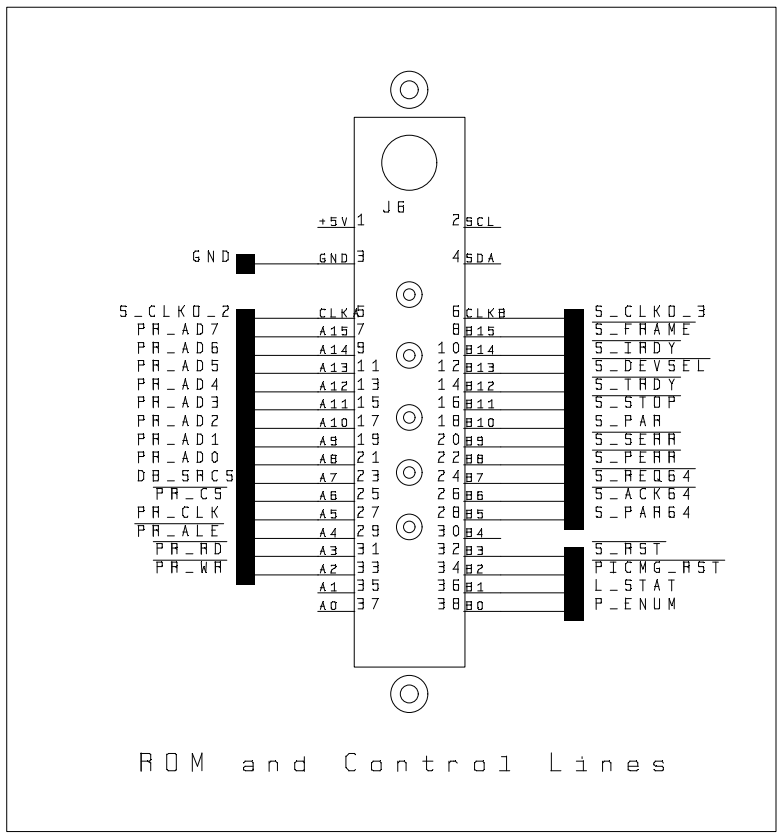
Secondary AD Signals



JTAG Connections



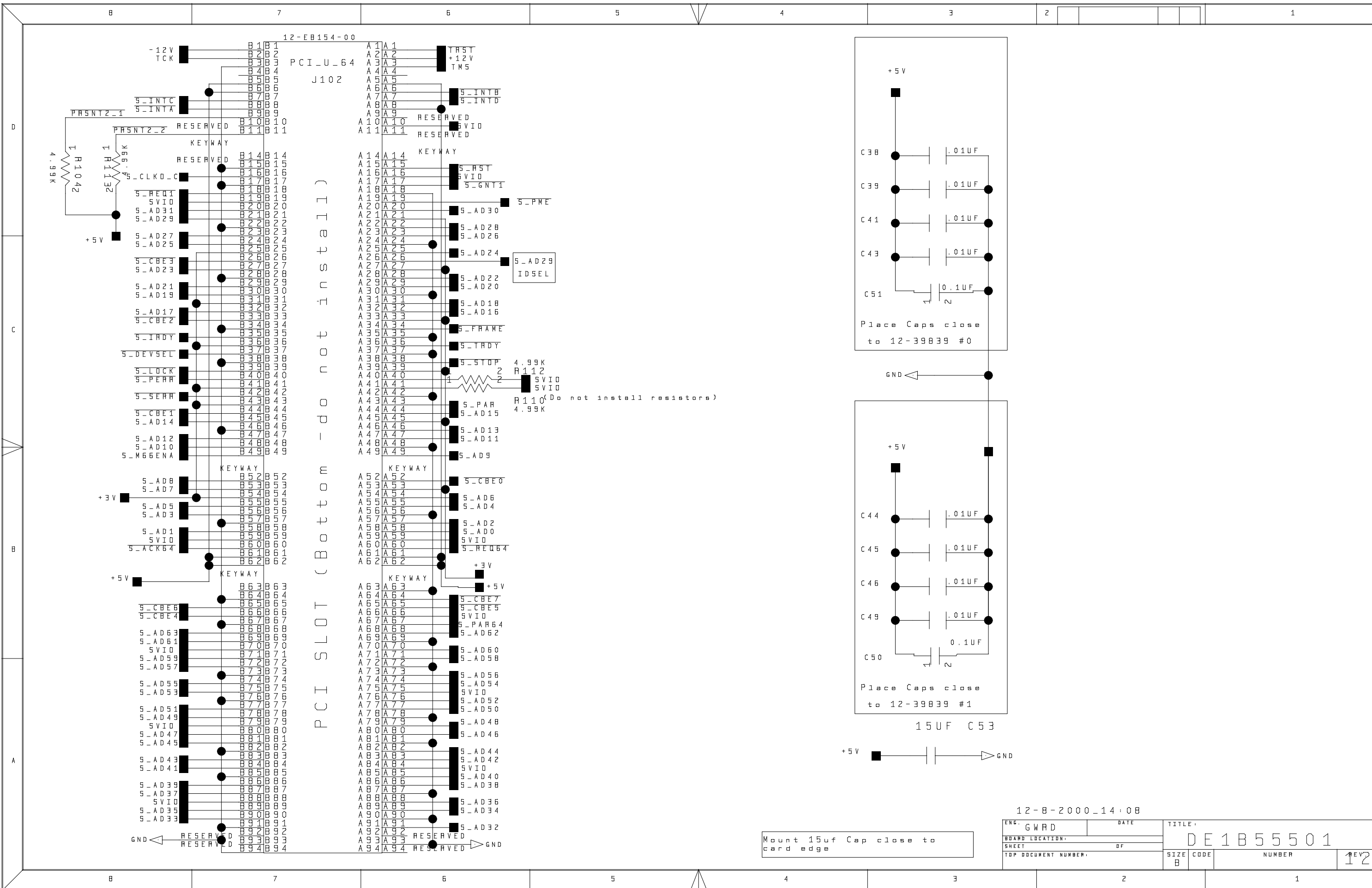
CBE, REQ, and GNT Lines



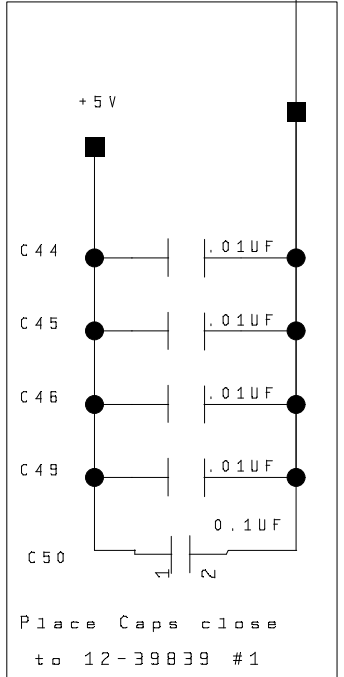
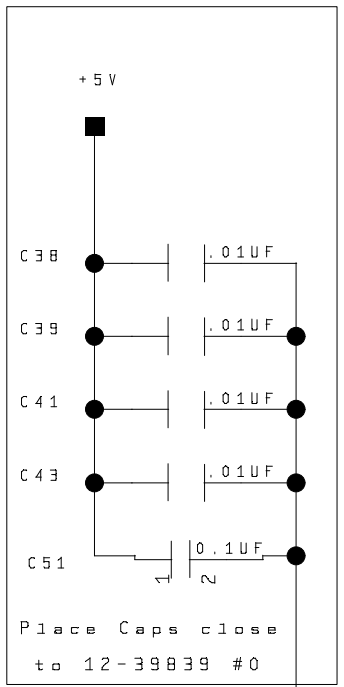
ROM and Control Lines

12-8-2000_14:08

ENG. GWRD	DATE	TITLE:	
BOARD LOCATION:	DF	DE1B55501	
SHEET	TOP DOCUMENT NUMBER:	SIZE B	CODE NUMBER
			1/1



PCI SLOT (Bottom)



15UF C53

Mount 15uf Cap close to card edge

12-8-2000_14:08		TITLE:	
ENG. GWRD	DATE	DE 1B55501	
BOARD LOCATION:		SIZE	CODE
SHEET		B	
TOP DOCUMENT NUMBER:		NUMBER	12