Technology Options for 22nm and Beyond

Kelin J. Kuhn
Intel Fellow
Intel Corporation
Director of Advanced Device Technology
AGENDA

• Scaling
• Gate control
• Mobility
• Resistance
• Capacitance
• Summary
AGENDA

• Scaling
  • Gate control
  • Mobility
  • Resistance
  • Capacitance
• Summary
### MOSFET Scaling

<table>
<thead>
<tr>
<th>Device or Circuit Parameter</th>
<th>Scaling Factor</th>
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<tbody>
<tr>
<td>Device dimension $tox, L, W$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Doping concentration $Na$</td>
<td>$\kappa$</td>
</tr>
<tr>
<td>Voltage $V$</td>
<td>$1/\kappa$</td>
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<tr>
<td>Current $I$</td>
<td>$1/\kappa$</td>
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<tr>
<td>Capacitance $\varepsilon A/t$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Delay time/circuit $VC/I$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Power dissipation/circuit $VI$</td>
<td>$1/\kappa^2$</td>
</tr>
<tr>
<td>Power density $VI/A$</td>
<td>1</td>
</tr>
</tbody>
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*R. Dennard, IEEE JSSC, 1974*

### Classical MOSFET scaling

was first described by Dennard in 1974
MOSFET Scaling

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R. Dennard, IEEE JSSC, 1974

Classical MOSFET scaling ENDED at the 130nm node (and nobody noticed ...)
90 nm Strained Silicon Transistors

Strained silicon provided increased drive currents, making up for the loss of classical Dennard scaling.
45nm High-k + Metal Gate Transistors

45 nm HK+MG

Hafnium-based dielectric
Metal gate electrode

High-k + metal gate transistors restored gate oxide scaling at the 45nm node
Changes in Scaling

THEN

• Scaling drove down cost
• Scaling drove performance
• Performance constrained
• Active power dominates
• Independent design-process
## Changes in Scaling

<table>
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<th>THEN</th>
<th>NOW</th>
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<tr>
<td>Scaling drove down cost</td>
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<tr>
<td>Scaling drove performance</td>
<td><strong>Materials</strong> drive performance</td>
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<tr>
<td>Performance constrained</td>
<td><strong>Power</strong> constrained</td>
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<tr>
<td>Active power dominates</td>
<td><strong>Standby power</strong> dominates</td>
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<tr>
<td>Independent design-process</td>
<td><strong>Collaborative</strong> design-process</td>
</tr>
</tbody>
</table>

130nm  90nm  65nm  45nm  32nm
Consistent 2-year scaling

- 90nm – TALL 1.0 μm²
- 65nm – WIDE 0.57 μm²
- 45nm – WIDE 0.346 μm²
- 32nm – WIDE 0.171 μm²
- 22nm – WIDE 0.092 μm²

- 90 nm 2003
- 65 nm 2005
- 45 nm 2007
- 32 nm 2009
- 22 nm 2011 projected
Transistor Performance

32 nm transistors continue Moore’s Law with improved drive at reduced pitch
Consistent SRAM Density Scaling

K. Zhang, ISCC, 2009; M. Bohr IDF 2010

Bitcell Area ($\mu m^2$)

2X bitcell area scaling

Process generation

90nm  65nm  45nm  32nm  22nm

K. Zhang, ISCC, 2009; M. Bohr IDF 2010
AGENDA

• Scaling
• Gate control
  • Mobility
  • Resistance
  • Capacitance
• Summary
MOSFET Challenges

- Resistance (Decreased S/D opening)
- Capacitance (Increased fringe to contact/facet)
- Gate control (SCE limitations with smaller Leff)
- Mobility (Reduced strain with decreased pitch)
MOSFET Challenges

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Ultra-thin body with RSD

Contact

Spacer

Gate

Epi RSD

Ultra-thin body (UTB)
MuGFET

Contact

Spacer

Gate

Vertical thin body
MuGFET VARIANTS

- FINFET
- TRIGATE
- PI-GATE
- Ω-GATE
- GAA (GATE-ALL-AROUND)
Nanowire

Contact

Spacer

Gate

Nanowire
Looking at all these in more detail
Ultra-thin body with RSD

Benefits

- Extension of planar technology (less disruptive to manufacturing)
- Improved RDF (low doped channel)
- Excellent channel control
- Potential for body bias

Compatible with RSD technology
Ultra-thin body with RSD

Challenges

- Capacitance: (Increased fringe to contact/facet)
- Variation: (film thickness changes affects VT and DIBL)
- Rext: (Xj/Tsi limitations)
- Strain: (strain transfer from S/D into the channel)
- Performance: (transport challenges with thin Tsi)
- Manufacturing: (requires both thin Tsi and thin BOX)
- Variation: (film thickness changes affects VT and DIBL)
Ultra-thin body

Barral – CEA-LETI – IEDM 2007

Cheng – IBM – VLSI 2009

NFET
Silicide
Faceted epi

PFET
20nm

Ultra-thin body

Drain current $I_{DS}$ (A/μm)

Gate voltage $V_{GS}$ (V)

Si film thickness $t_{Si}$ (nm)

DIBL (mV/V)

Drain Current (A/μm)

Gate Voltage (V)

Ref [1]
1.1 V

Ref [5]
1.1 V

Intel
Kelin Kuhn / IWJT / Shanghai / 2010
MuGFET

Benefits

- Double-gate relaxes Tsi requirements
  - Fin Wsi > UTB Tsi
  - (less scattering, improved VT shift)

- Nearly ideal sub-threshold slope
  - (gates tied together)

- Improved RDF
  - (low doped channel)

- Excellent channel control

- Can be on bulk or SOI
**MuGFET with RSD**

- Double-gate relaxes Tsi requirements
  - Fin Wsi > UTB Tsi
  - (less scattering, improved VT shift)

- Nearly ideal sub-threshold slope
  - (gates tied together)

- Compatible with RSD technology

- Improved RDF
  - (low doped channel)

- Excellent channel control

**Benefits**
MuGFET

Benefits

- Double-gate relaxes Tsi requirements
  - Fin Wsi > UTB Tsi
  - (less scattering, improved VT shift)

- Possibility for independent gate operation

- Improved RDF
  - (low doped channel)

- Excellent channel control
MuGFET

Challenges

- Capacitance (fringe to contact/facet)
  Plus, additional “dead space” elements

- Small fin pitch (2 generation scale?)

- Fin Strain engr. (Effective strain transfer from a fin into the channel)

- Variation (Mitigating RDF but acquiring Hsi/Wsi/epi)

- Gate wraparound (Endcap coverage)

- Fin/gate fidelity on 3’D (Patterning/etch)

- Topology (Polish / etch challenges)

- Rext: (Xj/Wsi limitations)
A Folded-channel MOSFET for Deep-sub-tenth Micron Era

Digh Hisamoto, Wen-Chin Lee*, Jakub Kedzierski*, Erik Anderson**, Hideki Takeuchi†, Kazuya Asano**, Tsu-Jae King*, Jeffrey Bokor*, and Chenming Hu*

Central Research Laboratory, Hitachi Ltd., †) EECS, UC Berkeley,
**) Lawrence Berkeley Laboratory, +) Nippon Steel Corp., ++) NKK Corp.

1. Folded channel MOSFET layout design and device structure. Bottom is A-A cross section, and the right is B-B cross section.
MuGFET

Kavalieros – Intel – IEDM 2006

Vellianitis – NXP-TSMC – IEDM 2007
MuGFET

Kang – Sematech – VLSI 2008

Chang – TSMC – IEDM 2009
Nanowire Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Improved RDF (low doped channel)
- Excellent channel control
- Nanowire further relaxes Tsi / Wsi requirements
Nanowire

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Compatible with RSD technology
- Improved RDF (low doped channel)
- Excellent channel control
Nanowire Challenges

- Gate conformity (dielectric and metal)
- Capacitance (fringe to contact/facet) Plus, additional "dead space" elements
- Variation (Mitigating RDF but acquiring a myriad of new sources)
- Fin/gate fidelity on 3'D (Patterning/etch)
- Topology (Polish / etch challenges)

Integrated wire fabrication (Epitaxy? Other?)

Wire stability (bending/warping)

Mobility degradation (scattering)

Fin Strain engr. (Effective strain transfer from wire into the channel)

Rext: (Xj/Wsi limitations)
Nanowire FETs

Yeo – Samsung – IEDM 2006

Dupre – CEA-LETI – IEDM 2008
Nanowire FETs

Wong – NUS Singapore – VLSI 2009

Bangsaruntip – IBM – IEDM 2009
MOSFET Challenges

- Resistance (Decreased S/D opening)
- Capacitance (Increased fringe to contact/facet)
- Gate control (SCE limitations with smaller Leff)
- Mobility (Reduced strain with decreased pitch)
Transistor Performance Trend

Strain is a critical ingredient in modern transistor scaling.
Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation.
Etch-stop nitride (CESL)

- **Ito – NEC**
  - IEDM 2000
  - NMOS SiN strain

- **Pidin – Fujitsu**
  - IEDM 2004
  - N and PMOS

- **Mayuzumi – Sony**
  - IEDM 2007
  - Dual-cut stress liners (MG process)
Strain: Pitch dependence

NMOS
Pitch degradation increases with film pinchoff, requires higher stress, thinner films

PMOS
eSiGe S/D mobility strongly dependent on pitch

Auth, Intel, VLSI 2008
Embedded SiGe (PMOS)

Thompson – Intel
IEDM 2002 / 2004

Ghani – Intel
IEDM 2003

Chidambaram
TI / Applied Materials
VLSI - 2004
Embedded Si:C (NMOS)

Ang – NUS-Singapore
IEDM 2004
Selective epi SiC (undoped)

Yang – IBM
IEDM 2008
In-situ epi P-SiC

Chung – Nat’l Chiao Tung U.
VLSI 2009
Implanted C + SPE
Strain: Pitch dependence

NMOS
Pitch degradation increases with film pinchoff, requires higher stress, thinner films

PMOS
eSiGe S/D mobility strongly dependent on pitch

Auth, Intel, VLSI 2008
Strain: Pitch dependence

What about strain options less sensitive to pitch?
Stress Memorization (SMT)

- Ota – Mitsubishi
  IEDM 2002
  NMOS SMT

- Chen – TSMC
  VLSI 2004
  NMOS SMT

- Wei – AMD
  VLSI 2007
  Multiple liners
Metal stress (gate and contact)

Kang – Sematech
IEDM 2006

Auth – Intel
VLSI 2008
Enhanced PMOS strain: Gate last HiK-MG

Before gate removal  After gate removal

Wang – Sony  VLSI 2007

Auth – Intel  VLSI 2008

14% RMG
ORIENTATION

(100) surface – top down

- Standard wafer / direction
  - (100) Surface / <110> channel
  - (100) Surface / <100>
    (a “45 degree” wafer)

- Both <110> directions are the same.

(110) surface – top down

- Non-standard
  - (110) Surface

- Three possible channel directions
  - <110> <111> and <100>
Non-standard (110) Surface

Three possible channel directions
<110>, <111> and <100>

Both <110> directions are the same.

(100) BEST NMOS

(a)

Electron mobility on (110) vs. (100)

(110)/<110>

(100)/<110>

(110) <110> BEST PMOS

(b)

Hole mobility on (110) vs. (100)

(100)/<110>

(110)/<110>

Yang
AMD/IBM
EDST 2007

Kelin Kuhn / IWJT / Shanghai / 2010
PMOS Vertical Devices on (100)

(110) surface <110> channel results when a VFET is fabricated on typical (100) Si - good for PMOS, not for NMOS

Chang - IBM – TED 2004

Kinugawa-Toshiba
VLSI 1986
Put NMOS at 45 degrees to PMOS?

(100) surface <100> channel for a VFET fabricated at 45 degrees typical (100) Si – very challenging for lithography.
Strain and Orientation
Piezoresistive coefficient as a function of direction

Comparison of (001), (110) and (111) Uniaxial- and Biaxial- Strained-Ge and Strained-Si PMOS DGFETs for All Channel orientations: Mobility Enhancement, Drive Current, Delay and Off-State Leakage

Tejas Krishnamohan, Donghyun Kim, Thanh Viet Dinh, Anh-tuan Pham, Bernd Meierzhagen, Christoph Jungemann, Krishna Saraswat
MOSFET Challenges

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Planar Resistive Elements

- \( R_{\text{CONTACT}} \)
- \( R_{\text{SILICIDE}} \)
- \( R_{\text{INTERFACE}} \)
- \( R_{\text{EPI}} \)
- \( R_{\text{SPREADING}} \)
- \( R_{\text{ACCUMULATION}} \)
Technology trends
Xj/Tsi, Lg, Racc

Technology Year
ITRS 2007 [19]

Technology Node
Noori - Applied Materials
TED 2008 [20]
# RTA effective annealing times

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Rampup Rate (C/s)</th>
<th>Typical peak time (s)</th>
<th>Rampdown Rate (C/s)</th>
<th>Effective Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soak</td>
<td>75</td>
<td>5-30</td>
<td>40</td>
<td>~5+t_{hold}</td>
</tr>
<tr>
<td>Spike</td>
<td>250</td>
<td>&lt;0.5</td>
<td>75</td>
<td>~1</td>
</tr>
<tr>
<td>Flash</td>
<td>1e5-1e6</td>
<td>&lt;1e-6</td>
<td>~1e6</td>
<td>0.1-1 ms</td>
</tr>
<tr>
<td>Scanning laser</td>
<td>1e5-1e6</td>
<td>&lt;1e-6</td>
<td>&gt;1e6</td>
<td>0.1-1 ms</td>
</tr>
<tr>
<td>Melt (laser)</td>
<td>1e7-1e8</td>
<td>&lt;1e-8</td>
<td>&gt;1e7</td>
<td>10-100ns</td>
</tr>
</tbody>
</table>

Effective annealing times are computed with realistic ramp shapes, assuming dominant Ea~5eV.
Annealing techniques: by physics of activation

- Melt Laser
- Flash or SubMelt Laser
- Spike RTA
- Soak RTA

Annealing techniques:
- by physics of activation
Annealing techniques:
by physics

Flash/submelt laser processes have the potential to "freeze" dopant profiles in place
Submelt Laser Anneal Test Stand

• Guassian beam: 400 μm wide (FWHM)
• Spinning stage: dwell time 60 – 200 μs
• Constant dwell time and track spacing are maintained by synchronizing spin speed and x-stage position
Submelt Laser Anneal Test Results

Junction depth = 26 nm
Sheet resistance = 150 Ω/sq

Junction depth = 28 nm,
Sheet resistance = 150 Ω/sq

Phosphorus

Arsenic

Freezing implants in place:
Submelt laser anneal showing no diffusion after 200 μS anneal
Dopant solubility limits are controlled by slower rather than faster processes permitting super-activation.

Slow characteristic times include clustering or precipitation reactions.

Fast characteristic times include Si Int diffusion and clustering and dopant substitutionality via substitutional-interstitial exchange reaction.
Superactivation with solid-phase epitaxial regrowth (SPER)

Laser melt anneal vs RTA, showing increased abruptness and non-equilibrium enhanced activation (superactivation).
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Planar Capacitive Elements

- Gated-edge junction
- Area junction
- Cjunction
- Cfringe to contact
- Cfringe to facet
- Cfringe to diffusion (of/ff)
- Cxud - device component of Cov (XUD-based)
- Channel component of Cgate

Kuhn, Intel, IEDM SC 2008
Innovative Spacer Technologies

SPACER REMOVAL
Liow – NUS Singapore
EDL 2008

SiBCN (Low-K) SPACER
Ko – TSMC
VLSI 2008
AGENDA

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# Looking Forward

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<tr>
<th>Low risk</th>
<th>Medium Risk</th>
<th>High risk</th>
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<td>Enhancements in strain technology</td>
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<tr>
<td>Enhancements in annealing/implant technology</td>
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<td>Optimized substrate and channel orientation</td>
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<td>Reduction in MOS parasitic resistance</td>
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<td>UTB devices</td>
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