Peering into Moore’s Crystal Ball: Transistor Scaling beyond the 15nm node

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AGENDA

• Scaling
• Gate control
• Mobility
• Resistance
• Capacitance
• Summary
Consistent 2-year scaling

90nm – TALL
1.0 μm²

65nm – WIDE - 0.57 μm²

45nm – WIDE
0.346 μm²

32nm – WIDE
0.171 μm²

22nm – WIDE
0.092 μm²

90 nm
2003

65 nm
2005

45 nm
2007

32 nm
2009

22 nm
2011
projected

90: 7
65: 8
45: 9
32: 9
Changes in Scaling

**THEN**
- Scaling drove down cost
- Scaling drove performance
- Performance constrained
- Active power dominates
- Independent design-process

**NOW**
- Scaling drives down cost
- **Materials** drive performance
- **Power** constrained
- **Standby power** dominates
- **Collaborative** design-process

Kelin Kuhn / Int’l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010
Consistent SRAM Density Scaling

K. Zhang, ISCC, 2009; M. Bohr IDF 2010
AGENDA

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Short Channel Control: HiK-MG

High-k/MG enabled 0.7X ToxE scaling while reducing Ig >> 25X for NMOS and 1000X for PMOS

HiK+MG

45 nm HK+MG

65nm: Bai 2004 IEDM
Ultra-thin body with RSD

Benefits

Extension of planar technology (less disruptive to manufacturing)

Compatible with RSD technology

Improved RDF (low doped channel)

Excellent channel control

Potential for body bias
Ultra-thin body with RSD

Challenges

Capacitance: (Increased fringe to contact/facet)

Variation: (film thickness changes affect VT and DIBL)

Rext: (Xj/Tsi limitations)

Strain: (strain transfer from S/D into the channel)

Manufacturing: (requires both thin Tsi and thin BOX)

Performance: (transport challenges with thin Tsi)
Ultra-thin body

Cheng – IBM – VLSI 2009
MuGFET

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)
- Improved RDF (low doped channel)
- Excellent channel control
- Can be on bulk or SOI

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MuGFET with RSD

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)
- Improved RDF (low doped channel)
- Excellent channel control
- Compatible with RSD technology
MuGFET

Benefits

Double-gate relaxes Tsi requirements Fin Wsi > UTB Tsi (less scattering, improved VT shift)

Possibility for independent gate operation

Improved RDF (low doped channel)

Excellent channel control
MuGFET

Challenges

Variation (Mitigating RDF but acquiring Hsi/Wsi/epi)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Gate wraparound (Endcap coverage)

Small fin pitch (2 generation scale?)

Fin/gate fidelity on 3’D (Patterning/etch)

Fin Strain engr. (Effective strain transfer from a fin into the channel)

Rext: (Xj/Wsi limitations)

Topology (Polish / etch challenges)
Nanowire Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Improved RDF (low doped channel)
- Excellent channel control
Nanowire

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Improved RDF (low doped channel)
- Excellent channel control
- Compatible with RSD technology

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Nanowire Challenges

Gate conformality (dielectric and metal)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Integrated wire fabrication (Epitaxy? Other?)

Variation (Mitigating RDF but acquiring a myriad of new sources)

Wire stability (bending/warping)

Fin/gate fidelity on 3’D (Patterning/etch)

Mobility degradation (scattering)

Fin Strain engr. (Effective strain transfer from wire into the channel)

Topology (Polish / etch challenges)

Rext: (Xj/Wsi limitations)
Nanowire FETs

(a) 3D-NWFET
(b) ΦFET

Bangsaruntip – IBM – IEDM 2009

Normalized delay vs. V_{DD}

D_{eff} (nm)
- 3.2
- 6.5
- 9.9
- 11.6
- 13.6
Nanowire FETs

Hashemi/Hoyt – MIT
IEDM 2008 EDL/ESSDRC 2009

Moselund – Ecole Polytechnique, Switzerland
IEDM 2007
Vertical Architectures

Benefits

- Vertical orientation may enable new circuit concepts
- 50% reduction in “plan view” density
- Possibility for different N/P materials/orientations
- Reduced vertical interconnect capacitance
Vertical Architectures

Challenges

- Rext: (Xj/Wsi limitations)
- Gate conformality (dielectric and metal)
- Thermal processing (Top layer may need to be processed over existing bottom layer)
- Fin/gate fidelity on 3’D (Patterning/etch)
- Contacts (Diffusion-diffusion, Gate-gate contacts extremely challenging)
- Topology (Polish / etch challenges)
- Lithography (May double the number of FE critical layers)
- Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)
- Variation (Mitigating RDF but acquiring a myriad of new sources)
- Strain engineering (more challenging than single layer)

Kelin Kuhn / Int’l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010
Batude – CEA LETI - IEDM 2009 – stacked 110/100

Jung – Samsung - IEEE TED 2010 – 3D stacked 6T

Kelin Kuhn / Int’l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010
TFET (Tunneling Field-Effect Transistor)

**Principle of operation**
- Band-to-band tunneling through source barrier, modulated by gate field

**Advantages**
- Steep (< 60 mV/dec) sub-threshold slope
- Large Ion/Ioff ratio

**Disadvantages**
- Low drive currents
- Ambipolar conduction
- Unidirectional conduction
- Potentially high hot-e⁻ effects

**Technology Intercept**
- Unlikely candidate for Si, Ge, or Si_{1-x}Ge_{x} systems (drive currents too low)
- Probably needs III-V band-gap engineering, perhaps with “broken-gap”

*Curtesy M. Luisier (Purdue)*
M. Luisier and G. Klimeck, EDL, 2009
Sensitivity to Source Doping Variation

TFET behavior is very sensitive to the source doping “shape”

MOS behavior has little sensitive to the source doping “shape”
Best Demonstrated TFETs

- Still MUCH lower drive currents than conventional MOS
- Require band-gap engineering with hetero-junction δ layers
- Sub-threshold slope still poor

![Graph showing Drain Current, I_D (A/μm) vs Gate Voltage, V_GS (V)]

Table I. Comparison to reported silicon TFETs. ($V_{DS} = V_{GS} - V_{BTBT} = 1.0V$)

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>SS (mV/dec)</td>
<td>52.8</td>
<td>42</td>
<td>~300</td>
<td>46</td>
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<tr>
<td>$I_{ON}$ (μA/μm)</td>
<td>12.1</td>
<td>0.01</td>
<td>1E-4</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_{ON}/I_{OFF}$</td>
<td>1E4</td>
<td>1E4</td>
<td>1E2</td>
<td>7E7</td>
</tr>
</tbody>
</table>

[1] K. Jeon, et al., VLSI (11.4.1.-1) 2010
AGENDA

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• Mobility
  • Resistance
  • Capacitance
• Summary
Transistor Performance Trend

Strain is a critical ingredient in modern transistor scaling. Strain was first introduced at 90nm, and its contribution has increased in each subsequent generation.
Strain in modern devices

Stress memorization

Wei, VLSI 2007

Ghani, IEDM 2003

Mayuzumi, IEDM 2007

Mayuzumi, IEDM 2007

Kelin Kuhn / Int'l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010

Yang, IEDM 2008

Auth, VLSI 2008
ORIENTATION

(100) surface – top down

- Standard wafer / direction
  (100) Surface / <110> channel

- (100) Surface / <100>
  (a “45 degree” wafer)

Both <110> directions are the same.

(110) surface – top down

- Non-standard
  (110) Surface

- Three possible channel directions
  <110> <111> and <100>
ORIENTATION

(100) surface – top down

- Standard wafer / direction
- (100) Surface / <110> channel
- (100) Surface / <100>
- (a “45 degree” wafer)

Both <110> directions are the same.

(110) surface – top down

- Non-standard
- (110) Surface
- Three possible channel directions
- <110> <111> and <100>

(100) BEST NMOS

(a) Mobility vs. N_INV (cm^-2)

(110) <110> BEST PMOS

(b) Hole mobility on (110) vs. (100)

Yang
AMD/IBM
EDST 2007

Kelin Kuhn / Int'l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010
Orientation and Strain:
More complex for non-(100) orientations

(100) Surface (k⊥=0) (001) Surface Vg=-1V (001) Surface Vg=-1V, Sxx=-1GPa

(110) Surface (k⊥=0) (110) Surface Vg=-1V (110) Surface Vg=-1V, Sxx=-1GPa

Kuhn/Packan, Intel, IEDM 2008
Si vs Ge MOSFETs

The introduction of manufacturable HiK-MG transistors has led to the reconsideration of Ge channels.
Ge Historical Issues: Still critical today

Narrow Bandgap

Poor Quality Dielectric

Kelin Kuhn / Int'l Symp. on Adv. Gate Stack Technology/ Sept. 29th, 2010
Narrow Bandgap

Band-to-band tunneling: challenge for low Eg materials

Adapted from Fischetti [7], Krishnamohan [60]

Adapted from Saraswat [59], Krishnamohan [60]
Since HiK-MG dielectrics typically form with a bilayer (the HiK + an interface layer) the challenge of germanium oxide still exists. Germanium oxide exists in several morphologies, unfortunately, most are hydroscopic and/or volatile.
Ge Benchmarking
III-V: The Lure of High Mobility

Adapted from J. Kavalieros – Intel - VLSI SC 2007
K. Kuhn – ECS 2010
III-V MOSFETs: “Density-of-states bottleneck”

- On-current of a MOSFET

- Velocity $v$
  - Diffusive: mobility $\mu$, $v = \mu E$
  - Ballistic: injection velocity $v_{inj}$
  - Light $m^*$ → high $\mu$, high $v_{inj}$

- Charge $Q$
  - MOS limit ($C_Q \gg C_{ox}$), $C \approx C_{ox}$
  - Light $m^*$ → less $D (C_Q)$, less $C$, less $Q$
  - More important for thin oxide (large $C_{ox}$),
    “DOS bottleneck”

\[ I = Qv \]

\[ Q = C(V_G - V_{th}) \]

\[ \frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_Q} \]

\[ C_Q = q^2 D \]
Use of L-valleys: GaAs

- GaAs 4 nm

Small DOS with high $v_{inj}$
High DOS with low $v_{inj}$

More DOS with high $v_{inj}$
Different body thicknesses (EOT=1.0 nm)

- GaSb > InGaAs > GaAs > Ge > Si
- GaSb, InGaAs > Ge, GaAs > Si
- InGaAs > GaSb > Ge, GaAs > Si

Different body thicknesses (EOT=0.5 nm)

- GaSb > GaAs > Ge > Si > InGaAs
- GaSb > Ge > GaAs > Si, InGaAs
- GaSb > Ge > GaAs, InGaAs > Si

From R. Kim
AGENDA

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Planar Resistive Elements

\[ R_{\text{CONTACT}} \]

\[ R_{\text{SILICIDE}} \]

\[ R_{\text{INTERFACE}} \]

\[ R_{\text{EPI}} \]

\[ R_{\text{SPREADING}} \]

\[ R_{\text{ACCUMULATION}} \]
Planar Resistive Elements

Racc: Sub-melt Laser Anneal

- #0 - No Laser
- #4 - 91%, 60us
- #5 - 88%, 60us
- #6 - 85%, 60us
- #7 - 54%, 200us

Kuhn, IWJT 20010

Racc: Solid-phase Epi Regrowth

Kuhn, IWJT 20010
Schottky Barrier Height Reduction is a critical area for development. Techniques under investigation include exotic alloys, implants, and Fermi-unpinning layers.
Planar Resistive Elements

R_{CONTACT} Decreased Resistance of the Contact Metal

Kuhn, IWJT 20010

R_{SILICIDE}

R_{INTERFACE}

R_{EPI}

R_{SPREADING}

R_{INTERFACE}

R_{EPI}

R_{SPREADING}

Copper Contacts
Topol, VLSI 2006

Kuhn, IWJT 20010
Schottky barrier S/D – an option?

- In a metal SB-MOS, S/D forms an atomically abrupt Schottky-barrier having the height $\phi_b$.
- The extreme limit for metal in the S/D regions (with associated improvements in $R_{ext}$)
- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)
Schottky barrier S/D – an option?

- Electron leakage set by Eg-SBH

Two possible conduction paths:
- Thermionic – over the barrier – good SS slope
- Tunneling – through the barrier – poor SS slope

- Unconventional operation (field emission device in the ON state)
- Needs complementary devices (midgap silicide or two silicides)

Metallic SD
Conventional

Larson – Spinnaker TED 2006

Hole barrier set by SBH
Schottky barrier S/D – an option?

**Benefits**
- Low bulk resistance contacts to the channel
- Very abrupt junctions
- No random s/d dopant fluctuation effects
- Minimize s/d carrier-carrier scattering effects

**Challenges**
- Poor experimental drive currents
- Requires bandedge Schottky barriers
- Ambipolar conduction (high drain-body leakage for bulk devices)
- Early contact formation limits midsection process temperatures
- Need alternative approach for s/d stressors

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**Electron leakage set by Eg-SBH**

**Metallic SD**

**Hole barrier set by SBH**

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• Summary
Planar Capacitive Elements

- Cfringe to contact
- Cfringe to facet
- Cfringe to diffusion (of/if)
- Cxud - device component of Cov (XUD-based)
- Gated-edge junction
- Gated-edge junction
- Channel component of Cgate
- Area junction

Kelin Kuhn / Int’l Symp. or Kuhn, Intel, IEDM SC 2008
Planar Capacitive Elements

Cfringe to Contact

Cfringe to facet

Cfringe to diffusion (of/if)

Cxud - device component of Cov (XUD-based)

Cchannel component of Cgate

SPACER REMOVAL
Liow – NUS Singapore
EDL 2008

SiBCN (Low-K) SPACER
Ko – TSMC
VLSI 2008

Area junction

Gate spacers removed
SiC

60nm

Si-H
N-H

Spectroscopy
Kulan Kuhn / Int’l Symp. on Adv. Gate Stack Technology / Sept. 29th, 2010

Kelvin Kuhn / Int’l Symp. or Kuhn, Intel, IEDM 08 2008
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## Looking Forward

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<th>Medium Risk</th>
<th>High risk</th>
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<td>Enhancements in strain technology</td>
<td>Optimized substrate and channel orientation</td>
<td>UTB devices / MuGFETS</td>
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<tr>
<td>Enhancements in HiK/MG technology</td>
<td>Reduction in MOS parasitic resistance</td>
<td>Nanowires</td>
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<td>Reduction in MOS parasitic capacitance</td>
<td>3’D Stacked Devices</td>
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<td>Advanced materials (Ge/III-V)</td>
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