CMOS Transistor Scaling Past 32nm and Implications on Variation

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AGENDA

I. Overview – variation sources
II. Next generation variation – lithography
III. Next generation variation – polish
IV. Next generation devices
V. Measurements, results and interpretation
VI. Closing thoughts
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VARIATION SOURCES

Contact
Spacer
Gate
Epi RSD

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Putting it all together for the gate layer of a 65nm MPU (magnified 25,000X)
Phase mask data

Putting it all together for the gate layer of a 65nm MPU

(magnified 25,000X)

C. Kenyon
TOK conf.
Dec. 2008

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Layout Restrictions 65nm to 32nm

65 nm Layout Style

- Bi-directional features
- Varied gate dimensions
- Varied pitches

32 nm Layout Style

- Uni-directional features
- Uniform gate dimension
- Gridded layout

M. Bohr, ISCC, 2009
Design → OPC/RET → Phase mask data → Trim mask data → Reticle manufacturing → Trim mask → Exposure → Etch

Putting it all together for the gate layer of a 65nm MPU

(magnified 25,000X)
Optical Proximity Correction (OPC) As a Resolution Enhancement Technique

Contour prediction – no OPC
Contour prediction – with OPC

SEM Image – no OPC
SEM Image – with OPC

K. Wells-Kilpatrick: 2007
Top-down resist CD meets spec, but poor contrast leads to poor resist profile which gets transferred to metal pattern after etch, resulting in shorting marginality.

Computational lithography solution

K. Kuhn, IEDM 2007
Putting it all together for the gate layer of a 65nm MPU (magnified 25,000X)
MEEF
Mask Error Enhancement Factor

• MEEF is a scaling factor that causes certain layout geometries to exhibit a greater sensitivity to mask dimension tolerances.

• Any dimensional error in the mask is magnified on the wafer by the MEEF value.

\[ \Delta W_{\text{wafer}} = \text{MEEF} \times \Delta W_{\text{mask}} \]

• Depending on the value of the mask error and the lithography exposure/focus conditions the final printed pattern can be either larger or smaller.
MEEF Impact on Ze Error

Ze error can be either positive or negative.

Yellow: DCCD contour after OPC
Green: with -3.375 nm mask making error
Red: with 3.375 nm mask making error

65nm Simulation
Notch width = 120nm
Notch height = 250nm

MEEF = 8.4
Low MEEF requires targeting in the “flat” portion of CD vs. pitch.

Process innovations continue this trend in the 32nm node.
Design

OPC/RET

Putting it all together for the gate layer of a 65nm MPU

(magnified 25,000X)

Phase mask data

Trim mask data

Reticle manufacturing

Phase mask

Trim mask

Exposure

Etch

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FLARE

- Flare is unwanted scattered light arriving at the wafer.
- Flare is caused by interactions that force the light to travel in a "non-ray trace" direction.
- Flare is both a function of local environment around a feature (short range flare) and the total amount of energy going through the lens (long range flare).
Impact of flare on gate CDs

- All structures have identical reticle CD and pitch

High chrome density

Moderate chrome density

Low chrome density

- During 65nm process development, large CD deviations were observed for structures having identical pitch and reticle CD due to flare
- Gates only 500\(\mu m\) away from one another could be >5nm different in CD

C. Kenyon
TOK conf.
Dec. 2008

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Flare Variation Improvement with OPC

Development effort produced an algorithm capable of scanning designs and binning regions by local chrome fraction. Binning algorithm is combined with flare-calibrated OPC model.

C. Kenyon, TOK conf., Dec. 2008
Design

OPC/RET

Phase mask data

Reticle manufacturing

Trim mask data

Phase mask

Trim mask

Exposure

Putting it all together for the gate layer of a 65nm MPU

(magnified 25,000X)

Etch

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C. Kenyon
TOK conf.
Dec. 2008
45nm highlights role of lithography/etch in resolving LER/LWR

Original

Improvement A

Improvements B,C

Final after improvements A,B,C

K. Kuhn, ITJ, 2008
Technology Trend
Systematic Gate CD Lithography Variation

Critical to management of variation is the ability to deliver a 0.7X gate CD variation improvement in each generation enabled by continuous process technology improvements.
Extend 193nm Optical Lithography as far as possible
Deploy EUV Lithography when available/affordable
Non-EUV Lithography Beyond 32 nm

Double Patterning
• Pitch doubling
• Improved 2-D features

Spacer Gate Patterning
• Pitch doubling
• Improved variation

Pitch Doubling

2-D Features

M. Bohr, ISCC, 2009
Bencher et al, Proc. of SPIE Vol. 6924 69244E-7
Pitch doubling and gate CD control

Neither Resist Freeze nor Double Pattern Transfer achieve full benefit of patterning at ½ pitch.

Both techniques still require resolution of a very small space (MEEF, LWR etc.)

C. Kenyon, TOK conf., Dec. 2008
Disadvantages of Double-patterning

Misalignment between the 2 exposures is a crucial liability for this technique and can limit its usability. Transistor parameters can be affected by asymmetry between the source and drain regions.
Pitch doubling and gate CD matching

Pitch doubling eliminates the close correlation which currently exists between the CDs of adjacent gates. This has implications for memory cells and other circuits which depend upon this CD matching.

C. Kenyon, TOK conf., Dec. 2008
Pitch doubling and gate CD matching

Single patterning: the distribution of CD mismatches between adjacent gates is a very small fraction of total gate CD variation

Pitch doubling: the distribution of CD mismatches is GREATER than the total gate CD variation

C. Kenyon, TOK conf., Dec. 2008
Non-EUV Lithography Beyond 32 nm

Double Patterning
- Pitch doubling
- Improved 2-D features

Spacer Gate Patterning
- Pitch doubling
- Improved variation

M. Bohr, ISCC, 2009
Bencher et al, Proc. of SPIE Vol. 6924 69244E-7
Spacer patterning retains correlation between doubled features
Alternative: Spacer patterning

Potential asymmetries

Cross-section

Top-down

However, spacer patterning comes with challenges of its own

Bencher et al, Patterning by CVD Spacer Self Alignment DoublePatterning (SADP), Proc. of SPIE Vol. 6924 69244E-7
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HiK-MG: Gate First vs Gate Last

**Gate-First**

- Dep Hi-k & Met 1
- Patt Met 1 & Dep Met 2
- Patt Met 2 & Etch Gates
- S/D formation & Contacts

**Hik-First, Gate-Last**

- Dep & Patt Hik+Gate
- S/D formation & ILD dep/polish
- Rem Gate & Patt Met 1
- Dep Met 2+Fill & Polish

**Advantages of gate last flow**

- **High Thermal budget available for Midsection**
  - Better Activation of S/D Implants
- **Low thermal budget for Metal Gate**
  - Large range of Gate Materials available
- **Significant enhancement of strain**
  - Both NMOS and PMOS benefit
CMP Integration at 45 nm – HiK Metal Gate

- STI deposition and polish
- Wells and VT implants
- ALD deposition of high-k gate dielectric
- Polysilicon deposition and gate patterning
- S/D extensions, spacer, Si recess and SiGe deposition
- S/D formation, Ni silicidation, ILD0 deposition
- Poly Opening Polish, Poly removal
- PMOS workfunction metal deposition
- Metal gate patterning, NMOS WF metal deposition
- Metal gate fill and polish, ESL deposition

First Generation HiK – Replacement Metal Gate
Three critical CMP operations in the FE

K.Mistry et al., IEDM (2007)
C.Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM (2008)
First Generation HiK – Replacement Metal Gate

Three critical CMP operations in the FE
STR Pattern Density Variation Impact

High Pattern Density

Low Pattern Density

Post STI Deposition

Nitride
Silicon
Oxide

Slower Polish Rate

Faster Polish Rate

Post STI Polish

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STI Step Height Variation

- High Pattern Density Area
- Low Pattern Density Area

STI topography impacts transistor $L_e$ and $Z_e$

Positive Step Height

Zero Step Height
STI Step Height Variation

High Pattern Density Area

Low Pattern Density Area

Poly

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STI Step Height Impact on Gate CD

Negative Step Height

“Dogbone”
Lg is longer at the diffusion boundary

Positive Step Height

“Icicle”
Gate CD is shorter at the diffusion boundary
CMP Integration at 45 nm – HiK Metal Gate

STI deposition and polish
Wells and VT implants
ALD deposition of high-k gate dielectric
Polysilicon deposition and gate patterning
S/D extensions, spacer, Si recess and SiGe deposition
S/D formation, Ni silicidation, ILD0 deposition
Poly Opening Polish, Poly removal
PMOS workfunction metal deposition
Metal gate patterning, NMOS WF metal deposition
Metal gate fill and polish, ESL deposition

K. Mistry et al., IEDM (2007)
C. Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM (2008)

First Generation HiK – Replacement Metal Gate
Three critical CMP operations in the FE
Variation Challenges of RMG CMP Steps

- Gate height control critical to reducing variation
- PMOS/NMOS differences complicate CMP

C. Auth et al. VLSI Symp, (2008)
J. Steigerwald, IEDM 2008
Variation Challenges of RMG CMP Steps

OVERPOLISH
- Exposes raised S/D
- Rext/mobility impact

UNDERPOLISH
- Underetched contact
- Rext impact

S/D region – attacked during poly etch

S/D region – marginal contact

Gate region

NMOS S/D region contact

J. Steigerwald, IEDM 2008
45 nm: POP CMP Improvement
Overscaling Topography Improvement

Improvements in polish enabled dramatic improvements in topography variation

J. Steigerwald, IEDM 2008
Generational Improvements
Patterning and Polish

65nm to 22nm: Patterning and polish enhancements

- Improved CD uniformity across STI boundaries
- Square corners (eliminate “dogbone” and “icicle” corners)
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MOSFET Challenges

- Capacitance (Increased fringe to contact/facet)
- Resistance (Decreased S/D opening)
- Gate control (SCE limitations with smaller Leff)
- Mobility (Reduced strain with decreased pitch)
Next Generation

- Resistance ( Decreased S/D opening )
- Capacitance ( Increased fringe to contact/facet )
- Contact
- Gate
- Epi RSD

MOSFET Challenges

- Gate control ( SCE limitations with smaller Leff )
- Mobility ( Reduced strain with decreased pitch )

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Ultra-thin body with RSD
MuGFET

Contact

Spacer

Gate

Vertical thin body
MuGFET VARIANTS

FINFET
TRIGATE
PI-GATE

Ω-GATE
GAA (GATE-ALL-AROUND)

Nearly ideal sub-threshold operation (gates tied together)

Silicon $\Omega$-GATE GAA (GATE-ALL-AROUND)
Looking at all these in more detail
Ultra-thin body with RSD

Benefits

- Extension of planar technology (less disruptive to manufacturing)
- Improved RDF (low doped channel)
- Compatible with RSD technology
- Excellent channel control
- Potential for body bias
Ultra-thin body with RSD

Challenges

- Capacitance (Increased fringe to contact/facet)
- Variation: (film thickness changes affects VT and DIBL)
- Rext: (Xj/Tsi limitations)
- Strain: (strain transfer from S/D into the channel)
- Manufacturing: (requires both thin Tsi and thin BOX)
- Performance: (transport challenges with thin Tsi)
Ultra-thin body

Barral – CEA-LETI– IEDM 2007

Cheng – IBM – VLSI 2009

Kelvin Kuhn / ASMC / SFO 2010
MuGFET

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Double-gate relaxes Tsi requirements, Fin Wsi > UTB Tsi (less scattering, improved VT shift)
- Improved RDF (low doped channel)
- Can be on bulk or SOI

Excellent channel control
MuGFET with RSD

Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Double-gate relaxes Tsi requirements
  Fin Wsi > UTB Tsi
  (less scattering, improved VT shift)
- Improved RDF (low doped channel)
- Excellent channel control
- Compatible with RSD technology
MuGFET

Benefits

- Double-gate relaxes Tsi requirements
  - Fin Wsi > UTB Tsi
  - (less scattering, improved VT shift)

- Possibility for independent gate operation

- Improved RDF
  - (low doped channel)

- Excellent channel control
MuGFET

Challenges

Variation (Mitigating RDF but acquiring Hsi/Wsi/epi)

Gate wraparound (Endcap coverage)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Small fin pitch (2 generation scale?)

Fin Strain engr. (Effective strain transfer from a fin into the channel)

Rext: (Xj/Wsi limitations)

Fin/gate fidelity on 3’D (Patterning/etch)

Topology (Polish / etch challenges)
MuGFET

Kavalieros – Intel – IEDM 2006

Chang – TSMC – IEDM 2009

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Nanowire Benefits

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Improved RDF (low doped channel)
- Excellent channel control
Benefits

Nanowire

- Nearly ideal sub-threshold slope (gates tied together)
- Nanowire further relaxes Tsi / Wsi requirements
- Improved RDF (low doped channel)
- Compatible with RSD technology
- Excellent channel control
Nanowire Challenges

Gate conformality (dielectric and metal)

Capacitance (fringe to contact/facet) (Plus, additional “dead space” elements)

Integrated wire fabrication (Epitaxy? Other?)

Wire stability (bending/warping)

Variation (Mitigating RDF but acquiring a myriad of new sources)

Mobility degradation (scattering)

Fin/gate fidelity on 3D (Patterning/etch)

Fin Strain engr. (Effective strain transfer from wire into the channel)

Rext: (Xj/Wsi limitations)

Topology (Polish / etch challenges)
Nanowire FETs

Dupre – CEA-LETI – IEDM 2008

Bangsaruntip – IBM – IEDM 2009

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Systematic and Random

- Statistician’s viewpoint:

- Process engineer’s viewpoint:

- Device engineer’s viewpoint:
Measurement of Random and Systematic VT Variation at the Device Level

Traditional method:
1. Measure two identical adjacent devices and extract the difference $\sigma(VT_A - VT_B)$
2. Measure the entire population of all devices and extract $\sigma(VT_{pop})$

Random Variation for a matched pair

$$Random_{mp} = \text{StdDev}(VT_A - VT_B) = \sigma(DVT)$$

Random Variation for a single device

$$Random_{\text{one-device}} = \frac{\text{StdDev}(VT_A - VT_B)}{\sqrt{2}} = \frac{\sigma(DVT)}{\sqrt{2}}$$

Systematic Variation for a single device

$$Systematic = \sqrt{(\sigma VT_{pop})^2 - \left(\frac{\sigma(DVT)}{\sqrt{2}}\right)^2}$$
Using Arrays for Variation Measurement
(this example is metal resistors)

1024 Etest structures in nominal density

256 structures in low density fillers

256 structures in high density fillers

256 Nom density fillers

256 Nom density fillers
Using Arrays for Variation Measurement
(this example is metal resistors)
Using Arrays for Variation Measurement
(this example is metal resistors)
Important of Comprehending de-Biasing in Arrays
Random and Systematic Variation
for Matched Ring Oscillators

Random:
• Calculate Delta
  \[ \Delta = \frac{\text{Freq}_A - \text{Freq}_B}{\sqrt{\text{Freq}_A + \text{Freq}_B}} \times 200 \]

• Random Variation
  \[ \text{Rand} = \text{StdDev}(\Delta) \] per data unit

Systematic:
• Total Sigma
  \[ \sigma = \text{StdDev}(\text{Freq}_A) \] per data unit

• Grand Mean
  \[ \mu = \frac{\text{Mean}(\text{Freq}_A) + \text{Mean}(\text{Freq}_B)}{2} \]

• Systematic Variation
  \[ \text{Syst} = \sqrt{\left(\frac{\sigma}{\mu}\right) \times 100}^2 - \text{Rand}^2 \] per data unit

Total Variation:
\[ \text{Total} = \frac{\text{StdDev}(\text{Freq}_A) \times 100}{\text{Mean}(\text{Freq}_A)} \] per data unit
45nm Product wafer: Random variation

K. Kuhn, ITJ 2008

Delta 4-5

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Random and Systematic Variation Trends

Systematic WIW variation is comparable from one generation to the next.

Random WIW variation in 32nm is comparable to 45nm and significantly improved over 65nm and 90nm due to HiK-MG.
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Yield: A pragmatic measure of variation

Defect Density (log scale)

350 nm 250 nm 180 nm 130 nm 90 nm 65 nm 45 nm 32 nm

Yield: A pragmatic measure of variation

Defect Density (log scale)

90 nm  65 nm  45 nm  32 nm

2002 2003 2004 2005 2006 2007 2008 2009


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Closing Thoughts

Process variation is not an insurmountable barrier to Moore’s Law, but is simply another challenge to be overcome.