Emerging Technologies & Research Focus

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Enabling a Steady Technology Cadence

TECHNOLOGY GENERATION

<table>
<thead>
<tr>
<th>Technology</th>
<th>Year</th>
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<tr>
<td>65nm</td>
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What to do now to enable these future generations?

Defined

To be defined
Ideal View of Research

Beyond

8 nm

11 nm

15 nm

22 nm

32 nm

Monitor

Prune

Integrate

Productize

Ramp

Internal Research

Decide

Development

External Research

Broad exploration
Create Options

Discovery
Enable long lead

Critical projects
Fill Gaps
Some Key Areas

- **Material integration**
  - Research to understand & manage below 15nm features
  - New materials which allow new functions
  - Managing granularity at small dimensions

- **New function integration**
  - Moving difficult to scale into easier to scale
  - Interfaces and interconnections
  - New functionality to make a platform more valuable

- **Devices as part of a connected network**

- **Discovery beyond our current visibility**

- **Mechanisms to rationalize and mature the portfolio of research investments**
Future Visibility: Lithography

Current Status
- 1st gen EUV tools have 0.25NA, sub 0.5nm wave front error
- Designs evaluated to 0.6NA
- Process window to 23nm HP, currently resist limited

Needed Focus
- Higher NA EUV
- Revolutionary materials
- Need progress on diffusion, sensitivity, integration
- Exotic: ebeam, self-assembly

20 nm L/S
17 nm L/S
16 nm L/S grating using EUV interference (ZnO4)

Modeled MET resolution
193i will coexist even when EUV ready

Line Doubling

More masks equal more printed information

2-D Features

Conventional Mask Structure

Alternate Phase Shift

More density for given printed information

Edge Doubling

Edge Quadrupling

More printed information for given tool capability
Complementary advantages

- Allows use of 1\textsuperscript{st} gen EUV tools = earlier start to development
- Better line edge roughness, sharper corners
- Less sensitive to mask defects
- Common design rules
Designing Materials with Smooth Grains

**Polymer Blend**
+ Mature materials platform
- Larger individual components

**Molecular glass**
+ Higher sensitivity at same resolution
- Lower mechanical strength (currently)

Need to engineer materials with components below 1nm

Future Visibility: Devices

Current Status
• Smallest Si devices functional to sub-10nm but poor on-off
• Increasing dimensional challenge to incorporate strain

Needed Focus
• New materials with bottoms-up fill to improve R & C
• Higher mobility materials to allow voltage scaling
• New device types, go vertical
• Exotic: graphene, CNT

Graphene
CNT
Nanowires
5nm
QW III-V Device
Contacted gate pitch
III-V Progress Scorecard

• Integration of III-V on Si – Feasibility demonstrated using MBE
  – Intel paper @ IEDM 2007

• Enhancement-mode operation – Feasibility demonstrated
  – MIT papers @ IEDM 2006 and 2007
  – Intel paper @ IEDM 2007

• III-V hole mobility (P-type) not high enough – Strain demo
  – Intel paper @ IEDM 2008
  – Ge PMOS QW devices may be alternatives

• Gate dielectric on III-V layers of interest – Demonstrated
  – Research on surface prep, novel materials

• Scalability compared to Si devices unknown
  – Work started on self-alignment, alternative geometries
  – Modeling efforts underway at universities and internal

• Manufacturing tool feasibility
  – Research tool selected
Future Visibility: Interconnects

Current Status
- Bottoms-up fill okay to about 20-25nm, liner is the limiter
- No “better than Cu” option
- <20nm L/S might exceed dielectric breakdown limit

Needed Focus
- Thin conformal plateable barrier … or self forming barrier
- Tall vias might use non-Cu
- Non-SiO2 dielectrics
- Exotic long interconnects: CNT (10’s um), optical (>mm)
Optical Interconnects

Nearer term: High bandwidth chip-chip interconnects

Longer term: On-chip interconnects

40 Gbps at 2.7Vpp

Ref. I. Young, paper 28.1, ISSCC ’09
3-D Chip Stacking & Other ways to integrate

+ High density chip-chip connections
+ Small form factor
+ Combine dissimilar technologies

? Added cost
? Degraded power delivery, heat sinking
? Area impact on lower chip

3-D chip stacking using through-silicon vias
Our limit to visibility goes out ~10 years

### TECHNOLOGY GENERATION

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- **Silicon lattice is ~ 0.5nm, hard to imagine good devices smaller than 10 lattices across – reached in 2020**

- **Carbon Nanotube**
  - ~1nm diameter

- **Graphene**
  - 1 atom thick

- **QW III-V Device**
  - 5nm

- **Nanowire**
  - 10 atoms across

- **Intel**

- [Image of Carbon Nanotube and Graphene]

- [Image of QW III-V Device and Nanowire]
Beyond 2020 and possible futures

- Conventional fabrication architectures continue
  - Individual steps continue as 2D layers
  - More and more layers stacked to give increasing function

Graphene layers can couple together and create a quantum condensate

Bilayer graphene structure
Theoretically >10000x less power

Beyond 2020 and possible futures

- Conventional fabrication architectures continue
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- Increasing use of heterogeneous technologies and novel ways to combine technologies
  - Mixture of tops-down and bottoms-up fabrication (ex. ALD, directed self assembly)
  - Eliminating, reducing cost of interfaces (ex. stacking)

Crafting Films with Atomic Layer Deposition
Beyond 2020 and possible futures

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• Non-binary or alternate state computation
  – Same fabrication complexity, more value per function

Spin wave majority phase logic

- Concept based on spin wave generation, modulation and detection
- Multi-bit transmission and processing
- No charge motion & Energy/bit = 1-100KT
- Championed by the WIN center at UCLA

Source: UCLA/WIN center
Discussion