Enabling IA SoCs with Intel’s Technology and Manufacturing Innovation

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Shared SoC Design & Manufacturing Technology Layers

MID

EMBEDDED

CE

SoC DESIGN TECHNOLOGY LAYER

PROCESS TECHNOLOGY & MANUFACTURING LAYER
Shared Process & Manufacturing Technology Layer

PROCESS TECHNOLOGY & MANUFACTURING LAYER
Silicon Process Technology Advantage
Faster Transistors and Improved Power at 32nm

INTEL 32nm SoC TECHNOLOGY EXTENDS THE REACH OF IA

LEAKAGE REDUCTION
3 ORDERS OF MAGNITUDE

TRANSISTOR PERFORMANCE
The Enabler

Intel’s Hi-K/Metal Gate Transistor Technology

45nm: IN PRODUCTION SINCE 2H’07

32nm: ON TRACK FOR 2\textsuperscript{nd} GEN RAMP IN 2H’09. HIGHEST DRIVE CURRENT AND SMALLEST GATE PITCH OF ANY REPORTED 32nm/28nm TECHNOLOGY
VARIETY OF OPTIONS TO ENABLE OPTIMIZED SILICON INTEGRATION OF DIVERSE SYSTEM COMPONENTS
Intel 32nm Package Options
Enabling SOC Optimization in Integration, Form Factor and Cost

- MCP FCBGA 2mm thick
- SINGLE DIE FCBGA 1.6mm thick
- DISCRETE FCMB <1 mm thick
- POP FCMB <0.8 mm thick
Intel’s Lead Free Package Technology

ALL OPTIONS ARE LEAD FREE FOR TECHNOLOGY NODES 45nm AND BELOW
INTEL’s 32nm SOC PROCESS DEVELOPMENT SHARES INVESTMENT AND LEARNING ON A COMMON PLATFORM WITH CPU PROCESS
### 32nm Silicon Shuttles

<table>
<thead>
<tr>
<th>SHUTTLE:</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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<td>Q307</td>
<td>Q208</td>
<td>Q308</td>
<td>Q109</td>
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<td>TECH FOCUS:</td>
<td>CPU TD</td>
<td>CPU Tech Cert</td>
<td>SOC TD</td>
<td>SOC Tech Cert</td>
<td>SOC Feature Refinements</td>
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<td>PROD FOCUS:</td>
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<td>Lead CPU Memory + Mixed-Signal IP</td>
<td>Lead SOC Memory IP</td>
<td>Lead SOC Memory + Mixed-Signal IP</td>
<td>Multi-Product Mixed Signal IP</td>
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UNFOLDING THE MAGIC OF 2\textsuperscript{nd} GEN 32nm TECHNOLOGY
Extending Decades of IDM Co-optimization to SOCs

- PROCESS
- PRODUCT
- DESIGN TOOLS
- MANUFACTURING
- MASKS
- PACKAGING

Co-optimized decisions from definition to ramp
Synchronized execution
Rapid yield learning & ramp
32nm Manufacturing Investment

D1D, Oregon [now]

F32, Arizona [2010]*

D1C, Oregon [Q409]*

F11x, New Mexico [2010*]

Intel News Release

Intel to Invest $7 Billion in U.S. Manufacturing Facilities
2-Year Plan to Focus on Leading-Edge Technologies

WASHINGTON, DC, Feb. 10, 2009 - Intel President and
A full, flowing, innovation pipeline

<22nm 2013+
22nm 2011
32nm 2009
45nm 2007
65nm 2005
90nm 2003

RESEARCH DEVELOPMENT MANUFACTURING

AND AS FAR AS WE CAN SEE... THE MAGIC CONTINUES

Future options subject to change
Shared SoC Technology Layer

SoC DESIGN TECHNOLOGY LAYER

PROCESS TECHNOLOGY & MANUFACTURING LAYER
Shared SoC Technology Layer

LEADERSHIP ATOM CORE

MODULAR SHARED IP LIBRARY

COMMON ARCH FRAMEWORK

COVERGED TOOLS & METHODOLOGIES

SoC DESIGN TECHNOLOGY LAYER

BENEFITS: TTM; MODULARITY/FLEXIBILITY/CUSTOMIZATION; COST/POWER/PERF/SIZE
IA-based Common Architecture Framework

IA SOFTWARE COMPATIBILITY
MODULAR INTEGRATION
BRIDGE TO EXTERNAL ECOSYSTEM FABRIC
Intel SoC Products
Intel Smart SoC Products

EP80579
FULL FEATURE SoC
ACCELERATORS
QUICK ASSIST TECH

LINCOLFT
45nm; ATOM CORE
CPU/GFX/MEH/DISPLAY
ADV. PWR MGMT

CE 3100
15 UNIQUE IP PIECES
AUDIO-VIDEO DECODE
GRAPHICS
DISPLAY PROCESSING

SODAVILLE
45nm; ATOM CORE
SEGMENT OPTIMIZED

FOURTEEN 32nm SoCs
IN PROGRESS*

*Future options subject to change
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This document contains information on products in the design phase of development.

45nm product is manufactured on a lead-free process. Lead is below 1000 PPM per EU RoHS directive (2002/95/EC, Annex A). Some EU RoHS exemptions for lead may apply to other components used in the product package.

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