Enabling New Ultra Portable Form Factors through Multi-Radio Integration

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Agenda

CSLL Vision

*Carry Small* Device Implications

Multi-radio Integration Needs

Digital CMOS Transceiver Innovations
Carry Small
A Vision of tomorrow’s mobile device:

- Carry only Essential Computational Resources
- Platform-wide Power Efficiency
- Anytime, Anywhere Collaboration with the Internet
- Sensor-based to understand the world around you
Carry Small:
Make Mobile Devices More Mobile!

More Performance
Increased Battery Life
More Connectivity Options
Better Graphics
Better Web Page Compatibility
Carry Small: More Form Factor Friendly

- Smaller Silicon Footprint
- Less Power Consumption
- Lower Cost
- Fewer Connectors
- Less Complexity

Today

Future

Required to deliver the Carry Small Vision
Live Large: Better Experience
That knows No Bounds...
• Delivers amplified, more robust mobile experience
  • Seamless access to new Devices, Networks and Services
  • Understands & Anticipates what you want to do
Carry Small: More Form Factor Friendly!

• Increasing Mobility needs
• Decreasing Form Factor Size

Need Technology Breakthroughs in:
• Architecture
• CMOS Process
• Radio Design

Big Opportunity with Serious Challenges

32 nm and Beyond!
Multi-radio Research Domain

- Tunable Front End Modules / Antenna
- Digitally Enhanced Radio RFIC
- Scalable Communication Core - PHY/MAC
- Radio Platform SoC RFI Mitigation
- Energy Efficient Communications
- Seamless connectivity
- Standards 802.11r, 802.11v, 802.16m, IETF
Integrate Multi-radio CMOS Transceiver with flexible baseband processor & multi-MAC

Requires technology breakthroughs in radio design
Digitally Enhanced Radio (DER) Architecture

Digitally Enhanced Radio

- Simplified analog receiver
- Sigma delta ADC
- Digital synthesizer
- Digital transmitter, Switching PA

Increased digital content → Cost reduction + Better platform integration
Motivation for High Performance ADC

- Scaled CMOS
- Lower Supply
- Simplify Analog Baseband
- Digital Programmability
- Multi-standard Receiver

Low Noise, High Linearity ΔΣ ADC Required!
Motivation for High Performance ADC

- Low resolution FLASH ADC for spectrum sensing
- Simple Spectrum Analyzer for spectrum estimation and ADC mode selection
Spectrum Sensing Wi-Fi/WiMAX ADC
Power Efficient 802.11n Operation

12 bit ADC allows Analog to be replaced by Digital circuits

Senses interference from other radios in the same band. Adjusts for optimal Power & Performance

Optimal channel selection maximizes real-life throughput

Supports Wi-Fi/WiMAX bandwidths in a power efficient manner

Lowest power 802.11n ADC - First reconfigurable ADC for 802.11n and multi-radio applications
Motivation for Reconfigurable ADC
Digitally Enhanced Radio Robustness

Adjacent Channels

Channel n

Channel n+1

Receiver Linearity Impacts performance
Digitally Enhanced Receiver Coexistence

Digital CMOS Receiver

- Mismatch Tuning
- Calibration Algorithm
- Baseband Processing

Differential LNA

Differential Amplifier

Goal: Digital calibration method to suppress interference due to 2nd order non-linearity
Digitally Enhanced Receiver Coexistence on IP2

China Beijing Lab’s Research improves Rx noise suppression at reduced calibration cost
Power amplifier is used to communicate from user device to base station
First power amplifier in 65nm CMOS (28.6dBm power output)

**Power amplifier innovation:**
- Delivers close to 1 Watt power for wide coverage
- Uses novel technique to introduce complex modulation required for high data rates
- Implemented in digital 65nm CMOS process for easy integration with digital processor (low cost)

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<th>Range &amp; Output Power</th>
<th>Data Rate &amp; Modulation Complexity</th>
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<tbody>
<tr>
<td><strong>Cellular</strong></td>
<td>HIGH</td>
<td>Small</td>
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<tr>
<td><strong>Wi-Fi</strong></td>
<td>Small</td>
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<td><strong>WiMAX</strong></td>
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60GHz presents opportunity for high throughput WPAN standard
First ever mm-wave CMOS synthesizer with <3kHz frequency resolution
Millimeter-wave CMOS Technology for Multi-Gb/s Wireless Communication

- Several GHz bandwidth available around 60GHz
- > 2GHz channel $\rightarrow$ > 5Gb/s data-rate
  - Download a full-HD movie in < 1 minute (compared to 1.5 hours for legacy WLAN)
- Frequency synthesizer is used for channel selection
- Fundamental building block required in CMOS for integrated mm wave radios
- Reduces size and improves yield with built in calibration
- Multi-Gb/s data-rate for (WPAN, wireless-HD etc)
Intel CMOS Xcvr Prototype
Multi-Band CMOS Transceiver with Integrated FE
90nm 802.11agn WLAN 1x2 MIMO

Power efficient dual band TX with full power on chip class AB PAs + Digital Pre-distortion
Advanced Digital-Pre-Distortion Calibration for excellent performance and system stability
Dual band (2.4G and 5 ÷ 6G) LNA integration
Full dual band FE integration enables low cost and high performance, enabling small form factor.

Excellent performance with on-chip PAs and advanced pre-distortion calibration.

Multi-Band CMOS Transceiver with Integrated FE
90nm 802.11agn WLAN 1x2 MIMO
Future Research Directions

Integrate Flexible Baseband processor & digital CMOS transceiver

Integrate remaining platform components for integrated multi-radio SoC solution
Summary

Intel is enabling ultra portable devices with new capabilities supporting new usage models.

Aggressive multi-radio integration with platform components necessary.

Technology breakthrough in multi-standard CMOS transceiver architecture is key step in multi-radio platform integration.
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