BOB BAKER
Senior Vice President
General Manager,
Technology and Manufacturing Group
Silicon Leadership:
Delivering Innovation

Relentless Pursuit of Moore’s Law

Innovations in Silicon Technology

Extending Leadership for New Opportunities
As the number of transistors goes UP, Price per transistor goes DOWN.

Moore's Law Still Drives Intel
If gas mileage improved as fast as CPU Mips/Watt, we’d have cars today with ~100,000 mpg.
The Fundamental Driver of Cost and Innovation

**Cost Reduction**
Same circuitry half the space

**OR**

**Architectural Innovation**
Twice the circuitry in the same space

= Option to design for optimal performance/cost

Source: Intel
45 nm Products Across the Board

Revolutionary high-k + metal gate transistors
>200 million units shipped
Innovation-Enabled Technology Pipeline:
Researchers are Moving on to Investigation of Novel Technology Options

Future options subject to change.
The New Era of Scaling

Modern CMOS scaling is as much about material innovation as dimensional scaling.
Professor Jesus del Alamo
Professor of Electrical Engineering
Donner Professor, MacVicar Faculty Fellow
Department of Electrical Engineering
and Computer Science
Massachusetts Institute of Technology
Continuing Moore’s Law

Scaling Enables Lower Cost and Higher Capability

Opportunities to Extend Moore’s Law

Researchers Doing Innovative Work
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On-Time 2 Year Cycles

- 130 nm  (2001)
- 90 nm   (2003)
- 65 nm   (2005)
- 45 nm   (2007)
- 32 nm   (2009)
- 22 nm   (2011)  [Projected]
- 15 nm   (2013)  [Projected]
32nm - Extending Technology Leadership

Industry-leading features:
- 2nd generation high-k/metal gate transistors
- 4th generation strained silicon
- Highest reported drive currents
- 0.7x pitch scaling enables 50% area reduction

First to demonstrate working 32nm processors

Intel’s 32 nm process is certified for production

291 Mbit SRAM >1.9 billion transistors
0.171 um2 cell size 3.8 GHz operation
32 nm Westmere Microprocessor in Production

CPU wafers are moving through the factory in support of planned Q4 revenue production.
32nm Manufacturing Fabs:
$7B Investment Over 2 Years

D1D
Oregon

Fab 32
Arizona

D1C
Oregon

Fab 11X
New Mexico
The World’s First 22 nm SRAM
The World’s First 22 nm SRAM

- 364 Mbit array size
- >2.9 billion transistors
- 3rd generation high-k + metal gate transistors
- Same transistor and interconnect features as on 22 nm CPUs

Demonstrating working 22 nm SRAMs is an important milestone towards building working 22 nm microprocessors.
22 nm Optimized for Wide Range of Applications

High density
0.092 \text{um}^2 \text{ SRAM cell}

Low voltage
0.108 \text{um}^2 \text{ SRAM cell}

0.092 \text{um}^2 \text{ is the smallest SRAM cell in working circuits reported to date}
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- Extending Leadership for New Opportunities
New Segment Opportunities: Internet Connected Devices

- CE
- Embedded
- Handhelds

New segments require new technology and manufacturing capabilities.

Source: Intel
Initial 45 nm Intel® processor based SoC products

Source: Intel
Integrated Device Manufacturer Advantage

- Design for Manufacturing
- Co-Optimized Process + Product
- Rapid Yield Learning
- Early Product Ramp

Process
Product
Design Tools
Manufacturing
Masks
Packaging
Expanded Support for New Opportunities

Customer Support

SoCs

Software

Process

Product

Memory

Design Tools

Manufacturing

Platforms

Packaging

Masks

Core 2 Extreme quad-core
SoC Process Builds on CPU Process

- **45nm**
  - 2007: P1266
  - 2008: P1266.8
  - Products: CPU, SoC

- **32nm**
  - 2009: P1268
  - 2010: P1269
  - Products: CPU, SoC

- **22nm**
  - 2011: P1270
  - 2012: P1271
  - Products: CPU, SoC

CPU and SoC versions of each process generation to provide transistors, interconnects and other device features optimized for each product line.

Source: Intel
32nm SOC Full-Featured Process Menu

Variety of Options to Enable Optimized Silicon Integration of Diverse System Components
SoC Design and Manufacturing Tools
Benefits: Time to Market, Modularity, Flexibility, Customization

LEADERSHIP DFx TOOLS

MODULAR SHARED IP LIBRARY
Internal or Customer

COMMON ARCH FRAMEWORK

CONVERGED TOOLS AND METHODOLOGIES

SoC DESIGN TECHNOLOGY LAYER

Source: Intel
Intel 32nm Package Options:
Enabling SOC Optimization in Integration, Form Factor and Cost

- MCP FCBGA
  2mm thick

- SINGLE DIE FCBGA
  1.6mm thick

- DISCRETE FCMB
  <1 mm thick

- POP FCMB
  <0.8 mm thick

IDF2009
INTEL DEVELOPER FORUM
Faster Factories Enable Improved Customer Response

Faster Factories

Better Commitment

Quicker Order to Delivery

Cycle Time Reduction: 62%

Cycle Time Days

2006 2007 2008 2009

IDF2009
INTEL DEVELOPER FORUM
Faster Factories Enable Improved Customer Response

Faster Factories  Better Commitment  Quicker Order to Delivery

3X INCREASE IN YES IN ONE DAY

2007  2008  2009
Faster Factories Enable Improved Customer Response

25% IMPROVEMENT IN LESS THAN A YEAR

Faster Factories  Better Commitment  Quicker Order to Delivery

July  2008  December  January  2009  May
NAND Scaling: Extending the Possibilities
Rick Coulson
Intel Senior Fellow
Director, Storage Technologies
Technology and Manufacturing Group
Platform Co-Optimizations with SSDs

SSDs benefit existing platforms

Storage subsystems lag

Co-optimizing SSDs and platform

Improves performance, scalability, power efficiency, total cost
In Closing...

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