A 32nm Logic Technology Featuring 2nd-Generation High-k + Metal-Gate Transistors, Enhanced Channel Strain and 0.171um² SRAM Cell Size in a 291Mb Array


Logic Technology Development, *QRE, ** TCAD
Intel Corporation
Outline

• Process Features
• Transistors
• Interconnects
• Circuits
• Conclusions
Process Features

- 32nm Groundrules
- 193nm Immersion Lithography
- 2nd Generation High-K + Metal Gate
- 4th Generation Strained Silicon
- 9 Cu Interconnect Layers
  - Low-k CDO / SiCN dielectric
- Cu bump with Lead-free Packaging
# 32nm Design Rules

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch (nm)</th>
<th>Thick (nm)</th>
<th>Aspect Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation</td>
<td>140.0</td>
<td>200</td>
<td>--</td>
</tr>
<tr>
<td>Contacted Gate</td>
<td>112.5</td>
<td>35</td>
<td>--</td>
</tr>
<tr>
<td>Metal 1</td>
<td>112.5</td>
<td>95</td>
<td>1.7</td>
</tr>
<tr>
<td>Metal 2</td>
<td>112.5</td>
<td>95</td>
<td>1.7</td>
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<tr>
<td>Metal 3</td>
<td>112.5</td>
<td>95</td>
<td>1.7</td>
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<tr>
<td>Metal 4</td>
<td>168.8</td>
<td>151</td>
<td>1.8</td>
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<tr>
<td>Metal 5</td>
<td>225.0</td>
<td>204</td>
<td>1.8</td>
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<tr>
<td>Metal 6</td>
<td>337.6</td>
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<td>1.8</td>
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<td>Metal 7</td>
<td>450.1</td>
<td>388</td>
<td>1.7</td>
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<tr>
<td>Metal 8</td>
<td>566.5</td>
<td>504</td>
<td>1.8</td>
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<tr>
<td>Metal 9</td>
<td>19.4um</td>
<td>8um</td>
<td>1.5</td>
</tr>
</tbody>
</table>

~0.7x linear scaling from 45nm
Contacted Gate Pitch

- Transistor gate pitch of 112.5nm
- Continues 0.7x per generation scaling

Tightest contacted gate pitch reported for 32nm generation
**SRAM Cells**

- **0.171 \( \text{um}^2 \) SRAM cell**

Transistor density doubles every two years.
SRAM Array Density

- SRAM array density achieves 4.2 Mb/mm²
  - Includes row/column drivers and other circuitry

Array density scales at ~2X per generation
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Key Transistor Features

• 30nm gate length with 112.5nm contacted gate pitch

• 2\textsuperscript{nd} generation Hi-k + Metal Gate
  – 0.9nm EOT Hi-K with dual workfunction metal gate electrodes
  – Continued use of Replacement Metal Gate approach
    • Metal gate deposition after high temperature anneals
    • Integrated with strained silicon process
  – Transistor mask count same as 45nm
  – Adds \(~4\%\) process cost over non hi-k/MG

• 4\textsuperscript{th} generation of strained silicon
Device Characteristics

Excellent Vt roll-off and DIBL
Well controlled short channel effects
Subthreshold slope $\sim 100$ mV/decade
NMOS $I_{DSAT}$ vs. $I_{OFF}$

$V_{dd}=1.0\text{V}$

$I_{off}$ (nA/μm)

$I_{dsat}$ (mA/μm)

1.55 mA/μm at $I_{OFF} = 100$ nA/μm

14% better than 45nm

45nm: Mistry, 2007 IEDM

112.5 nm
PMOS $|I_{DSAT}|$ vs. $I_{OFF}$

Vdd=1.0V

45nm: Mistry, 2007 IEDM

$1.31 \text{ mA/\mu m at } I_{OFF} = 100 \text{ nA/\mu m}$

22% better than 45nm

32nm PMOS $I_{DSAT}$ almost equal to 45nm NMOS $I_{DSAT}$!
NMOS $I_{DLIN}$ vs. $I_{OFF}$

$V_{dd} = 1.0V$
$V_{ds} = 0.05V$

$I_{DLIN}$ vs. $I_{OFF}$

0.228 mA/$\mu$m at $I_{OFF} = 100$ nA/$\mu$m
19% better than 45nm

45nm: Mistry, 2007 IEDM

112.5 nm
$V_{dd} = 1.0V$
$V_{ds} = 0.05V$

<table>
<thead>
<tr>
<th>$I_{ddlin}$</th>
<th>(mA/μm)</th>
<th>$I_{off}$</th>
<th>(nA/μm)</th>
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</thead>
<tbody>
<tr>
<td>0.228</td>
<td></td>
<td>100</td>
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</table>

28% better than 45nm

Average 20% NMOS/PMOS Sat/Lin drive current gain over 45nm
Transistor Performance vs. Gate Pitch

Highest reported drive current at tightest reported gate pitch
Simultaneous performance and density improvement

1.0V, 100 nA/μm
90nm: Mistry, 2004 VLSI
65nm: Tyagi, 2005 IEDM
45nm: Mistry, 2007 IEDM

IDSAT (mA/μm)

Contacted Gate Pitch (nm)

Gate Pitch (Generation) 320nm (90nm) 220nm (65nm) 160nm 112.5nm (32nm)

PMOS
NMOS

1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0

1000
100

0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6

15
Transistor Reliability - TDDB

32nm supports 10-15% higher E-field
Enables same voltage with lower EOT
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Interconnects

- Metal 1-3 pitches match transistor pitch
- Graduated upper level pitches optimize density & performance
- Extensive use of low-k ILD and SiCN
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32nm Shuttle

291 Mbit SRAM array
PROM array
High speed register file
High speed I/O circuits
High frequency
PLL/Clock

Discrete test structures

32nm shuttle with SRAM and key Logic circuits
Allows early co-optimization of process and design
SRAM Test Vehicle

- 291 Mb, 0.171um2 SRAM Cell
  - >1.9B transistors
  - First reported functional operation in Sep ‘07
- Process learning vehicle demonstrates
  - High yield
  - High performance
  - Stable low voltage operation

<table>
<thead>
<tr>
<th>Voltage (V)</th>
<th>Frequency (GHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.300V</td>
<td>3.80</td>
</tr>
<tr>
<td>1.250V</td>
<td>3.33</td>
</tr>
<tr>
<td>1.200V</td>
<td>3.06</td>
</tr>
<tr>
<td>1.150V</td>
<td>2.66</td>
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<tr>
<td>1.100V</td>
<td>2.29</td>
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<tr>
<td>1.050V</td>
<td>2.00</td>
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<tr>
<td>1.000V</td>
<td>1.72</td>
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<tr>
<td>0.950V</td>
<td>1.44</td>
</tr>
<tr>
<td>0.925V</td>
<td>1.29</td>
</tr>
</tbody>
</table>

2GHz  2.29GHz  2.66GHz  3.2GHz  4GHz  5.33GHz
SRAM $V_{\text{min}}$

$V_{\text{min}}$ distribution for 3.25Mb sub-arrays
Healthy 770mV median $V_{\text{min}}$
SRAM Yield

32nm SRAM yield maintains 2-year cadence
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Conclusions

• An industry leading 32nm logic technology is presented
• Continues Moore’s law relative to 45nm:
  – 0.7x contacted gate pitch scaling
  – 0.5x SRAM cell size scaling
  – 2.2x array density scaling
• Record linear and saturated transistor drive currents achieved
  – Average of 20% improvement in drive current over 45nm
• Healthy yield achieved on 291Mb SRAM with 0.171 \( \mu \text{m}^2 \) SRAM cell size and excellent low voltage operation
• Completed development phase on 32nm CMOS
  – On track for production readiness in H2’09
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  - Logic Technology Development
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  - Assembly & Test Technology Development
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