The Architecture for Discovery in a Parallel Universe

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General Manager, Datacenter & Connected Systems Group
Uncharted Territory on Path to Discovery
In Science and Engineering
HPC: Not an Optional Investment

To Compete You Must Compute.
To Compute.. 
You Must Have The 
RIGHT ARCHITECTURE
IT’S THE LAW.. 

“The speedup of a program using Multiple processors in parallel computing is limited by the sequential fraction of the program.”

Gene Amdahl
Xeon: Most Commonly Used Parallel Processor

Parallel, Fast Serial
Multicore + Vector
2X Cadence Through Haswell Leadership Today and Tomorrow

Parallel Features From Intel® Xeon® E5 Processors Make It Ideal For Most HPC Applications

* Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (1 Intel® Xeon® faster)
Application Algorithms Improvement
Increasing The Number Of
HIGHLY PARALLEL APPLICATIONS

* Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (Intel® Xeon® faster)
Highly Parallel Applications and Processors

Optimized for Highly Parallel Many Core
Wider SIMD16 Vector instructions
Up to 8X increase in Theoretical Performance
Designed for Reliability In Large Systems

It’s the Highly Vectorizable Applications that Benefit from Highly Parallel Architecture

* Theoretical acceleration of a highly parallel processor over a Intel® Xeon® parallel processor (<1 Intel® Xeon® faster)
Programming on CPU and Coprocessor

Unlike accelerators, optimizations for Intel® Xeon Phi™ and Intel® Xeon® products share the same languages, directives, libraries, and tools.

“Unmatched Productivity”

OpenMP* TR
Open, Standard, Supports Diverse Hardware
Intel will support the OpenMP TR for targeting extensions in January 2013!

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Introducing the Intel® Xeon Phi™ Coprocessor Family
Intel® Xeon Phi™ Coprocessor 3100 Family

Outstanding Parallel Computing Solution

Available first half of 2013
>1000 Gigaflops DP (peak)
6GB GDDR5 memory at 240 GB/s
Active and Passive form factors at 300W TDP
Less than $2,000

Intel® Xeon Phi™ Coprocessor 5100 Family

Highly Parallel Computing Solution that is Optimized for High Density Environments

General Availability Jan 28 2013
Up to 1010 Gigaflop DP (peak)
8GB GDDR5 memory at 320 GB/s
Passive form factor at 225W TDP
$2,649 RCP
Myth busting – >100x Improvement in Performance

Intel® Xeon Running Serial Code

Intel® Xeon Phi™ Parallelized Code

PARALLEL CODE

!SOMP PARALLEL do PRIVATE(j,k)
do i = 1, 20
offset = i*128
do j = 1, 5000000
!dir$ vector aligned
do k = 1, 128
fa(k+offset) = a * fa(k+offset) + fb(k+offset)
end do
end do
end do

67.097 SECONDS

0.197 SECONDS 340X?
Same Code Improves Xeon Performance!

Intel® Xeon Running Serial Code
- **Intel® Xeon**
- Serial Code
- **67.097 SECONDS**

Intel® Xeon Parallelized Code
- **Intel® Xeon**
- Parallelized Code
- **0.46 SECONDS**
- **145X FASTER**

Intel® Xeon Phi™ Parallelized Code
- **Intel® Xeon Phi™**
- Parallelized Code
- **0.197 SECONDS**
- **2.3X! FASTER**

PARALLEL CODE

```plaintext
!SOMP PARALLEL do PRIVATE(j,k)
do i = 1, 20
  offset = i*128
  do j = 1, 5000000
    !dir$ vector aligned
do k = 1, 128
  fa(k+offset) = a * fa(k+offset) + fb(k+offset)
  end do
end do
end do
```
Synthetic Benchmark (Intel® MKL)
Measured on the TACC+ Stampede Cluster

Notes
1. Intel® Xeon® Processor E5-2680 used for all SGEMM Matrix = 12800 x 12800, DGEMM Matrix = 10752 x 10752, SMP Linpack Matrix 26000 x 26000
2. Intel® Xeon Phi™ coprocessor SE10P (ECC on) with “Gold” SW stack SGEMM Matrix = 12800 x 12800, DGEMM Matrix = 12800 x 12800, SMP Linpack Matrix 28672 x 28672
3. Average single-node results from measurements across a set of nodes from the TACC+ Stampede Cluster
+ Texas Advanced Computing Center (TACC) at the University of Texas at Austin.

Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products.

Source: Intel Measured on TACC cluster results as of October 25, 2012   Configuration Details: Please reference slide speaker notes.

For more information go to http://www.intel.com/performance
Application Performance: Intel® Xeon Phi™ Coprocessor

**Finite Element Analysis**
- SANDIA NATIONAL LABS MiniFE
  - **UP TO** 1.7X

**Embree Raytracing**
- INTEL LABS RAYTRACING
  - **SPEED-UP** 1.8X

**Seismic**
- ACCELEWARE 8TH ORDER ISOTROPIC VARIABLE VELOCITY
  - **UP TO** 2.05X

**Molecular Dynamics**
- LOS ALAMOS MOLECULAR DYNAMICS
  - **UP TO** 2.52X

**Physics**
- JEFFERSON LAB LATTICE QCD
  - **UP TO** 2.7X

**Finance**
- BLACKSCHOLES SP
  - **UP TO** 7X
- Monte Carlo SP
  - **UP TO** 10.75X

* Xeon = Intel® Xeon® processor;
* Xeon Phi = Intel® Xeon Phi™ coprocessor

Notes:
1. 2S Intel® Xeon® processor X5690 vs. 2S Intel® Xeon® + 1 Intel® Xeon Phi™ coprocessor (pre production HW/SW)
2. 2S Intel® Xeon® processor E5-2687 vs. 1 Intel® Xeon Phi™ coprocessor (preproduction HW/SW) (960 versions of improved workload)
3. 2S Intel® Xeon® processor E5-2680 vs. 1 Intel® Xeon Phi™ coprocessor (preproduction HW/SW)
4. 4 node cluster, each node with 2S Intel® Xeon® processor E5-2867 (comparison is cluster performance with and without 1 pre-production Intel® Xeon Phi™ coprocessor per node)
5. Includes additional FLOPS from transcendental function unit

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Source: Intel Measured results as of October 17, 2012   Configuration Details: Please reference slide speaker notes.

For more information go to http://www.intel.com/performance
Discovery and Innovation

Efficiency
Streamline bringing New Ideas to light

Programmability to Enable Scientific Discovery

Source: Intel Discovery Cluster Linpack benchmark run, June 2012
Welcome!

Bob Galush
Vice President, System x IBM

Dr. Daniel Duffy
Lead Systems Engineer
NASA Center for Climate Simulation (NCCS)
NASA Goddard Space Flight Center (GSFC)
Welcome!

Paul Santeler
VP & GM, Hyperscale Business Unit / ISS
Hewlett Packard Company

Lincoln Wallen
Chief Technology Officer
DreamWorks Animation

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Welcome!

Brian Payne
Executive Director, PowerEdge Server Marketing
Dell Inc.

Jay Boisseau, Ph.D
Director
Texas Advanced Computing Center
Developing Today on Intel® Xeon Phi™ Coprocessors

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Top 500 Highlights

Intel® Xeon® processor:
• 379 systems
• 91% of new listings
• Intel® Xeon® processor 2600 family
  Fastest growing CPU on list

Intel® Xeon Phi™ coprocessor:
• 7 systems listed!
• 2.6 Petaflops #7 TACC Stampede
• Outstanding efficiency up to 75%
• ...and...

Other brands and names are the property of their respective owners.
Source: www.top500.org
WORLD RECORD!

"Beacon" at NICS

Intel® Xeon® + Intel Xeon Phi™ Cluster
Most Power Efficient on the List
2.449 GigaFLOPS / Watt
70.1% efficiency

Source: www.top500.org
Two new Intel® Xeon Phi™ coprocessor families provide:

Performance and Performance/Watt
For highly parallel HPC workloads with cores, threads, wide-simd, caches, memory BW

While maintaining the advantages of Intel Architecture
General purpose programming environment advanced power management technology

First products shipping now
General availability January 2013
Parallelism is Your Path to the Future

Intel is more than ever.. Your Roadmap
Risk Factors

The above statements and any others in this document that refer to plans and expectations for the fourth quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel's actual results, and variances from Intel's current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be the important factors that could cause actual results to differ materially from the company's expectations. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions, including supply constraints and other disruptions affecting customers; customer acceptance of Intel's and competitors' products; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Uncertainty in global economic and financial conditions poses a risk that consumers and businesses may defer purchases in response to negative financial events, which could negatively affect product demand and other related matters. Intel operates in intensely competitive industries that are characterized by a high percentage of costs that are fixed or difficult to reduce in the short term and product demand that is highly variable and difficult to forecast. Revenue and the gross margin percentage are affected by the timing of Intel product introductions and the demand for and market acceptance of Intel's products; actions taken by Intel's competitors, including product offerings and introductions, marketing programs and pricing pressures and Intel's response to such actions; and Intel's ability to respond quickly to technological developments and to incorporate new features into its products. The gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; start-up costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; product manufacturing quality/yields; and impairments of long-lived assets, including manufacturing, assembly/test and intangible assets. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Expenses, particularly certain marketing and compensation expenses, as well as restructuring and asset impairment charges, vary depending on the level of demand for Intel's products and the level of revenue and profits. Intel's results could be affected by the timing of closing of acquisitions and dispositions. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues, such as the litigation and regulatory matters described in Intel's SEC reports. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel's ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel's results is included in Intel's SEC filings, including the company's most recent Form 10-Q, Form 10-K and earnings release.
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