Enabling Breakthroughs In Technology

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Enabling a Steady Technology Cadence

TECHNOLOGY GENERATION

MANUFACTURING

65nm 2005
45nm 2007
32nm 2009
22nm 2011
14nm 2013
10nm 2015
7nm 2017
Beyond 2020

DEVELOPMENT

2009
2011
2013
2015
2017

RESEARCH

What to do now to enable these future generations?

Defined

To be defined

Not to scale
But first
some old technology ...
Transistor Innovations Enable Technology Cadence

- 2003: 90 nm, Invented SiGe Strained Silicon
- 2005: 65 nm, 2nd Gen. SiGe Strained Silicon
- 2007: 45 nm, Invented Gate-Last High-k Metal Gate
- 2009: 32 nm, 2nd Gen. Gate-Last High-k Metal Gate
- 2011: 22 nm, First to Implement Tri-Gate

Strained Silicon
High k Metal gate
Tri-Gate

Tri-Gate Invented
- Single-fin transistor demonstrated 2002
- Multi-fin transistor demonstrated 2003
- Tri-gate SRAM cells demonstrated 2006
- Tri-gate RMG process flow developed 2007

Tri-Gate Selected for 22nm node

Tri-Gate Mfg
- Tri-gate optimized for HVM
Exploration - late 90’s
• Talk of 0.1um as the end due to leakage power
• 248nm lithography limited device exploration

Then enabled
• Creation of sub-resolution features
• Study of dense patterns (later)

1997 Intel Invention
Spacer based pattern

10.00 nm
Intel: 10nm planar transistor

Exploration was not limited by lithography
Exploration - late 90’s
• Talk of 0.1um as the end due to leakage power
• 248nm lithography limited device exploration

Exploration today
193 immersion lithography
+ Spacer based pattern twice

1997 Intel Invention
Spacer based pattern

Exploration (still) not limited by lithography
Evaluation – early 00’s
- 15 yrs discussion of possible non-planar device concepts
- No systematic scaling studies

Then enabled
- Assessment of scaling challenges and critical parameters
- Focus for optimization

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<tr>
<th>Planar</th>
<th>Thin body SOI</th>
<th>FinFET on SOI</th>
<th>Trigate on SOI</th>
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<tbody>
<tr>
<td><img src="image1.png" alt="Planar Diagram" /></td>
<td><img src="image2.png" alt="Thin body SOI Diagram" /></td>
<td><img src="image3.png" alt="FinFET on SOI Diagram" /></td>
<td><img src="image4.png" alt="Trigate on SOI Diagram" /></td>
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Build all variations and compare
Evaluation - early 00’s
• 15 yrs discussion of possible non-planar device concepts
• No systematic scaling studies

Evaluation today
• Assessment of scaling challenges and critical parameters for III-V

Thin body SOI

FinFET on SOI

Trigate on SOI

Quantum Well equivalent to Thin body SOI

3D devices

InGaAs
Integration - mid 00’s
- Move to bulk silicon (cost)
- Catch up to planar for high k/metal gate + strain
- Create working CMOS

Then enabled
- Quality decision to adopt
- Development roadmap
- Lots more work !!!!

2006
Tri-gate SRAM cells demonstrated

2007
Tri-gate RMG process flow developed
Integration - mid 00’s
- Move to bulk silicon (cost)
- Catch up to planar for high k/metal gate + strain
- Create working CMOS

Integration Today
- III-V grown on bulk silicon
- High k integration done
- Strain engineering - not needed
- 3D devices – partially done
- N and P on same wafer – NOT DONE

Tri-gate SRAM cells demonstrated
Tri-gate RMG process flow developed
Optimizing Choices for Transistors on Multiple Fronts

Increasing MOBILITY (better ON)

- Strain
- Ge

Increasing COUPLING (better OFF)

- Planar With High K
- UTB SOI (or QW)
- Fins
- Wires/Dots

Graphene

CNT

Intel
Optimizing Choices for Transistors on Multiple Fronts

Increasing MOBILITY (better ON)

Increasing COUPLING (better OFF)

UTB SOI (or QW)

Fins

Wires/Dots

Graphene

CNT

Strain

Ge

III-V

Now

Source n-Ge Drain

i₃Ga₅As contact
InP etch stop
In₃Al₅As top barrier
Si N-doped layer
In₃Ga₅As channel
In₃Al₅As bottom barrier
In₄Al₅As graded buffer
GaAs buffer
4°(100) offcut Si substrate
Interconnects Need to Scale

Needed Focus

- Thin conformal plateable barrier
  ... or self forming barrier
- Tall vias might use non-Cu
- Non-SiO2 dielectrics
- Exotic long interconnects: CNT (10’s um), optical (>mm)
- 3D stacking
Broad Range of Options

**STRUCTURE**
- Relay (Liu IEDM 2010)
- TFET (M. Luisier, Purdue, EDL 2009)

**MOBILITY**
- III-V
- Ge
- Strain
- 32nm

**INTEGRATION**
- System-in-package
- System-on-chip

**COUPLING**
- UTB SOI
- Fins
- Wires/Dots
We Expect Technology Innovation to Continue

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*projected

- III-V Materials Synthesis
- Optical Interconnect
- Computational Lithography
- Interconnects
- High-K Germanium Dense Memory
- Nanowires
Conclusions

- Moore’s Law is not a law of nature, it is an expectation of continued innovation

- We expect to continue through focused research, rapid development, investment in production

- Scaling research is increasingly about materials research, solving problems brings opportunities

- New product opportunities will arise from continued advances in integration, connectivity