Intel Labs ISSCC 2012 Highlights

1. **Efficient Computing Research:** Making the most of every milliwatt to make computing greener and more scalable across the Continuum
   - 5-10x efficiency gains by enabling low or near-threshold voltage (NTV) operation
   - Applying low voltage techniques broadly to compute, graphics, and memory circuits

2. **Digital Radio Research:** Simplifying radio architecture by approaching it as a computing problem rather than a circuit design problem
   - Enabling Moore’s Law for RF circuits through digital techniques
   - Tackling the last few barriers to make digital RF practical for SoC integration

3. **High-Efficiency Math:** Reducing power while guaranteeing the accuracy of numeric computations with “right-sized” floating point arithmetic
   - Revolutionary approach to attack floating point challenges at the architecture level
Investing in Near Threshold Voltage

- Peak energy efficiencies at NTV
- Greater dynamic operating range
- Ideal for variable workloads and highly parallel applications
- Applicable from deeply embedded to exascale computing

**Threshold**: Voltage at which transistors begin to conduct electricity (turn on)
Near Threshold Voltage Processor
(3.6) A 280mV-to-1.2V Wide-Operating-Range IA-32 Processor in 32nm CMOS

- Claremont: low-power IA concept processor
  - Initially demoed at Fall IDF 2011
- First processor to demonstrate the benefits of (NTV) circuits for compute
- New for ISSCC
  - Overview of chip layout, design methodology, etc.
  - Built in low-leakage 32nm SoC technology
  - Operates from 280mV @3MHz to 1.2V @915MHz
  - 4.7x better energy efficiency in NTV mode
  - 2mW minimum power

Core demonstrated running Windows and Linux powered by this solar cell
Lowering the Operating Voltage for Memory

(13.3) Capacitive-Coupling Wordline Boosting with Self-Induced VCC Collapse for Write $V_{\text{min}}$ Reduction in 22-nm 8T SRAM

- Demonstrates voltage scaling for medium or large memory arrays with minimal area or capacitance impact
- Allows 80-140mV $V_{\text{min}}$ reduction for a 1MB memory array by boosting voltage on sensitive writes
- Typically requires a costly charge pump circuit for a local voltage increase
- Eliminates need for charge pump via clever and novel use of intrinsic capacitances
NTV SIMD Engine for Processor Graphics

(10.1) A 280mV-to-1.1V 256b Reconfigurable SIMD Vector Permutation Engine With 2-Dimensional Shuffle in 22nm CMOS

- First demonstration of NTV on 22nm Tri-Gate technology
- Shows NTV viability for both compute and memory on representative SIMD block: Vector Permutation Engine
- Dynamic voltage scaling down to 280mV: 9x efficiency gain

Winner ISSCC 2012 Distinguished Technical Paper Award
Conventional radio circuits are analog, struggle to keep up with CMOS scaling

Intel Labs investing in research to fully exploit computational nature of radio

Removing the final barriers to make digital RF practical for SoC integration

Bringing the benefits of Moore’s Law to RF circuits
Pure Digital RF Transmitter

(9.4) A 20dBm 2.4GHz Digital Outphasing Transmitter for WLAN Application in 32nm CMOS

- Switching power amplifier enables performance to improve with CMOS scaling
- 1\textsuperscript{st} demonstration of a digital phase modulator architecture delivering full WiFi bandwidth
- State-of-the-art power efficiency and designed to improve with further CMOS scaling
First Atom SoC with CMOS WiFi Radio

(3.4) 32nm x86 OS-Compliant PC On-Chip With Dual-Core Atom® Processor and RF WiFi Transceiver

- Rosepoint: First 32nm SoC with WiFi RF transceiver and two Atom cores on the same die
- Demonstrates effective mitigation of interference between the WiFi radio and IA cores, despite operation in similar frequency range
- Cross-corporate collaboration between Intel research, development, and manufacturing
Variable Precision Floating Point Unit

(10.3) A 1.45GHz 52-to-162GFLOPS/W Variable-Precision Floating-Point Fused Multiply-Add Unit With Certainty Tracking in 32nm CMOS

• 1st reported variable-precision floating point unit with accuracy tracking for multiply-add
• Today’s floating-point math wastes energy, time, and storage by using worst-case precision everywhere
• Using variable precision (24-bit → 12-bit → 6-bit) as needed can cut energy by 50%
• Uses NTV circuits for up to 7x further efficiency gain
Additional Intel Papers at ISSCC 2012

**Processor**
- A 22nm IA Multi-CPU and GPU System-on-Chip

**Low Power**
- A 2.05G Vertices/s 151mW Lighting Accelerator for 3D Graphics in 32nm CMOS
- A 4.6GHz 162Mb SRAM in 22nm CMOS With Integrated Active VMIN-Enhancing Assist Circuitry

**Digital Radio**
- A 32nm CMOS All-Digital Reconfigurable Fractional Freq. Divider for Multistandard SoC Radios

**Clock Generation**
- A Reconfigurable Distributed All-Digital Clock Generator Core in 22nm High-k Tri-Gate LP CMOS
- A TDC-Less ADPLL With 200-to-3200MHz Range for Mobile SoC Clocking in 22nm CMOS

**Sensing**
- Ratiometric BJT-Based Thermal Sensor in 32nm and 22nm Technologies
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