Advancing Moore’s Law on 2014!
Monday, August 11, 2014

Rani Borkar – Vice President, Platform Engineering Group
Rani leads the Product Development Group, and will present Intel’s 14nm product development vision as manifest in the Broadwell microarchitecture.

Mark Bohr – Intel Senior Fellow, Logic Technology Development
Mark directs process architecture, development and Integration for Intel’s advanced logic technologies, delivering staggering innovations in accord with Moore’s Law.

Stephan Jourdan – Intel Fellow, Platform Engineering Group
Formerly chief architect of Broadwell, Stephan currently directs the definition and architectural development of Intel’s SoCs for tablets and phones.
Risk Factors

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If we use any non-GAAP financial measures during the presentations, you will find on our website, intc.com, the required reconciliation to the most directly comparable GAAP financial measure.
A Multi-Year Journey

Rani Borkar
Vice President, Product Development Group

August 11, 2014
14nm and Broadwell Micro-architecture

Enabling A Broad Spectrum of Leadership Products
A Multi-Year Journey to Re-invent the Notebook

What the Market Saw...

2010
Unveils New 2010 Intel® Core™ Processor Family
Intel® Core™ Processor

2011
Category Introduction Drive To Thin
2nd Generation Intel® Core™ Processor

2012
Adding Touch
3rd Generation Intel® Core™ Processor

2013
Ultrabook™ & 2 in 1
4th Generation Intel® Core™ Processor
A Multi-Year Journey to Re-invent the Notebook

What Was Going On Under the Hood...

2010
Westmere 32nm
- ULV processors
- Turbo
- Integrated Gfx on Package
- Power Control Unit
- Power Gates
- Increased Parallelism & Hyper-Threading

2011
Sandy Bridge 32nm
- Integrated On-die Gfx
- More Aggressive Turbo
- Core/Gfx Power Balancing
- Platform Power Limits
- More efficient OoO Engine

2012
Ivy Bridge 22nm
- 22nm Tri-gate Transistor
- Improved Perf at Low V
- Configurable TDP
- Increased 3D Gfx Perf
- DirectX11 Support

2013
Haswell 22nm
- ULT Process Optimization
- 2X Battery life
- 20X Idle power reduction
- Chipset MCP Integration
- Low Latency Idle States
- New FIVR
- Increased Dynamic Operating Range

2014
Broadwell-Y 14nm

Intel® Core™ Processor Low Power Evolution
Coming Soon: Intel® Core™ M

- 14nm 2\textsuperscript{nd} Gen Tri-Gate Transistors
- TDP Reduction Enabling ≤ 9mm Fanless Designs
- System Optimized Dynamic Power & Thermal Management
- Reduction in SOC Idle Power & Increased Dynamic Operating Range
- 2\textsuperscript{nd} Gen FIVR & 3DL Technology
- Next Gen Broadwell Converged Core
- Next Gen Graphics/Media/Display
- Chipset: Lower Power, Voice Usages, Faster Storage

Delivering The Experience of Intel® Core™
In Fanless Form Factors
A Multi-Year Journey to Re-invent the Notebook

What the Users Will Experience...

Thickness: From 26mm to 7.2mm
TDP: 4X Reduction
Graphics: 7X Improvement
IA Core: 2X Improvement
½ the Battery Size & Double the Life

Intel® Core™ Processor

2010

Intel® Core™ M

2014
Outside-In System Design

Innovations Across the Stack

- Packaging & Form Factor Optimizations
- Efficient Power Delivery
- Platform Power/Thermal Mgt.
- SoC Power Reductions
- 14nm Process & Design Co-optimization
Outside-In System Design

Innovations Across the Stack

Enabled Board Area Reduction of ~25% Compared to Haswell with 50% Smaller Package

2nd Gen FIVR & 3DL for Increased Power Delivery Efficiency & Performance

Enhanced Turbo Boost, Increased Dynamic Operating Range & System Optimized Power/Thermal Management

Adopted Advanced Design Techniques for Aggressive Power Reduction

14nm Design/Process Optimizations Delivered 2X Lower Power than Traditional Scaling
Intel® Core™ M Processor Improvements

- Enables ≤9mm Fanless 2-in1's for the First Time on the Intel Core™ Roadmap
- Greater than 2X reduction in TDP with better performance vs. Haswell-Y
- 50% Smaller Package (XY), 30% Thinner
- 60% Lower SOC Idle Power for Increased Battery Life
14 nm Technology Announcement

Mark Bohr
Intel Senior Fellow
Logic Technology Development

August 11, 2014
Key Messages

- Intel’s 14 nm technology is now qualified and in volume production
- This technology uses 2nd generation Tri-gate (FinFET) transistors with industry-leading performance, power, density and cost per transistor
- The lead 14 nm product is a family of processors using the new Broadwell microarchitecture
- Intel’s 14 nm technology will be used to manufacture a wide range of products, from high performance to low power
## Minimum Feature Size

<table>
<thead>
<tr>
<th></th>
<th>22 nm Node</th>
<th>14 nm Node</th>
<th>Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistor Fin Pitch</td>
<td>60</td>
<td>42</td>
<td>.70x</td>
</tr>
<tr>
<td>Transistor Gate Pitch</td>
<td>90</td>
<td>70</td>
<td>.78x</td>
</tr>
<tr>
<td>Interconnect Pitch</td>
<td>80</td>
<td>52</td>
<td>.65x</td>
</tr>
</tbody>
</table>

*Intel Has Developed a True 14 nm Technology with Good Dimensional Scaling*
Transistor Fin Improvement

22 nm Process

60 nm pitch

34 nm height

Si Substrate

14 nm Process

Si Substrate
Transistor Fin Improvement

Tighter Fin Pitch for Improved Density

22 nm Process

14 nm Process
Transistor Fin Improvement

Current and Performance

Taller and Thinner Fins for Increased Drive Current and Performance
Transistor Fin Improvement

Reduced Number of Fins for Improved Density and Lower Capacitance
Transistor Fin Improvement

22 nm 1\(^{st}\) Generation Tri-gate Transistor

14 nm 2\(^{nd}\) Generation Tri-gate Transistor
Transistor Fin Improvement

22 nm 1st Generation Tri-gate Transistor

14 nm 2nd Generation Tri-gate Transistor
Interconnects

52 nm Interconnect Pitch Provides Better-than-normal Interconnect Scaling

22 nm Process

80 nm minimum pitch

14 nm Process

52 nm (0.65x) minimum pitch
SRAM Memory Cells

22 nm Process

.108 um²
(Used on CPU products)

14 nm Process

.0588 um²
(0.54x area scaling)

14 nm Design Rules + 2nd Generation Tri-gate Transistor Provides Industry-leading SRAM Density
Transistor Performance vs. Leakage

14 nm Transistors Provide Improved Performance and Leakage ...
Transistor Performance vs. Leakage

Lower Leakage Power
1x
0.1x
0.01x
0.001x
65 nm
45 nm
32 nm
22 nm
14 nm

Higher Transistor Performance (switching speed)

Server Computing
Client Computing
Mobile Computing
Mobile Always-On Circuits

... To Support a Wide Range of Products
New technology generations provide improved performance and/or reduced power, but the key benefit is improved performance per watt.
Product Benefits

14 nm BDW-Y delivers >2x improvement in performance per watt

- 2\textsuperscript{nd} generation Tri-gate transistors with improved low voltage performance and lower leakage
- Better than normal area scaling
- Extensive design-process co-optimization
- Micro-architecture optimizations for Cdyn reduction
Logic Area Scaling

Logic area continues to scale ~0.53x per generation
Logic Area Scaling

In the Past, Others Tended to Have Better Density, but Came Later Than Intel

Others based on published information:
45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
Logic Area Scaling

![Diagram showing logic area scaling with technology node and gate pitch data]

Intel Continues Scaling at 14 nm While Others Pause to Develop FinFETs

Others based on published information:
- 45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
- 28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
- 20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
- 16nm: S. Wu (TSMC), 2013 IEDM, p. 224
- 10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14
Intel is Shipping its 2nd Generation FinFETs Before Others Ship Their 1st Generation

Logic Area Scaling

Others based on published information:
45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14
Intel has Developed a True 14 nm Technology
Denser and Earlier Than What Others Call “16 nm” or “14 nm”

Logic Area Scaling

Others based on published information:
45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14
14 nm Achieves Better-than-Normal Area Scaling with Use of Advanced Double Patterning Techniques
Wafer Cost Increasing Due to Added Masking Steps
Intel 14 nm Continues to Deliver Lower Cost per Transistor
Leadership Technologies are Never Easy (at First!)

14 nm Broadwell SoC Yield Trend

- 14 nm product yield is now in healthy range with further improvements coming
- Process and lead product are qualified and in volume production
- 14 nm manufacturing fabs are located in Oregon (2014), Arizona (2014) and Ireland (2015)
- Production yield and wafer volume are projected to meet the needs of multiple 14 nm product ramps in 1H '15

22 nm data are shifted to align date of lead product qual
Depicts relative health, lines not to scale
Summary

Intel has developed a true 14 nm technology with industry-leading performance, power, density and cost per transistor

- 2\textsuperscript{nd} generation Tri-gate transistors
- 42 nm fin pitch
- 70 nm gate pitch
- 52 nm interconnect pitch
- 0.0588 μm\textsuperscript{2} SRAM cell

Intel’s 14 nm technology will be used to manufacture a wide range of products, from high performance to low power.

The 14 nm technology and the lead Broadwell SoC product are now qualified and in volume production.
Broadwell Microarchitecture Disclosures

Stephan Jourdan
Intel Fellow
Director, System-on-Chip Architecture
Platform Engineering Group

August 11, 2014
Agenda: Broadwell Micro-architecture

The Fanless Challenge
The Journey to Fanless
Broadwell Converged Core Improvements
Graphics/Media/Display
Delivering the Intel® Core™ Processor Experience in Fanless Form Factors

• Performance, Responsiveness, Battery Life, Ecosystem, etc.
• Embraced Outside-In Approach
The Fanless Challenge:
8-10mm, 10.1” Display, Fanless Designs Allow 3-5W Operations

SoC Sustainable Power Depends on:
1. Display Size (X and Y dimensions)
2. Chassis Z-height
3. Chassis material and target skin temp
4. Ambient temp

Metal chassis, $41^\circ C T_{\text{skin}}$, $25^\circ C T_{\text{Ambient}}$
The Fanless Challenge:
Delivering the Intel® Core™ Processor Experience in Fanless Form Factors

1. Maintaining Peak Burst Capability
2. Providing Power / Perf Efficiency

Normalized Performance

- Peak Performance Limited
- Thermal/Power Limited

- Target

- Bursty Workloads
- Light Sustained Workloads
- Heavy Sustained Workloads

Traditional Tablet
The Journey to Fanless:

- 14nm Process & Design Co-optimization
- Packaging and Form Factor Innovations
- 2nd Gen FIVR and 3DL Technology
- Enhanced Power Management
- Aggressive Power Reduction
The Journey to Fanless:

- 14nm Process & Design Co-optimization
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Broadwell Y 14nm Design/Process Optimizations Delivered 2x Lower Power than Traditional Scaling

A new process flavor for fanless optimization point for BDW –Y

<table>
<thead>
<tr>
<th></th>
<th>Traditional</th>
<th>14nm Broadwell Y Process Flavor</th>
<th>SoC Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance</td>
<td>0.75x</td>
<td>0.65x</td>
<td>25% lower power</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Enabled by transistor/interconnect scaling and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>optimizations</td>
</tr>
<tr>
<td>Lower Minimum operating</td>
<td>Same</td>
<td>10% lower</td>
<td>20% lower power</td>
</tr>
<tr>
<td>Voltage</td>
<td></td>
<td></td>
<td>Enabled by lower variation and design</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>optimizations</td>
</tr>
<tr>
<td>Low Voltage Transistor</td>
<td>Traditionally optimized for high voltage operation</td>
<td>10-15% transistor performance improvement</td>
<td>14nm was optimized for low-voltage performance</td>
</tr>
<tr>
<td>Performance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Leakage</td>
<td>0.8x</td>
<td>Optimized for 2X lower leakage</td>
<td>~10% lower power</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14nm natively optimized for BDW-Y</td>
</tr>
<tr>
<td>Area scaling</td>
<td>0.51x (feature neutral)</td>
<td>0.63x (with features)</td>
<td>Enabled by 14nm design rule and density</td>
</tr>
</tbody>
</table>
The Journey to Fanless:

- 14nm Process & Design Co-optimization
- Packaging and Form Factor Innovations
- 2nd Gen FIVR and 3DL Technology
- Enhanced Power Management
- Aggressive Power Reduction
Broadwell Y Platform Enabled Board Area Reduction of ~25% Compared to Haswell

50% Smaller XY
30% Smaller Z

Key Enablers:
• 0.63x scaling due to 14nm
• 0.5mm ball pitch
• 200um PKG Core
• 170um thin die
• 3DL

HSW U/Y
40x24x1.5mm

BDW-Y
30x16.5x1.04mm
The Journey to Fanless:

- 14nm Process & Design Co-optimization
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- 2nd Gen FIVR and 3DL Technology
- Enhanced Power Management
- Aggressive Power Reduction
2nd Generation FIVR & 3DL Power Delivery Efficiency

2nd Gen of FIVR enables better efficiency at lower voltages:

- Non-linear Droop Control
- Dual FIVR LVR Mode

3DL Modules:

- Inductors removed from package substrate to modules under the die. Better efficiency and package Z-height reduction
The Journey to Fanless:

- 14nm Process & Design Co-optimization
- Packaging and Form Factor Innovations
- 2nd Gen FIVR and 3DL Technology
- Enhanced Power Management
- Aggressive Power Reduction
Enhanced Turbo Boost: Maximizing the Opportunity to Boost While Maintaining System Reliability

![Graph showing Power vs Time with PL1, PL2, and PL3 levels]
Managing Excursions

Max Turbo

IA Frequency

Chipset Throttling

GT Frequency

T1  T2  T3

Duty Cycle Throttle
Turning blocks On/Off

Managing Excursions
System Optimized Thermal Management: Platform Power Sharing for Optimal Performance

Intel Dynamic Power & Thermal Management Framework

- Processor
  - Temperature
  - Power Control
  - P/T States
- Processor Graphics
  - Temperature
  - Power Control
  - RP States, EU^®
- PCH
  - Temperature
  - Power Control^®
- Memory
  - Temperature
  - Power Control^®
- WLAN, WWAN
  - Temperature
  - Power Control^®
- Battery Charger
  - Charge Rate Control
- Skin Thermal Sensor(s)
  - Temperature
- Display
  - Brightness Control
- System Fan(s)
  - Fine Grained Fan Control
The Journey to Fanless:

- 14nm Process & Design Co-optimization
- Packaging and Form Factor Innovations
- 2nd Gen FIVR and 3DL Technology
- Enhanced Power Management
- Aggressive Power Reduction
SoC Power Reduction

**Power = Active Power \((C_{\text{dyn}}V^2F)\) + Leakage Power**

**Active Power Reduction:**
- Design Process co-optimization to reduce minimum operating voltage
- Optimized design methods for \(C_{\text{dyn}}\) reduction
- Major re-arch of DDR/IO/PLL/Graphics
- Micro-architecture optimizations for \(C_{\text{dyn}}\) reduction in IA, Graphics and PCH
- IA/GT/Cache Lower Operating Frequency Range
- Other algorithmic enhancements (E.g. Dynamic Display voltage resolution)

**Leakage Power Reduction:**
- Design Process co-optimization to reduce minimum operating voltage
- Lowered \(T_{\text{jmax}}\) to reduce voltage
Extending the Efficient Operating Range

- **DCC**: Duty Cycle Control
- Implemented with HW & graphics driver collaboration
Enables ≤9mm Fanless 2-in1's for the First Time on the Intel Core™ Roadmap

Greater than 2X reduction in TDP with better performance vs. Haswell-Y

50% Smaller Package (XY), 30% Thinner

60% Lower SOC Idle Power for Increased Battery Life
Agenda: Broadwell Micro-architecture

The Fanless Challenge
The Journey to Fanless
Broadwell Converged Core Improvements
Graphics/Media/Display
Broadwell Converged-Core

>5% IPC over Haswell

- Larger out-of-order scheduler, Faster store-to-load forwarding
- Larger L2 TLB (1K to 1.5K entries), new dedicated 1GB Page L2 TLB (16 entries)
- 2nd TLB page miss handler for parallel page walks
- Faster floating point multiplier (5 to 3 cycles), Radix-1,024 divider, faster vector Gather
- Improved address prediction for branches and returns
- Targeted cryptography acceleration instruction improvements
- Faster virtualization round-trips

Power efficiency

- Performance features designed at ~2:1 Performance:Power ratio
- Power gating and design optimization increase efficiency at every operating point
Agenda: Broadwell Micro-architecture

The Fanless Challenge
The Journey to Fanless
Broadwell Converged Core Improvements
Graphics/Media/Display
Broadwell Graphics Architecture Provides Faster 3D and Compute Performance

3D / Compute Architectural Enhancements

- 20% More Computes and 50% Higher Sampler Throughput
- Microarchitecture improvements for Increased Geometry, Z, Pixel Fill Performance
- More Thermal Headroom with 14nm Process
- Scalable Architecture

Software Enhancements

- Continued Focus on Gaming with support for Direct X* 11.2 & OpenGL* 4.3
- OpenCL 1.2 and 2.0 (with Shared Virtual Memory support) for GPU compute

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Broadwell Graphics Architecture Provides End-to-End 4K Media Experience

Media Architecture Enhancements

- 50% more Media Sampler plus 20% more compute
- Up to 2x Video Quality Engine throughput
- Continued quality and performance improvement for Intel™ Quick Sync Video Technology.
- Significant power reduction (thus longer battery) provided by the energy efficient 14nm process

Display Technology

- Native support for 4K and UHD resolutions
- Improved SoC level power reduction and DPST

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Key Messages

Multi-year journey to exciting products

14nm provided a tremendous advantage

Embracing outside-in system design

Intel is furiously delivering on our vision with compelling products!
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• Relative performance for each benchmark is calculated by taking the actual benchmark result for the first platform tested and assigning it a value of 1.0 as a baseline. Relative performance for the remaining platforms tested was calculated by dividing the actual benchmark result for the baseline platform into each of the specific benchmark results of each of the other platforms and assigning them a relative performance number that correlates with the performance improvements reported.

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