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**Patents**

- 6762464, N-P butting connections on SOI substrates, 7/13/2004.
- 6706584, On-die de-coupling capacitor using bumps or bars and method of making same, 3/16/2004.
- 6337507, Salicide agglomeration fuse device with notches to enhance programmability, 1/8/2002.
- 5976939, Low damage doping technique for self-aligned source and drain regions, 11/2/1999.
- 5969404, Silicide agglomeration device, 10/19/1999.
- 5734187, Memory cell design with vertically stacked crossovers, 3/31/1998.
» 5420051, Pre-poly emitter implant, 5/30/1995.
» 4505026, CMOS process for fabricating integrated circuits, particularly dynamic memory cells, 3/19/1985.
» 4364075, CMOS dynamic RAM cell and method of fabrication, 12/14/1982.
» 4282648, CMOS process, 8/11/1981.
Publications/Speakershships


**Professional Affiliations**

- National Academy of Engineering member (2005)
- IEEE Fellow
- Senior sponsor for the University of Illinois campus for Intel’s Academic Relations group.
- Executive Committee for the VLSI Symposia