



Manufacturing with Intel® Products: System Manufacturing Test to Meet Quality Goals

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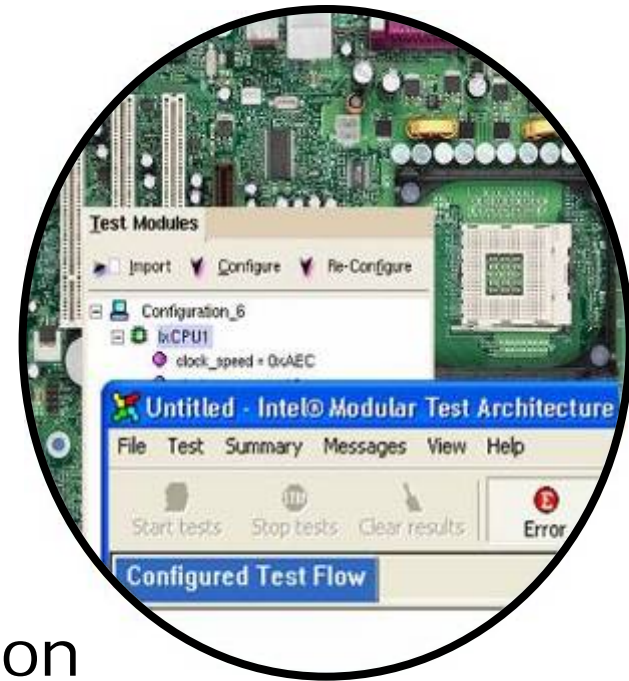
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Introduction

- The objective of MAS is:
 - to allow our customers test quality access and achieve successful High Volume Manufacturing as rapidly as possible (as opposed to waiting for test coverage)
 - to reduce **C**ustomer **L**ine **F**allout (CLF) → equating to higher 1st pass line yields, reduce **C**ustomer **I**nduced **D**amage (CID) returns and reduce **N**o **D**efect **F**ound (NDF) returns.
- This material is not designed to present detailed technical information or specifications, but to share experiences that can be utilized in **C**ustomer **M**anufacturing **E**nabling (CME).

Why Test at All?

- The main objective to testing is to meet quality requirements for the customer.
- The objective of functional testing is to ensure that all components attached to the CPU, Mother Board, and chassis are fully functional.
- The critical to functional **test limit** is the range within which the electrical circuits can be expected to meet specified performance requirements.
- Not testing the entire **functional limit** can degrade system performance, cause logic errors, or cause component and/or system damage.



Why Do I Need Increased Test Quality? (1/2)

- As CPU speeds, chipsets, operating systems, drivers, feature sets, and motherboard complexity change, the risks of quality escapes rise with each new change while the test software remains constant and unchanging.
- Test escapes cause increased warranty returns and field failures. Data matching with factory defects is crucial to the success for meeting world class quality. Hand written data logs are not accurate, and quality information and test software correlation is important.
- The impact of a premature device failure from stresses related to inadequate testing can result in infant mortalities in the field and loss of customers.

Why Do I Need Increased Test Quality? (2/2)

- Meeting customer quality goals.
- Independently stress test all the connections, components, and sockets on current processors.
- Improving supplier quality and design validation.
- Solution capable of detecting failure rates beyond 10K.
- Determine whether the process is at issue, instead of components.
- Time to Market



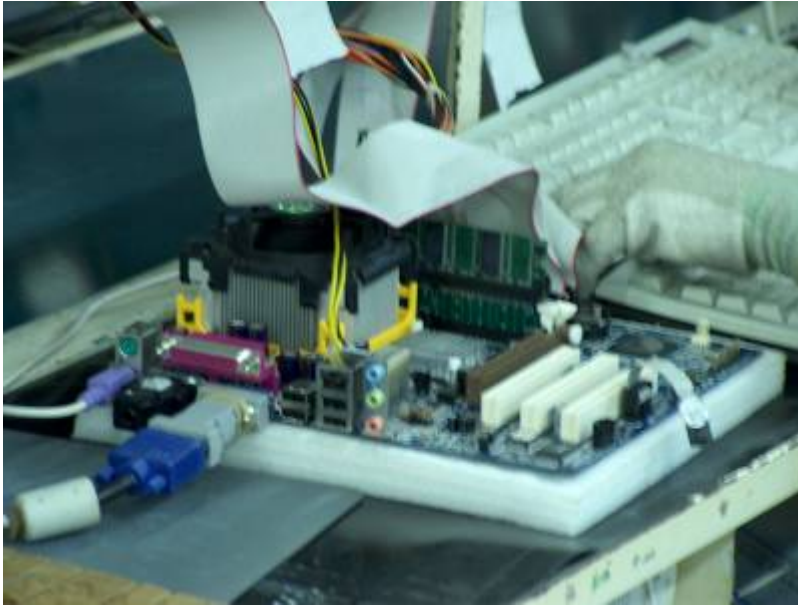
Test Architecture Overview (1/2)

There are some key items in a test architecture that help success of motherboard manufacturers:

- Test coverage using DOS is decreasing and is becoming more inadequate with time. Using the customer OS is preferred.
- Intel requires a minimum of all sockets and connectors be tested at systems level. (Example: Fully stuffed USB and memory)
- Intel uses ambient temperature tests only with added stress and coverage. Temperature cycling requirements or elevated temperature testing was eliminated or reduced to ORV (ongoing reliability validation) type tests.
- Reduce manufacturing escapes and excursions

Increases current test coverage from Low to High

Test Architecture Overview (2/2)



- Test stations in systems and boards **require a faster and more stressful test** solution than offered by PC test solutions.
- Using **a stress test** with increased test coverage provides a robust solution capable of **detecting** less than 1K DPM, faster test times, test package flexibility across multiple test platforms all to meet manufacturing quality goals and reduce warranty returns.
- Have a plan for testing all critical to function parameters identified for the products features and **manufacturing risks** that have been identified.

- ✓ On board programming (example = MAC address, ME, BIOS)
- ✓ Information system (example = test data collection)
- ✓ Fault coverage (example = audio and video coverage)
- ✓ Test stability (example = false failures)
- ✓ Test environment (example = AC power integrity)

Platform Test Priority/Formula

- ❑ **Programming**
(example = BIOS, MAC, and EEPROM, ME FW)
- ❑ **Assembly Verification**
(example = cables and add-in cards)
- ❑ **Correct Material**
(example = hard drive size, memory, firmware revision)
- ❑ **Latent Defects**
(example = long time to failure)
- ❑ **Test Process Health**
(example = false failures)



Current Operating Environment

- Some system test software is based on user influenced tests and pass/fail user interface. This results in a high percentage of test escapes or gaps in quality perception by manufacturing and customers.
- Most manufacturing test software does not permit the test suite to reduce test times or influence the amount of test stress needed in a factory environment.
- Direct measurement and correlation of returns can not be determined since most test HW equipment sets use different hardware combinations which make data impossible to correlate.

Software Design Envelope

- The Test Architecture extends from boards to systems manufacturing needs. Test software should be used at incoming receiving inspection all the way to post sales support.
- Test Architecture can be used by test engineers to add test modules for increased coverage.

Test Architecture Critical to Function Parameters (1/3) – overview

- ✓ **Processor Features**
- ✓ **MCH/GMCH**
- ✓ **Memory & Memory Bridge**
- ✓ **PCI/PCI-X/PCI-Express**
- ✓ **Network Controller**
- ✓ **Power Management Logic**
- ✓ **Video/Graphics**
- ✓ **SAS Features**
- ✓ **Removable Media**
- ✓ **(IPMI) Server Management**
- ✓ **IDE/ATA/SATA**
- ✓ **SCSI**
- ✓ **SMB**
- ✓ **Fan**
- ✓ **Hot Swap Controller / ICH**
- ✓ **Real Time Clock**
- ✓ **SIO Features**
- ✓ **Serial Ports**
- ✓ **Parallel Port**
- ✓ **Emergency Management Port**
- ✓ **Audio**
- ✓ **USB and 1394**
- ✓ **ICMB**
- ✓ **ME/AMT**
- ✓ **iTPM**

Test Architecture

Critical to Function Parameters (2/3)

<p>Processor Features</p> <p><u>CPU Type, Model & Stepping</u></p> <p><u>CPU Clock Speed</u></p> <p><u>Floating Point Unit</u></p> <p><u>MMX & MMX2 Instructions</u></p> <p><u>SIMD & XMM registers</u></p> <p><u>Cache, SMP Testing</u></p> <p><u>SMP Cache Coherency</u></p> <p><u>FSB Speed</u></p> <p>MCH/GMCH/PCH Features</p> <p>Device Type & Revision</p> <p>Internal Controller / Registers</p> <p>ME/AMT</p> <p>Memory & Memory Bridge</p> <p><u>Device Type & Revision</u></p> <p><u>Internal Controller / Registers</u></p> <p><u>Memory > 4GBytes</u></p> <p><u>Memory Bus Speed</u></p> <p><u>Memory Data Coherency</u></p> <p>Parallel Port</p> <p>Signal Lines</p> <p>Compatible - Unidirectional Mode</p>	<p><u>PCI/PCI-X/PCI-Express Features</u></p> <p><u>Devices Presence</u></p> <p><u>PCI Cfg Space & Device Enum</u></p> <p><u>Data Coherency</u></p> <p>Network Controller</p> <p>Presence & Revision Registers</p> <p>Network Frequency</p> <p>Data Coherency</p> <p>MAC Address Verification</p> <p>EEPROM Verification</p> <p>Serial over LAN</p> <p>Power Management Logic</p> <p>Wake on LAN Header</p> <p>Video/Graphics Features</p> <p>VGA Mode</p> <p>Intel® Graphics Config</p> <p>Memory Coherency, Size</p> <p>Video Signal Timing</p> <p>Pixel Count</p> <p>DAC</p> <p>Visual Dot Rate</p> <p>Resolution Modes</p> <p>Visual Pattern</p> <p>GDI, 3D, DirectX 9</p> <p>AGP and PCI-Express Modes</p>	<p>SAS Features</p> <p>Transfer Rate</p> <p>Data Coherency</p> <p>RAID</p> <p>Removable Media</p> <p>Transfer Rate</p> <p><u>Audio & MPEG Playback</u></p> <p><u>Media Presence & Change</u></p> <p><u>USB Drives</u></p> <p><u>Floppy, CD & DVD Drives</u></p> <p>SMB</p> <p><u>Hardware Monitor</u></p> <p>Serial EEPROM</p> <p>Alert-on-LAN</p> <p>Fan</p> <p>Presence</p> <p>Speed</p> <p>Hot Swap Controller Features</p> <p>Device ID, Self Test & FW Version</p> <p>Enclosure</p> <p>Switches, LEDs</p> <p>FW Mode & Checksum</p>	<p>ICH Features</p> <p>Device Type & Revision</p> <p>Internal Controller / Registers</p> <p><u>DMA Controller</u></p> <p>Multimedia Timers</p> <p>High Perf Event & 82C54 Timers</p> <p>ATA100 - 2 channels</p> <p>Real Time Clock Features</p> <p>Absolute Time</p> <p>Clock & Accuracy</p> <p>Interrupt & RAM</p> <p>SIO Features</p> <p>Device Type & Revision</p> <p>Programmable Interrupt Timers</p> <p>Programmable Interrupt Controller</p> <p>Keyboard & Mouse</p> <p>Speaker</p> <p>Serial Ports</p> <p>COM Internal/External Loop back</p> <p>COM Modem Status Reg</p> <p>COM Baud Rate</p> <p>COM FIFO, Status & Control signals</p>
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Test Architecture

Critical to Function Parameters (3/3)

<p>(IPMI) Server Management Features</p> <ul style="list-style-type: none"> Device ID, FW version & Self Test Watchdog Timer Post Code & System Event Log Generation Discrete Sensors Analog Sensors, switches, LEDs Fan Sensor & Control Secure Mode Firmware Update Mode & Checksum Heceta LAN Alert <p>Emergency Management Port Features</p> <ul style="list-style-type: none"> Device ID EMP MUX EMP Password DCD Activation RI Activation PING 	<p>Audio</p> <ul style="list-style-type: none"> Intel® High Definition Audio and Intel® AC'97 Audio FFT Analysis on all available channels Line Level, Coaxial and Optical <p><u>USB and 1394 Features</u></p> <p><u>Presence & Revision by Port</u></p> <p><u>Transfer Rate</u></p> <p><u>Data Coherency</u></p> <p><u>Modes (1.1 or 2.0)</u></p> <p>IDE/ATA/SATA Features</p> <ul style="list-style-type: none"> Presence & Revision Transfer Rate Data Coherency Register & Memory Access RAID <p>SCSI Features</p> <ul style="list-style-type: none"> Presence & Revision Transfer Rate Data Coherency Register & Memory Access RAID 	<p>(IPMI) Server Management Features</p> <ul style="list-style-type: none"> Device ID, FW version & Self Test Watchdog Timer Post Code & System Event Log Generation Discrete Sensors Analog Sensors, switches, LEDs Fan Sensor & Control Secure Mode Firmware Update Mode & Checksum <p><u>Heceta</u></p> <ul style="list-style-type: none"> LAN Alert <p>Emergency Management Port Features</p> <ul style="list-style-type: none"> Device ID EMP MUX EMP Password DCD Activation RI Activation PING 	<p>Parallel Port</p> <ul style="list-style-type: none"> Signal Lines Compatible - Unidirectional Mode <p>ICMB Features</p> <ul style="list-style-type: none"> Device ID, FW Version & Self Test Bridge State ICMB Address Chassis Online Data Loop Back Firmware Mode & Checksum <p>ICMB Features</p> <ul style="list-style-type: none"> Device ID, FW Version & Self Test Bridge State ICMB Address Chassis Online Data Loop Back Firmware Mode & Checksum
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Manufacturing with Intel® Management Engine (ME) Ignition Firmware on Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset

- 1. FLASH IMAGE CREATION: Tools and methods for BIOS/ME image creation.**
 - Recommend usage of the Intel® ME SPI Flash Image Configuration Wizard to create the entire flash image.
 - Recommend lock access to certain portions of flash during image development, rather than on the manufacturing line.
 - Recommend a combine BIOS/ME image be provided to factory floor. BIOS and ME are “paired” together so resultant change control challenges if BIOS and ME sent separately to factory.
- 2. BOARD DESIGN: Ensure that flash unlock capability is designed into the board, to assist with factory and post sales debug and repair.**
 - Recommend GPIO33 unlock mechanism be designed into the motherboard. Without GPIO33 unlock mechanism, flash device must be physically replaced if flash data corrupted or defective flash device.
- 3. FLASH IMAGE OWNER: Who in your company owns the BIOS/ME image?**
 - Recommend a single owner for the BIOS/ME image. Best for change control to limit the number of image region owners.
- 4. FLASH TOOLS: Use appropriate tools for all flash updates.**
 - Recommend the IBV flash tool for the BIOS/ME runtime image updates. Intel FPT tool can also be used for BIOS/ME flashing.

Manufacturing with Intel® Management Engine (ME) Ignition Firmware on Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset (Continued)

5. FLASH PROCESS VALIDATION.

- What does the “BIOS” update image contain? BIOS image may include both the BIOS and the Intel ME regions.
- Recommend that R&D team performed a first article inspection of the flash region. Need to ensure that correct BIOS and ME versions and configurations settings are correct.
- Ensure that IBV (BIOS Vendor) flash tool works properly. Be sure to understand what regions (BIOS, ME, MAC address, etc) are being flashed on system factory floor.
- Ensure that any utilities that write to the flash region, such as DMI, do not overwrite other regions inappropriately. Some utilities might inappropriately overwrite the MAC address, BIOS or ME regions.

6. SYSTEM TEST PROCESS:

- Recommend usage of MEManuf Test Tool to confirm that ME and firmware are OK. Takes <5 seconds to run.

7. SYSTEM AUDIT PROCESS:

- Recommend adding ME related tests to Outgoing Quality monitor process step.

Manufacturing with Intel® Management Engine (ME) Ignition Firmware on Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset (Continued)

- 8. BIOS/ME IMAGE DEPLOYMENT to factory floor:**
 - Recommend usage of a server/network to propagate the flash image. Media such as hard drives, floppies, CD's, DVD and USB flash sticks are difficult to maintain change control and slower to deploy image updates.
- 9. FLASH PROCESS: Unnecessary reflash of BIOS or ME exposes data image to corruption and requires additional factory test times.**
 - Recommend that system factory flash BIOS/ME image only on a as needed basis and limit to only 1 flash.
- 10. REWORK PROCESS: Clearing CMOS values:**
 - Recommend that clearing CMOS be performed with hardware reset method. Software CMOS clearing does not align all hardware to “reset” condition.
- 11. REWORK Process. Some flash devices will fail due to flash data corruption:**
 - Recommend that system factory has flash equipment to reflash devices with corrupted images.

Manufacturing with Intel® Management Engine (ME) Ignition Firmware on Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset (Continued)

- 12. Fault inject: Purposely not flash BIOS/ME on one board/system and then send that board/system thru test process .**
 - Recommend that test process coverage for correct BIOS/ME image be tested by sending a board/system without image thru test process. Ensure that test process detects and fails the board/system with the faulty BIOS/ME image.

- 13. BIOS/ME data corruption: Data corruption in factories can impact output, yield and quality of products.**
 - Recommend factory review the data corruption avoidance MAS.

- 14. ME system critical to functions: Defines items that impact ME process and product health.**
 - Recommend system factory review the system critical to function (CTF) list and align system manufacturing process to system CTF and reference process.

Future Challenges

- Customer transition to new BIOS and/or OS that are not supported by existing test solution providers
- Proliferation of test packages to support multiple product configurations.
- Test process must detect system induced damage
 - Motherboard and DDR strain flexure
 - Assembly issues
 - Insertion
 - Contaminated Material (flux on edge fingers)
- Customer hard drive software images are increasing in size. Flash image size increasing as well.
- Provisioning/programming ME FW and locking descriptor field.

Considerations

- Adding stress tests in manufacturing will improve quality.
- Owning the test coverage and test time creates flexibility in manufacturing.
- Eliminating elevated temp testing will reduce costs.
- Controlling quality goals by dialing in the quality of tests needed.
- Ensuring that ME/AMT configurations are properly set.

Presence and Functional Test Coverage Plans (an example)

Product Features	Test of Features from SOW Rev .XX	DOS		Windows			COMBINED	
		Presence (60%)	Functional (40%)	Presence (60%)	Functional (40%)			
		+	+	+	+		+	+
		+	+	+	+		+	+
				+	+	~ ~ ~	+	+
		+	+	+	+		+	+
		+	+	+	+		+	+
				+	+		+	+
		+	+	+	+		+	+

Note: Test Coverage shown here is an example only and not intended for use or reference to specific products.

SOW: Scope of Work

