

Intel[®] 82583V Gigabit Ethernet Controller Specification Update

August 2009
Revision 2.2

Order Number: 322117-003



Revision History

Date	Revision	Description
August 2009	2.2	Added Erratum #5. Updated Section 1.3.
June 2009	2.1	Added Specification Clarification #1.
June 2009	2.0	Initial Public Release.
April 2009	1.0	Initial Release (Intel Confidential).

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1.1 Introduction and Scope

This document applies to the 82583V GbE Ethernet Controller.

This document is an update to a published specification, the *Intel® 82583V GbE Controller Datasheet*. It is intended for use by system manufacturers and software developers. All product documents are subject to frequent revision, and new order numbers will apply. New documents may be added. Be sure you have the latest information before finalizing your design.

References to PCIe* in this document refer to PCIe Rev. 1.1 (2.5 GHz) x1.

1.2 Product Code and Device Identification

Product Code: WG825583V.

The following tables and drawings describe the identifying markings for the 82583V:

Table 1. Marking

Device	Stepping	Top Marking	Description
82583V	A1	WG82583V	Production (Lead Free)

Table 2. Device ID

82583V Device ID Code	Vendor ID	Device ID	Revision ID
82583V	0x8086	0x150C	N/A

Table 3. MM Numbers

Product	MM Number	Tray/Tape and Reel
WG82583V	903008	Tape and Reel; SLGVC
WG82583V	903072	Tray; SLGVD

1.3 Marking Diagram

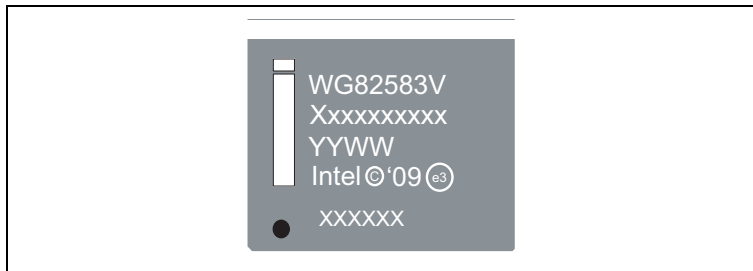


Figure 1. Top Marking Example With Identifying Marks

Notes:

- Line 1: Marketing Name (WG82583V)
- Line 2: TSMC Fab Lot Number "XXXXXXXX" or "XXXXXXXX.X"
- Line 3: Assembly Date Code "YYWW"
- Line 4: "INTEL", © Copyright including two number date code, circled "e3" lead-free mark
- Line 5: Country of Origin

1.4 Nomenclature Used In This Document

This document uses specific terms, codes, and abbreviations to describe changes, errata, sightings and/or clarifications that apply to silicon/steppings. See [Table 4](#) for a description.



Table 4. Terms, Codes, Abbreviations

Name	Description
Specification Changes	Modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.
Errata	Design defects or errors. Errata may cause device behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.
Specification Clarifications	Greater detail or further highlights concerning a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.
Documentation Changes	Typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.
Yes or No	If the errata applies to a stepping, "Yes" is indicated for the stepping (for example: "A0=Yes" indicates errata applies to stepping A0). If the errata does not apply to stepping, "No" is indicated (for example: "A0=No" indicates the errata does not apply to stepping A0).
Doc	Document change or update that will be implemented.
Fix	This erratum is intended to be fixed in a future stepping of the component.
Fixed	This erratum has been previously fixed.
NoFix	There are no plans to fix this erratum.
Eval	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box)	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Red Change Bar/or Bold	This Item is either new or modified from the previous version of the document.
DS	Data Sheet
DG	Design Guide
SDM	Software Developer's Manual
EDS	External Data Specification
AP	Application Note

1.5 Changes, Errata, and Clarifications

See [Section 1.4](#) for an explanation of terms, codes, and abbreviations used in the following tables and discussions.



Table 5. Summary of Changes, Errata and Corrections; Errata Include Steppings

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1.5.1 Specification Changes

None active.

1.5.2 Specification Clarifications

1. A1=Yes; No Fix. Spec Clarification for PCIe 1 Devices

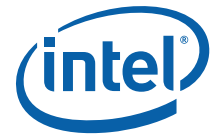
If the latency for PCIe completions in a system is above 21 ms and PCIe completion timeout mechanism is enabled, there may be unpredictable system behavior.

The 82583V complies with the PCIe 1.1 specification for completion timeout mechanism. The PCIe 1.1 specification provides a timeout range between 50 μ s to 50 ms with a strong recommendation that it be at least 10 ms. The 82583V uses a range of 21-42 ms.

The completion timeout value in a system MUST be above the expected maximum latency for completions in the system in which the 82583V is installed. This will ensure that the 82583V receives the completions for the requests it sends out, avoiding a completion timeout scenario. If the latency for completions is above 21 ms this can result in the device timing out prior to a completion returning. In the event of a completion timeout, per direction in the PCIe specification the device assumes the original completion is lost, and resends the original request. In this condition, if the completion for the original request arrives at the 82583V devices, this will result in two completions arriving for the same request, which may cause unpredictable system behavior.

Therefore, if the PCIe completion latency for a system cannot be guaranteed to be lower than 21 ms, the PCIe completion timeout mechanism should be disabled by setting GCR.Disable_timeout_mechanism.

For more details on Completion Timeout operation in the 82583V refer to the *Intel® 82583V GbE Controller Datasheet*.



1.5.3 Documentation Changes

None active.

1.5.4 Errata

1. A1=Yes; No Fix. 10BASE-T IEEE-Specified Harmonic Content Level Issue

Problem: On some board designs, the 82583 might not meet the IEEE specification (1411.10.03) that states that the harmonic content is to be at least 27 dB below the 10 MHz fundamental frequency.

Implication: IEEE conformance is marginal. There is no impact on system level performance; however, care should be taken to verify the impact of radiated EMI (Electromagnetic Interference) on system-level EMI tests.

Workaround: There is no silicon/firmware/software workaround; however, using short low-resistance traces (less than four inches and without a LAN switch) can help reduce harmonic content.

Status: No Fix. There are no plans to fix this erratum.

2. A1=Yes; No Fix. 100BASE-TX Marginal Rise/Fall Time Performance

Problem: The 82583 rise/fall time has been marginal compared to the IEEE specification (5 ns).

Implication: IEEE conformance is marginal. Depending on system topology (LAN switch/no LAN switch), MDI trace lengths, and configuration (docked/undocked), the 100BASE-TX rise/fall time might not meet the IEEE specification. Note that there is no impact on system level performance.

Workaround: There is no silicon/firmware/software workaround. However, using short low-resistance traces (less than four inches and without a LAN switch) can help improve rise time. In some designs it's better to use two 82583's instead of a LAN switch.

Status: No Fix. There are no plans to fix this erratum.

3. A1=Yes; No Fix. Revision ID is Zero for the 82583 A1 Stepping

Problem: The Revision ID field in the PCIe configuration space is zero instead of one.

Implication: Error counters may not be accurate.

Workaround: None.

Status: No Fix. There are no plans to fix this erratum.



4. A1=Yes; No Fix. Missing Interrupt Following ICR Read

Problem: If the Interrupt Cause Register (ICR) is read when at least one bit is set in the interrupt mask register and INT_ASSERTED is set to 0b, a new interrupt event occurring on the same clock cycle as the ICR read is ignored.

Implication: Missed interrupts leading to delays in responding to interrupt events. Specifically, this can cause a delay in processing a received packet.

Typically, the ICR is only read in response to an interrupt so this problem does not occur. However, when using legacy interrupts and sharing interrupts between devices, software might poll all the devices to find the source of the interrupt, including those devices that did not assert an interrupt. There might also be other situations in non-Intel drivers where ICR is polled even when no interrupt has been asserted.

Workaround: If reading ICR when there is no active interrupt cannot be avoided, clear the mask register (by writing 0xFFFFFFFF to IMC) before reading ICR. Note that in this case the ICR is cleared when read even if INT_ASSERTED is set 0b.

Status: No Fix. There are no plans to fix this erratum.

5. A1=Yes; No Fix. PCIe: Missing Replay Due to Recovery During TLP Transmission

Problem: If the replay timer expires during the transmission of a TLP and the LTSSM moves from L0 to recovery during the transmission of the same TLP, the expected replay does not occur. Additionally, the replay timer is disabled, so no further replays occur unless a NAK is received.

Implication: This situation should not occur during normal operation. If it does occur while the upstream switch is waiting for a replay, the result would be a Surprise Down error which might halt the system.

Workaround: None.

Status: No Fix. There are no plans to fix this erratum.