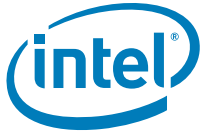


Intel[®] 3100 Chipset

Specification Update

November 2010

Notice: The Intel[®] 3100 Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.



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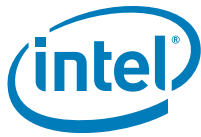
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Revision History

Revision	Description	Date
001	Initial public release	June 2006
002	Added A1 information (i.e., device id, component markings, fixed errata #35-37), added specification clarifications #2-3, added documentation change #1.	November 2006
003	Corrected inaccuracy in the External Design Specification regarding XOR chain #3 and XOR chain #4. These fixes were added as documentation change #2. Added Documentation Change 1 which documents additional processors supported by the Intel® 3100 Chipset.	June 2007
004	Added Documentation Change 2 which documents an additional Intel® Core™2 Duo processor L7400 supported by the Intel® 3100 Chipset.	June 2007
005	Added Documentation Change 1 which documents an additional Intel® Core™2 Duo processor U7500 supported by the Intel® 3100 Chipset. Added Specification Change 1 to correct the TAP pin VIL maximum level from 0.5 V to 0.35 V.	August 2007
006	For Erratum 24, the workaround was clarified to point customers to the ICH6 BIOS Specification Update, instead of the BIOS Specification. Added 16 Specification Clarifications (1 to 19). Added five Documentation Changes (1 to 6).	November 2007
007	Added Spec Change #2 to update and add Icc Max Currents to Data Sheet. Fixed Spec Clarification #11 to change the HCLKIN 700 mil trace length recommendation back to 425 mil. Added 5 Spec Clarifications (20 to 24) related to PCIE Spread-Spectrum limitations, USB 33MHz Baud clock operations, added Intel® 3100 Chipset Package substrate dimension and clarifications to 2 Platform Design Guides.	April 2008
008	Added Errata 40. Updated Errata 5. Added Errata 41. The Intel® 3100 Chipset Datasheet has been updated to include all previously relevant Specification Changes/Clarifications and Documentation Changes; as such references to these documents have been removed here.	November 2008
009	Added Specification Clarification 2 and 3 Updated Affected Documents/Related Documents table The Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide, Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform Design Guide, and Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide have been updated to include all previously relevant Specification Changes/Clarifications and Documentation Changes.	March 2009
010	Added Errata 42	July 2009
011	Added Specification Clarification 4. Added Errata 43.	August 2009
012	Added Specification Clarification 5.	April 2010
013	Added Specification Clarification 6.	November 2010



Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and document errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in the Nomenclature section are consolidated into this update document and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Document Title	Location/CDI Number
Intel® 3100 Chipset Datasheet	http://developer.intel.com/design/intarch/datashts/313458.htm
Intel® Pentium® M Processor on 90nm Process and Intel® 3100 Chipset Development Kit User's Manual	http://www.intel.com/design/intarch/manuals/313498.htm
Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Development Kit User's Manual	http://www.intel.com/design/intarch/manuals/315879.pdf
Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset Development Kit User Guide	http://www.intel.com/design/intarch/manuals/316639.pdf
Intel® 3100 Chipset External Design Specification Addendum	Document Number 394371-3.1 Contact your Intel sales representative.
Intel® Pentium® M Processor on 90 nm process and Intel® 3100 Chipset Platform Design Guide	Document Number: 349801-2.1 Contact your Intel sales representative.
Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide	Document Number: 645136-2.1 Contact your Intel sales representative.
Intel® Core™ 2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform Design Guide	Document Number: 349830-2.1 Contact your Intel sales representative
Intel® Core™ 2 Duo LV/ULV on 45 nm process and Intel® 3100 Chipset Platform Design Guide	Document Number: 383399 2.1 Contact your Intel sales representative.

Nomenclature

Errata are design defects or errors. These may cause the Intel® 3100 Chipset to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

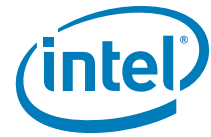


Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note:

Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 3100 Chipset product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark) or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been fixed in a previous stepping.

No Fix: There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



Summary Table of Changes (Sheet 1 of 2)

No.	Stepping		Page	Status	ERRATA
	A0	A1			
1	X	X	11	No Fix	DMA channel source address checking error
2	X	X	11	No Fix	Data corruption after illegal front side bus configuration write
3	X	X	11	No Fix	Incorrect PCI Express* (PEA) link/lane numbers driven in degraded link
4	X	X	11	No Fix	PCI Express* (PEA) enhanced configurations to non-existent devices cause a system hang
5	X	X	12	No Fix	Spurious errors logged during link training events
6	X	X	12	No Fix	DDR2 write offset issue
7	X	X	12	No Fix	Intel® 3100 Chipset fails to train when non-TS1/TS2 training sequences are received
8	X	X	13	No Fix	Configuration transaction may be ignored in the Intel® 3100 Chipset when Configuration Request Retry Status is enabled in PCI Express* (PEA) to PCI/PCI-X bridges
9	X	X	13	No Fix	PCI Express* (PEA) x4 and x8 links may train down to lower width
10	X	X	14	No Fix	END symbol omitted from the last PM_Request_Ack DLLP while entering L2 state on x1 PCI Express* (PEA) link
11	X	X	14	No Fix	SMBSDA and SMBSCS signals pulled down in S5
12	X	X	14	No Fix	Multiple PCI Express* port PEA protocol errors may result in fatal receiver overflow
13	X	X	14	No Fix	System marginalities may result in spurious link-down error events on power state changes
14	X	X	15	No Fix	SATA COMINIT/COMWAKE Detection
15	X	X	15	No Fix	Noise on PCI Express* (PEB) TX coming out of Electrical Idle
16	X	X	15	No Fix	Intel® 3100 Chipset sending less than the minimum number of Power Management Acknowledgements (PMAKs) to SATA
17	X	X	16	No Fix	Advanced Host Controller Interface (AHCI): Improper length Register Device-to-Host FIS
18	X	X	16	No Fix	Split-Lock cycle to LPC space resulting in FSB timeout and IERR
19	X	X	16	No Fix	Intel® 3100 Chipset SATA signal voltage level
20	X	X	16	No Fix	PCI Express* (PEB) completion timer not halting in L1
21	X	X	16	No Fix	PCI Express* (PEB) Extended Tag capability bit
22	X	X	17	No Fix	Intel® 3100 Chipset does not ignore a PCI Express* Null Packet on port PEB
23	X	X	17	No Fix	PCI Express* port PEB Link layer should drop Data Link Layer Packets (DLLPs) with unknown encoding type
24	X	X	17	No Fix	SATA SRST during link power states
25	X	X	17	No Fix	Unsolicited COMINIT while FIS posting pending will corrupt the FIS posting cycle
26	X	X	17	No Fix	USB output voltage
27	X	X	18	No Fix	Intel® 3100 Chipset AHCI PxCMD.CR bit
28	X	X	18	No Fix	Intel® 3100 Chipset PIO setup FIS error
29	X	X	18	No Fix	Intel® 3100 Chipset PCI Express* port PEB surprise removal
30	X	X	18	No Fix	SATA EB buffer overflow should set ERR.E bit instead of ERR.M bit
31	X	X	19	No Fix	PCI Express* port PEB SKP/InitFCx contention
32	X	X	19	No Fix	PCI Express* port PEB downstream ports flag inbound 4 KByte memory read as malformed TLP
33	X	X	19	No Fix	Full Speed USB ISOC End of Packet
34	X	X	19	No Fix	AHCI Host Bus Adapter (HBA) BSY bit set when recovering from fatal error
35	X		20	Fixed	Intel® 3100 Chipset 2 Gbit refresh violation



Summary Table of Changes (Sheet 2 of 2)

No.	Stepping		Page	Status	ERRATA
	A0	A1			
36	X		20	Fixed	Intel® 3100 Chipset lock-up due to internal downstream EDMA and arbitration error
37	X		20	Fixed	System lock condition with numerous split-lock cycles on PCI Express* Port B in conjunction with Heavy PCI Express* traffic on both Port A and Port B
38	X	X	21	No Fix	PCI Express* Port PEB scrambling
39	X		21	No Fix	Behavior of Serial Port Interrupt Enable Register
40	X	X	21	No Fix	Intel® 3100 Chipset boundary scan operation is not guaranteed above room temperature
41	X	X	21	No Fix	Potential performance/hang issue caused by incorrect default setting of FSB Retry Grace Period
42	X	X	22	No Fix	PCI Express Enable No Snoop ENS register bit not behaving as specified
43	X	X	22	Fixed	Memory initialization may fail at low temperatures.

Specification Changes

No.	Page	SPECIFICATION CHANGES
		No specification changes for this revision of this specification update.

Specification Clarifications

No.	Page	SPECIFICATION CLARIFICATIONS
1	24	Access to TPM components not enabled
2	24	PECLK Period Discrepancies
3	25	AC Coupling when using PCIE down devices
4	25	FSB Max Undershoot TYPO by a factor of 10.
5	25	Clarifications to Tables in Electrical Characteristics Section of Datasheet
6	28	Pairing Intel® 3100 Chipset with Intel® Core™ Duo Processor

Documentation Changes

No.	Page	DOCUMENTATION CHANGES
1	29	USB3/2 ports need to be swapped in User's Manuals



Identification Information

Component Identification via Programming Interface

The Intel® 3100 Chipset can be identified by the following register contents:

Stepping	Vendor ID ¹	Device ID ²	Stepping ID ³
A0	8086h	2670h	00h
A1	8086h	2670h	01h

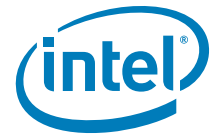
Notes:

1. The Vendor ID corresponds to bits [15:0] of the Vendor ID Register located at offset 00–01h in the PCI B0: D31: F0 configuration space.
2. The Device ID corresponds to bits [15:0] of the Device ID Register located at offset 02–03h in the PCI B0: D31: F0 configuration space.
3. The Stepping ID corresponds to bits [23:16] of the Manufacturer's ID Register located at offset F8h in the PCI B0: D31: F0 configuration space.

Component Marking Information

The Intel® 3100 Chipset stepping can be identified by the following component markings:

Stepping	Q-Spec/S-Spec	Description
A0	Q176	Pb Free Engineering
A0	SL8YC	Pb Free Production
A1	Q699	Pb Free Engineering
A1	SL9PU	Pb Free Production



Errata

1. DMA channel source address checking error

Problem: In the DMA controller memory mapped registers, bit [6] of the DCRs (Descriptor Control Registers Memory Mapped I/O Address Offset 2Ch-2Fh, 6Ch-6Fh, 0ACh-A7h, 0ECh-EFh) for channels 0-3 should be RO, but it is implemented as RW.

Implication: The DMA controller does not implement error checking for this case if this bit is set to '1.'

Workaround: Do not write a '1' to bit [6] of the DCRx for channels 0-3.

Status: No Fix.

2. Data corruption after illegal front side bus configuration write

Problem: When an illegal FSB configuration write occurs (bits [30:24] of the Configuration Address Register [CONFIG_ADDRESS, I/O address 0CF8h] are non-zero), PCI configuration accesses following this write may be corrupted.

Implication: This is a mishandled error case and causes corruption of transactions after this transaction. This is an illegal case.

Workaround: Do not write non-zero values to the PCI configuration address register reserved fields.

Status: No Fix.

3. Incorrect PCI Express* (PEA) link/lane numbers driven in degraded link

Problem: If a failure of receiver detect or bit/symbol lock occurs on lane 0 (lane 7 in the case of a physical lane reversal) while other lanes successfully achieve bit/symbol lock in the early stages of Polling.Active, the Intel® 3100 Chipset will exhibit anomalous lane numbering during the ensuing failed training sequence. Note that this anomalous behavior only occurs in situations where the combination of successful and failing lanes will result in a training failure, and a return to the Polling state.

Implication: When such a failed training is in progress, non-compliant non-PAD lane numbers may be observed on the Intel® 3100 Chipset downstream lanes. The observed behavior may be seen as the Intel® 3100 Chipset attempting a link split.

Workaround: None

Status: No Fix.

4. PCI Express* (PEA) enhanced configurations to non-existent devices cause a system hang

Problem: A system hang may occur when writing or reading to offsets above 0FFh using the PCI Express* (PEA) enhanced configuration space of a non-existent device.

Implication: An invalid access error will be flagged, and a system hang may result.

Workaround: Polling or testing for devices must be done using offsets below 0FFh. Access must not be issued to offsets above 0FFh unless the targeted device is confirmed present.

Status: No Fix.



5. Spurious errors logged during link training events

Problem: The Intel® 3100 Chipset reports spurious receiver errors during initial link training, after a retrain, or after a secondary bus reset has occurred.

Implication: Spurious receiver errors will be logged in the associated port. There are no negative side effects besides the misreported error.

Workaround: Upon initial training and after each retrain or secondary bus reset clear the following bits (if set): NSI_FE, PA_FE, or PA1_FE of the Global First Error and Global Next Error Registers (GLOBAL_FERR, Device 0, Function 1, Offset 40-43h bits[25/23/22]) and (GLOBAL_NERR, Device 0, Function 1, Offset 44-47h bits[25/23/22]).

If NSI_FE (bit 25) was set in GLOBAL_FERR or GLOBAL_NERR, clear the Receiver Error Status bit of the NSI First Error and NSI Next Error Registers (NSI_FERR, Device 0, Function 1, Offset 48-4Bh, bit[9]) and (NSI_NERR, Device 0, Function 1, Offset 4C-4Fh, bit[9]).

If the PA_FE (bit 23) or PA1_FE (bit 22) were set in GLOBAL_FERR or GLOBAL_NERR, clear the following bits in the following registers:

- Correctable error detected bit of the PCI Express Device Status Register (PEADDEVSTS, Device 2-3, Function 0, Offset 6E-6Fh, bit[0])
- Receiver error status bit of the PCI Express Correctable Error Status Register (CORERRSTS, Device 2-3, Function 0, Offset 110-113h, bit[0])
- Correctable error bits of the Root Port Error Message Status Register (RPERRMSTS, Device 2-3, Function 0, Offset 130-133h, bits[0/1])
- Correctable error bits of the PCI Express First Error and PCI Express Next Error Registers (PEAFERR, Device 2-3, Function 0, Offset 160-163h, bit[6]) (PEANERR, Device 2-3, Function 0, Offset 164-167h, bit[6])

Status: No Fix.

6. DDR2 write offset issue

Problem: DQ/DQS signals terminate to a level about 300 mV below VDDQ/2 between write bursts. No functional failures have been observed as a function of this issue.

Implication: Signal integrity issues may be observed.

Workaround: None

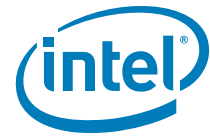
Status: No Fix.

7. Intel® 3100 Chipset fails to train when non-TS1/TS2 training sequences are received

Problem: During the PCI Express (PEA) training sequence, if a broken endpoint or a good endpoint on a broken board has correct receiver termination on any lane and transmits signals on that lane that can be seen at the Intel® 3100 Chipset and are not valid TS1/TS2 training sequences, the Intel® 3100 Chipset will fail to train that link.

Implication: The PCI Express specification intends that, if some lanes are transmitting bogus data instead of valid training sequences, those lanes should be treated as broken, and the link should fail down to an acceptable width (such as x1). If lane 0 were failing in this manner, the link would fail to train per the PCI Express specification. If a higher-numbered lane were failing in this manner, the PCI Express specification requires the link attempt to train as a x1 on lane 0—the Intel® 3100 Chipset will not train in this scenario.

Failures are anticipated to occur because of a broken transmitter/receiver path, or a silent transmitter. None of those failure modes will cause the Intel® 3100 Chipset to fail to train, since either the receiver termination will be missing, or the transmitted signals



will not be seen at the Intel® 3100 Chipset. In order to see invalid transmitted signals at the Intel® 3100 Chipset, either a logic bug in the other PCI Express endpoint would be required, or a signal integrity issue so severe as to make operation impossible.

Workaround: None

Status: No Fix.

8. Configuration transaction may be ignored in the Intel® 3100 Chipset when Configuration Request Retry Status is enabled in PCI Express* (PEA) to PCI/PCI-X bridges

Problem: Under certain circumstances that include a mix of PCI Express traffic in the presence of completions with Configuration Retry Status (configuration space traffic receiving CRS, and other traffic that is posted / governed by Posted Flow Control credits) on a given PCI Express port, the Intel® 3100 Chipset may ignore and fail to issue an outbound configuration space access indefinitely. This behavior has been observed in configurations with PCI Express to PCI/PCI-X bridge devices under circumstances where at least one device behind the bridge is active and operational, while at least one other device behind the bridge remains unresponsive to configuration requests for an extended period of time. Such failures ultimately manifest themselves as CPU IERR# assertions, which commonly precipitate a platform reboot. Completions with Configuration Request Retry Status are generally sent by a PCI Express to PCI/PCI-X bridge when it relays configuration space traffic to a PCI/PCI-X device which exhibits a long latency in responding to configuration space traffic. The CRS completion status mechanism is intended to prevent a PCI Express completion timeout from occurring in cases where historical PCI/PCI-X implementations would experience an extended latency without response, but would not generate any timeout or associated error.

Implication: A system hang may occur.

Workaround: To avoid configuration transactions from being ignored, Intel strongly recommends that BIOS should disable Configuration Request Retries in all PCI Express bridge devices. For the Intel® 6700PXH 64-bit PCI Hub, this is accomplished by clearing the Bridge Configuration Retry Enable bit in the Device Control Register (D0:F0,2:R04Ch bit [15]). This bit is cleared by default. Some PCI or PCI-X devices may require a lengthy self-initialization sequence (up to 1.5 sec. as defined by PCI Express Base Specification 1.0a) to complete before they are able to service Configuration Requests after reset. In order to ensure the ability of the system to successfully enumerate PCI devices, BIOS should disable PCI Express Completion Timeout in the root port configuration of the Intel® 3100 Chipset links connected to the Intel® 6700PXH 64-bit PCI Hub, Intel® IOP332 I/O processor, and Intel® 41210 Serial to Parallel PCI Bridge (including add-in cards) by setting the Completion Timeout Timer Disable bit in the Vendor Specific Command Register (D2-7:F0:R045h bit [3]). BIOS should ensure that the Completion Timeout Timer remains enabled (default) for other active PCI Express links. BIOS should also ensure that the Completion Timeout Error Mask is set in the Intel® 3100 Chipset root ports associated with inactive PCI Express links (unpopulated slots or disabled devices).

Status: No Fix.

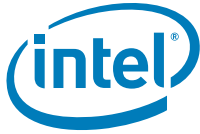
9. PCI Express* (PEA) x4 and x8 links may train down to lower width

Problem: It has been observed that x4 and x8 links may fail to train to their full link widths. This behavior occurs infrequently. The issue is caused by the Intel® 3100 Chipset exiting the Polling.Active state and entering the Polling.Config state prior to the downstream device entering the Polling.Active state.

Implication: PCI Express ports may fail to train at full width.

Workaround: Intel recommends an algorithm that will issue a Secondary Bus Reset upon a link training failure for 2 ms. The algorithm should support at least three iterations of Secondary Bus Resets.

Status: No Fix.



10. END symbol omitted from the last PM_Request_Ack DLLP while entering L2 state on x1 PCI Express* (PEA) link

Problem: When a PEA x1 link transitions into the L2 state, the Intel® 3100 Chipset may fail to transmit the END symbol of the last PM_Request_Ack DLLP.

Implication: If a downstream device expects an END symbol in the last PM_Request_Ack DLLP from the Intel® 3100 Chipset, it may incorrectly decode the electrical ordered set that follows. Endpoints should expect the COM symbol in the electrical ordered set to indicate a final confirmation to transition the link to the L2 state.

Workaround: None

Status: No Fix.

11. SMBSDA and SMBSCSCL signals pulled down in S5

Problem: According to SMBus Specification 2.0, the SMBSDA and SMBSCSCL signals are to float while in the S5 state. Due to device protection circuitry, these signals are pulled down while in the S5 state.

Implication: Devices on auxiliary power such as a BMC that share an SMBus connection with the Intel® 3100 Chipset will not be able to signal on the SMBus in the S5 state due to the signals being pulled down.

Workaround: A mux can be incorporated into the SMBus to disconnect the Intel® 3100 Chipset when the platform goes into the S5 state.

Status: No Fix.

12. Multiple PCI Express* port PEA protocol errors may result in fatal receiver overflow

Problem: If a PCI Express device connected to the Intel® 3100 Chipset port PEA generates multiple transaction layer protocol errors, including unexpected completion packets or malformed Transaction Layer Packets (TLPs) that otherwise pass all link-layer error checking, and have the correct alignment on the interface, the Intel® 3100 Chipset may experience a fatal receiver overflow.

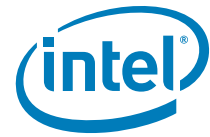
Implication: If the above conditions are met, the Intel® 3100 Chipset may detect and log a fatal receiver overflow error. The Intel® 3100 Chipset behavior in the presence of this error is consistent with the specification, in that continued operation on the port after such an error may be unreliable.

Workaround: Intel recommends avoiding the use of PCI Express devices that generate unexpected completion or malformed TLP protocol violations. If this is unavoidable, the receiver overflow error detected by the Intel® 3100 Chipset may be escalated to a system event (e.g., SERR#) that prevents continued operation on the compromised link.

Status: No Fix.

13. System marginalities may result in spurious link-down error events on power state changes

Problem: On system power state changes (S3 and S5), PCI Express devices are placed in the D3 device power state by the operating system, which results in automatic negotiation with the Intel® 3100 Chipset to enter the L1 link state. In systems where the cumulative noise present at the Intel® 3100 Chipset receiver pins exceeds the Intel® 3100 Chipset receiver threshold for detecting Electrical Idle, the transition into L1 may fail to complete normally; ultimately, resulting in a spurious link-down error from the Intel® 3100 Chipset. If a link-down error (D2-3:F0:0140h, bit [11]) is escalated using a fatal system error (SERR#) mechanism, a blue-screen may result on exposed systems.



The PCI Express specification for Electrical Idle at the receiver is 65 mV peak-peak differential, and characterization of the Intel® 3100 Chipset indicates that some lanes on some devices are marginal with respect to this specification. While L1 failures should be exceedingly rare, Intel recognizes that this specification is difficult to meet and acknowledges the exposure.

Implication: Systems with sufficient noise at the Intel® 3100 Chipset receivers and a BIOS profile that escalates the link-down error as a fatal system event may be exposed to a blue-screen occurrence on system power state transitions. Exposure to the error increases with the cumulative noise (platform noise + silicon noise) present at the Intel® 3100 Chipset receivers when the link is in Electrical Idle. Systems utilizing a BIOS configuration that does not escalate the link-down error as a fatal error are not exposed.

Custom operating systems or future operating systems that independently manage the power state of PCI Express devices outside the scope of system power state transitions would be similarly exposed to link-down errors via the same mechanism. In cases where the destination power state on the attached device is between D0 and D3, any such link-down event constitutes a real error from which software may only recover by fully reconfiguring the devices below the affected link.

Workaround: None

Status: No Fix.

14. SATA COMINIT/COMWAKE Detection

Problem: During Out-Of-Band (OOB) sequencing, the Intel® 3100 Chipset may detect COMINIT/COMWAKE when only two or three bursts of ALIGNs are received from the SATA device instead of the required four bursts as per the SATA Specification 1.0a.

Implication: No known implications—the Intel® 3100 Chipset appropriately handles subsequent ALIGNs.

Workaround: None

Status: No Fix.

15. Noise on PCI Express* (PEB) TX coming out of Electrical Idle

Problem: The PCI Express (PEB) Common Mode Voltage is not stable immediately after Receiver Detect Sequencing when entering Polling.Active from Detect.Active states.

Implication: Common Mode Voltage noise may result in bet errors early in the Polling.Active state. It may result in additional training time before transitioning on to Polling.Configuration.

Workaround: None

Status: No Fix.

16. Intel® 3100 Chipset sending less than the minimum number of Power Management Acknowledgements (PMAKs) to SATA

Problem: The SATA specification requires the Intel® 3100 Chipset to send at least four PMAKs to the SATA device. The Intel® 3100 Chipset sends only three PMAKs before entering a lower power state after the device requests a partial or slumber state on the SATA bus.

Implication: This errata violates the SATA specification but is not expected to cause any functional failures.

Workaround: None

Status: No Fix.



17. **Advanced Host Controller Interface (AHCI): Improper length Register Device-to-Host FIS**

Problem: If a SATA device sends less than a five dword Register Device-to-Host FIS, the Intel® 3100 Chipset will correctly respond with RERR but may not be able to accept any further FISes from the device.

Implication: The SATA bus will hang. This only applies while operating in AHCI mode. No known devices use Register Device-to-Host FIS sizes less than five dwords, as these are not allowed by the SATA Specification 1.0a.

Workaround: The AHCI driver should reset the bus by sending COMRESET per the AHCI specification.

Status: No Fix.

18. **Split-Lock cycle to LPC space resulting in FSB timeout and IERR**

Problem: The Intel® 3100 Chipset may not properly handle split locked cycles to the LPC when a PHOLD sequence is going on concurrently. The hang occurs when the second split lock memory read request is sent out on the NSI but never receives a completion.

Implication: The system could hang. This issue has only been replicated using a synthetic test environment and has not been reported using commercially available hardware/software.

Workaround: None

Status: No Fix.

19. **Intel® 3100 Chipset SATA signal voltage level**

Problem: The Intel® 3100 Chipset SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel® 3100 Chipset SATA transmit signalling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specification (section 6.6.2 of the SATA Specification 1.0a).

Implication: No known implications.

Workaround: None

Status: No Fix.

20. **PCI Express* (PEB) completion timer not halting in L1**

Problem: The Intel® 3100 Chipset PCI Express completion timer does not halt when the link enters the L1 state. This affects the port PEB.

Implication: The Intel® 3100 Chipset will flag a completion timer error.

Note: This requires a device that is not fully compliant with the PCI Express specification and has only been replicated in a synthetic test environment.

Workaround: None

Status: No Fix.

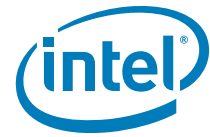
21. **PCI Express* (PEB) Extended Tag capability bit**

Problem: The Intel® 3100 Chipset incorrectly has the PCI Express Extended Tags Supported capability bit (D28:F0/1/2/3:Offset 44h:bit [5]) set to '1,' though the Intel® 3100 Chipset does not support Extended Tags.

Implication: Software will not be able to implement Extended Tags support.

Workaround: None

Status: No Fix.



22. Intel® 3100 Chipset does not ignore a PCI Express* Null Packet on port PEB

Problem: If the Intel® 3100 Chipset receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any ACK or NAK DLLP. The Intel® 3100 Chipset still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: The Intel® 3100 Chipset port PEB may send an ACK or NAK DLLP in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None

Status: No Fix.

23. PCI Express* port PEB Link layer should drop Data Link Layer Packets (DLLPs) with unknown encoding type

Problem: A received DLLP which is not corrupt, but which uses unsupported DLLP Type encoding is discarded without further action. This is not considered an error.

Implication: If the Intel® 3100 Chipset interprets this as an NAK, a needless replay may occur. This bug violates the PCI Express specification but is not expected to cause any functional failures.

Workaround: None

Status: No Fix.

24. SATA SRST during link power states

Problem: When exiting SATA link partial or slumber states, the Intel® 3100 Chipset may not send a SRST when instructed by software.

Implication: The device will not appear to software until SRST is retried.

Workaround: Refer to the latest ICH6 BIOS Specification Update for workaround details.

Status: No Fix.

25. Unsolicited COMINIT while FIS posting pending will corrupt the FIS posting cycle

Problem: Only in AHCI mode, the SATA controller may post a FIS incorrectly if either an unsolicited COMINIT arrives or if software performs a post reset, while FIS posting is pending internally.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a production environment.

Implication: A malformed TLP is delivered and inappropriate data is delivered on the next upstream cycle.

Workaround: None. The system can be configured to detect this anomalous condition and reset the system to prevent this data migration. Refer to the latest BIOS Specification for workaround details.

Status: No Fix.

26. USB output voltage

Problem: The Intel® 3100 Chipset High Speed USB 2.0 V_{HSOL} and V_{HSOH} may not meet the USB 2.0 specification. The expected V_{HSOL} is 60 mV and the maximum expected V_{HSOH} is 470 mV.

Implication: No known implications.

Workaround: None

Status: No Fix.



27. Intel® 3100 Chipset AHCI PxCMD.CR bit

Problem: If a Task File fatal error occurs during a SATA.AHCI transfer, the Intel® 3100 Chipset will not automatically clear the PxCMD.CR bit, as required by the AHCI Specification 1.0, until the AHCI driver software follows the specification-defined recovery mechanism.

Implication: No known implications as AHCI compliant driver software will cause the Intel® 3100 Chipset to clear the CR bit during error recovery

Workaround: None

Status: No Fix.

28. Intel® 3100 Chipset PIO setup FIS error

Problem: The Intel® 3100 Chipset SATA AHCI controller may set the ERR.T and PxIS.IFS bits when a link error (such as a CRC error) or the Intel® 3100 Chipset SATA receiver error occurs on a PIO Setup FIS, instead of setting the PxIS.INFS bit, as defined by the AHCI Specification 1.0.

Implication: A spurious interrupt is generated, and the AHCI driver software will detect the error and retry.

Workaround: None

Status: No Fix.

29. Intel® 3100 Chipset PCI Express* port PEB surprise removal

Problem: After eight surprise removal or non-software initiated link-down events on a PCI Express port PEB without a platform reset, the Intel® 3100 Chipset may not be able to receive completions from the device on the PCI Express link.

Implication: The system may hang.

Note: Issue requires multiple PCI Express drives to be populated in the system with simultaneous upstream requests. Software must also de-program the PCI Express port PEB number that experienced the event before hardware is able to fully respond to the link-down condition. Known software does not de-program the surprise removal port before hardware responds. This issue has only been observed in a simulation environment.

Workaround: Perform a platform reset.

Status: No Fix.

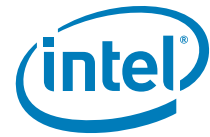
30. SATA EB buffer overflow should set ERR.E bit instead of ERR.M bit

Problem: The Intel® 3100 Chipset erroneously sets the PxSERR:[M] (Recovered Communications Error) when the internal elasticity buffer experiences an overflow or if a miss-align is detected after PhyRDY is detected. A miss-align may happen during resume from the Partial or Slumber link PM states and will cause the M-bit to be erroneously set.

Implication: As a result of M-bit setting while resuming, the host will set the Interface Non-Fatal Status (INFS) bit since it happens while the interface has no Frame Information Structure being transferred or received. INFS is expected to be recoverable by S/W (mostly ignored) and should not have an impact to subsequent command execution. No restart of the controller is needed in this case.

Workaround: None needed.

Status: No Fix.



31. PCI Express* port PEB SKP/InitFCx contention

Problem: During PCI Express port PEB initialization, if a SKP is being transmitted immediately before a InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. The device may report correctable errors. InitFCx will automatically be repeated.

Workaround: None

Status: No Fix.

32. PCI Express* port PEB downstream ports flag inbound 4 KByte memory read as malformed TLP

Problem: PCI Express downstream ports (PEB1 and PEB2) flag inbound 4 kByte memory read requests as malformed TLPs. The downstream ports will log the malformed TLP error and discard the memory read requests. This condition could occur if downstream devices can generate read request up to 4 KByte.

Implication: Inbound 4 KByte memory read request will fail, and the downstream device will lose flow control credit.

Workaround: Refer to the latest BIOS Specification for workaround details.

Status: No Fix.

33. Full Speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in the frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None. The resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not inaccessibly data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None.

Status: No Fix.

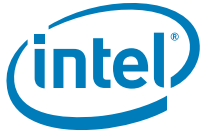
34. AHCI Host Bus Adapter (HBA) BSY bit set when recovering from fatal error

Problem: During an AHCI fatal error condition, if the device signals a Task File Error (TFES), the Intel® 3100 Chipset may not be able to recover correctly after software performs the AHCI specification-defined fatal error recovery mechanism.

Implication: The SATA port will appear busy resulting in the device being inaccessible.

Workaround: The AHCI driver should toggle the ST bit to '1' and back to '0' upon detecting TFES bit set after the ST bit is cleared.

Status: No Fix.



35. Intel® 3100 Chipset 2 Gbit refresh violation

Problem: The Intel® 3100 Chipset violates the auto refresh cycle time (T_{rfc}) specification for 2 Gbit DDR2 400 memory devices. The Intel® 3100 Chipset currently has a refresh cycle time of 27 clocks (135 ns); however, a minimum of 39 clocks (195 ns) is necessary for 2 Gbit devices.

Implication: The Intel® 3100 Chipset will not support 2 Gbit memory devices.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a production environment since reliable 2 Gbit based DIMM samples are not yet available.

Workaround: None.

Status: Fixed in A1 stepping. For the steppings affected, see the “Summary Table of Changes” table.

36. Intel® 3100 Chipset lock-up due to internal downstream EDMA and arbitration error

Problem: The Intel® 3100 Chipset will lock-up due to simultaneous downstream transactions destined to the same PCI Express port PEA link. The simultaneous downstream transactions that must occur are a FSB or Memory Read Request (MRR), an EDMA memory to PCI Express port A request, and a PCI Express port A peer-to-peer transaction. The PCI Express port A must be configured as a 2x4 or 2x1 port for this event to occur.

Implication: The FSB or MRR transaction has the highest priority and will be serviced first by the Arbiter. At the same time the Arbiter believes the EDMA request has also been serviced. Because the EDMA request was not serviced its request is still pending. The Arbiter is unaware of the pending EDMA request and the Intel® 3100 Chipset will not allow anymore requests through the system until the pending EDMA request is serviced, at this point the system hangs.

Workaround: Two workarounds are available for this erratum.

- Configure the PCI Express Port PEA as 1x8, 1x4, or 1x1.
- Disable EDMA memory to I/O transactions completely.

Status: Fixed in A1 stepping. For the steppings affected, see the “Summary Table of Changes” table.

37. System lock condition with numerous split-lock cycles on PCI Express* Port B in conjunction with Heavy PCI Express* traffic on both Port A and Port B

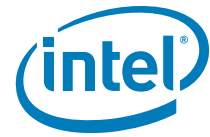
Problem: A hang condition occurs when the processor issues split-locked request (R-R-W-W) to any PCI express device on Port B combined with heavy traffic on both Port A and Port B. This issue can be noted under the following scenario:

- Downstream split-lock cycle destined to a device on Port B
- Port A sending upstream snoop and non-snoop transactions during the lock on Port B
- Port B sends upstream non-snoop requests during the lock on Port B

Implication: A hang condition occurs

Workaround: Refer to the latest BIOS Specification for workaround details. Upstream ports on PEA will always snoop the FSB with this workaround.

Status: Fixed in A1 stepping: For the steppings affected, see the “Summary Table of Changes” table.



38. PCI Express* Port PEB scrambling

Problem: While entering the recovery state, the port PEB stops scrambling two symbols before the first Training Sequence (TS).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned.

Note: There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

Workaround: None

Status: No Fix.

39. Behavior of Serial Port Interrupt Enable Register

Problem: The Serial Port Interrupt Enable Register (IER) bit 1 (Transmit Data request Interrupt Enable) will not change status if the bit has been set previously.

Implication: Will not cause an interrupt if the register bit has been set already.

Workaround: Customers may be able to implement a BIOS workaround to clear out the bit IER bit 1 to '0' before programming the bit to '1'.

Status: No Fix.

40. Intel® 3100 Chipset boundary scan operation is not guaranteed above room temperature

Problem: The integrity of boundary scan data is not guaranteed for temperatures above room temperature (~25° C TCASE).

Implication: Boundary scan operation is not guaranteed above room temperature (~ 25° C TCASE).

Workaround: Applications which use boundary scan at temperatures greater than 25° C TCASE should remove the Intel® 3100 Chipset from the chain (via the BYPASS register and/or muxing), and develop an alternate form of test coverage for the Intel® 3100 Chipset itself, if required.

Status: No Fix.

41. Potential performance/hang issue caused by incorrect default setting of FSB Retry Grace Period

Problem: For designs that use Intel® Core™ 2 Duo Processors on either 65 nm or 45 nm process combined with very slow PCIe devices connected to Intel 3100 chipset, when CPU1 is doing PCIe posted memory writes every 180ns (or faster) and CPU0 is doing periodic IO Port non-posted writes, there is a potential for too many CPU1 posted memory writes to accumulate causing the chipset internal A-UNIT buffer queue to become full.

Implication: When the chipset internal A-UNIT buffer queue becomes full, the chipset is forced to keep RETRYing the IO Port non-posted write while accepting more PCIe posted memory writes, because both CPU1 and CPU0 take turns owning the FSB. Overall, this causes increased FSB RETRY timeouts that potentially impacts overall system performance.

Workaround: The BIOS workaround involves changing the IO Retry setting from [4] to [8] (option SV > WA > IO Retry). This workaround increases the "default" setting of the FSB Retry Grace Period field (Bits 07:04 of a reserved 24-bit chipset register at Bus=0: Device=8: Function=0: offset=40h) from 40h to 80h. Increasing this default setting gives the chipset more time to free up the internal A-UNIT buffer queue, lessening the number of FSB retries.

Status: Default setting of the FSB Retry Grace Period to be fixed in a next release of BIOS.



42. PCI Express Enable No Snoop ENS register bit not behaving as specified

Problem: The PCI Express Device Control Register (Offset 6C-6Dh) includes an Enable No Snoop (Bit 11) ENS which specifies that all outbound transactions should be sent with snoop not required attribute set to 0 (i.e., all packets must be snooped at the destination). However, even though this ENS register bit is always set and read as a 0, the Intel® 3100 Chipset always sets the snoop not required attribute to 1 for all outbound transactions that are not initiated by the EDMA controller.

Implication: Cache coherency cannot be guaranteed at the destination. For example, if the endpoint is another CPU complex that is a caching agent, the CPU will not be snooped to insure the data is coherent with main memory. For PCI endpoint that is not a caching agent, there is no issue. EDMA initiated transactions are not affected by this erratum.

Workaround: For memory mapped I/O to memory transfers, system software must be responsible for maintaining system memory coherency. For memory to memory mapped I/O transfers, the EDMA controller can be used to specify the appropriate snoop non required attribute.

Status: No Fix.

43. Memory initialization may fail at low temperatures.

Problem: Some customers found that at lower temperatures the Intel® Chipset can encounter a Receive Enable Calibration Failure.

Implication: The Intel® 3100 Chipset may not detect particular DQS lanes toggling for all DLL offsets during the receive calibration at cold temps.

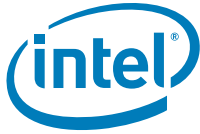
Workaround: Upgrade the Intel® 3100 Memory Reference Code to version 1.41.

Status: For the Steppings affected, see the *Summary Table of Changes*.



Specification Changes

There are no Specification Changes in this revision of the Specification Update.



Specification Clarifications

1. Access to TPM components not enabled

Issue: All Intel 3100 Chipset Development Kit User’s Manuals that are listed in Affected Documents include one TPM overview section that summarizes TPM capabilities on the Development Kit. Although TPM components exist on our platform, access to these TPM components on the LPC (Low Pin Count) bus is not currently enabled by the BIOS. A second paragraph needs to be added to this TPM section to clarify TPM capabilities, as follows:

Trusted Platform Module (TPM)

The Trusted Platform Module (TPM) is a component of the platform that is specifically designed to enhance platform security above and beyond the capabilities of today’s software. It provides protected space for key operations and other security critical tasks. Using both hardware and software, the TPM protects encryption and signature keys at their most vulnerable stages of operation, for instance, when the keys are being used in an unencrypted plain text form. The TPM is specifically designed to shield unencrypted keys and platform authentication information from software-based.

Add the following second paragraph.

Although all Development Kits include TPM hardware connected to the Intel 3100 Chipset LPC (Low Pin Count) bus, the platform BIOS does not currently support the enabling of TPM access to hardware located on the LPC. Therefore, all memory access cycles to 0xFED40000-0xFED40FFF (per Table 100 in the Intel 3100 Chipset Datasheet) are driven out on to the PCI to PCI Bridge where they are dropped. Customers need to work with their BIOS vendor to integrate and then enable the TPM feature.

Affected Docs: Intel® Pentium® M Processor on 90nm Process and Intel® 3100 Chipset Development Kit User’s Manual, Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Development Kit User’s Manual, Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset CRB User’s Manual

2. PECLK Period Discrepancies

Issue: The Intel® 3100 Chipset EDS Addendum includes two tables that contain conflicting information related to the PECLK Period specification. These two tables need to be clarified with the following updates:

Table 48 titled “PCI Express* Clock AC Characteristics” needs to have the Tabsmin symbol replaced with Tperiod-abs, and needs to include both min and max specs with the addition of new note #3 as follows:

CHANGE	Symbol	Parameter	Min	Nom	Max	Unit	Figures	Notes
FROM	Tabsmín	PECLK Period	9.872			ns	Figure 1	
TO:	Tperiod-abs	PECLK Period	9.872		10.203	ns	Figure 1	3

Note #3. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.

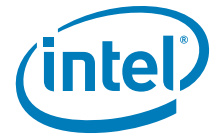


Table 49 titled “I/O Clock Timings” needs to have one header row changed as follows:

FROM: SATA Clock (SATA_CLKp, SATA_CLKn) / PEB Clock (PEB_CLKp, PEB_CLKn)

TO: SATA Clock (SATA_CLKp, SATA_CLKn)

Affected Docs: Intel® 3100 Chipset External Design Specification Addendum

3. AC Coupling when using PCIe down devices

Issue: All four Platform Design Guides for the Intel® 3100 Chipset properly introduce the requirement to use AC coupling capacitors for PCIe Transmit signals that are routed from PCI Express down devices to the PCIe Receive inputs of the Intel® 3100 Chipset. Although these AC coupling requirements are also illustrated in the first figure of the PCI Express Section 8.0, there are several figures and tables in the remainder of the PCI Express Section 8.x that are missing these AC coupling capacitors for PCIe down devices, and these figures and tables need to be clarified.

Affected Docs: Intel® Pentium® M Processor on 90 nm process and Intel® 3100 Chipset Platform Design Guide, Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide, Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform Design Guide, Intel® Core™2 Duo LV/ULV on 45 nm process and Intel® 3100 Chipset Platform Design Guide.

4. FSB Max Undershoot TYPO by a factor of 10.

Issue: Section 7.0 of the EDS Addendum specifies maximum overshoot/undershoot for the FSB in Table 62. The VUS_MAX parameter for Absolute Maximum Undershoot contains a TYPO and should be changed from -0.03V to -0.30V.

Changes	Symbol	Parameter	Max	Time Duration	Note
FROM	VUS_MAX	Absolute Maximum Overshoot	-0.03V	<1.5 ns	2
TO	VUS_MAX	Absolute Maximum Overshoot	-0.30V	<1.5 ns	2

Affected Docs: Intel® 3100 Chipset External Design Specification Addendum.

5. Clarifications to Tables in Electrical Characteristics Section of Datasheet

Issue: Tables 1104, 1107, 1108, 1110, 1111, and 1113 through 1120 in section 32.0, “Electrical Characteristics” have clarifications to be made to specific rows, as detailed below:

Table 1. Clarifications to Datasheet Tables (Sheet 1 of 3)

#	Clarification Description	Affected Table	Signal Group	Symbol	Parameter	Min	Max	Unit	Notes
1	Modify row by adding Note 7	1104	(5)	V _{CROSS(ABS)}	Absolute Crossing Point	0.250	0.550	V	2, 5, 7
1	Modify row by adding Note 7	1104	(5)	ΔV _{CROSS}	Range of Crossing Points	-	0.140	V	2, 7
2	Modify row by adding Max of 10μA	1104	(1), (2)	I _{OH_H}	Host AGTL + Output High Current	-10		μA	-
3	Modify row by adding parenthesis to Max Formula	1104	(1), (3)	V _{IL_H}	Host AGTL + Input Low Voltage	-	GTLREF - (0.10 x VTT)	V	1

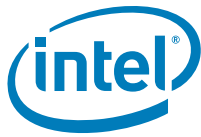


Table 1. Clarifications to Datasheet Tables (Sheet 2 of 3)

#	Clarification Description	Affected Table	Signal Group	Symbol	Parameter	Min	Max	Unit	Notes
3	Modify row by adding parenthesis to Max Formula	1104	(1), (3)	V_{IH_H}	Host AGTL + Input High Voltage	GTLREF + (0.10 x VTT)	-	-	-
5	Modify row by adding Note 9	1107	(17)	$V_{CROSS(ABS)}$	Absolute Crossing Point	0.250	0.550	V	1, 7, 9
5	Modify row by adding Note 9	1107	(17)	ΔV_{CROSS}	Range of Crossing Points	-	0.140	V	1, 9
5	Modify table by adding Note 9 to bottom of table	1107	-	-	-	-	-	-	Note 9: Guaranteed by Design
6	Add this row to the table	1108	(18)	I_{LEAK}	Leakage Current	-	10	μA	-
7	Delete this row from the table	1108	(19 ¹), (20 ¹)	I_{OH}	Output High Current	2	-	mA	-
A	Modify table by deleting Note 2 from bottom of table	1110	-	-	-	-	-	-	Note 2: Signals are 5.0V tolerant.
A	Modify row by deleting Note 2 reference	1110	(27)	V_{IL3}	Input Low Voltage	-0.5	0.8	V	2
A	Modify row by deleting Note 2 reference	1110	(27)	V_{IH3}	Input High Voltage	2.0	Vcc3)3 + 0.5	V	2
9	Add this row to the table	1110	(29)	I_{LEAK}	Leakage Current	-	10	μA	-
4	Add this row to the table	1111	(10)	I_{LEAK}	Leakage Current	-	10	μA	-
4	Add this row to the table	1111	(11)	I_{LEAK}	Leakage Current	-	10	μA	-
10	Modify 3 rows by changing all () Signal Groups to (34)	1113	From: () To: (34)	-	-	-	-	-	-
10	Add this row to the table	1113	(32), (34)	I_{LEAK}	Leakage Current	-	10	μA	-
11	Add this row to the table	1114	(35)	I_{LEAK}	Leakage Current	-	10	μA	-
11	Add this row to the table	1114	(36)	I_{LEAK}	Leakage Current	-	10	μA	-
14	Add this row to the table	1115	(40)	I_{LEAK}	Leakage Current	-	10	μA	-
15	Add this row to the table	1116	(42)	I_{LEAK}	Leakage Current	-	10	μA	-
16	Modify this row by adding Note as shown	1117	(44)	V_{IH9}	Input High Voltage	0.40	1.2	V	The 0.4V Min applies to RTCX only when clocking while chipset is in power-down state

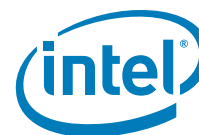


Table 1. Clarifications to Datasheet Tables (Sheet 3 of 3)

#	Clarification Description	Affected Table	Signal Group	Symbol	Parameter	Min	Max	Unit	Notes
17	Modify row by adding Note 1 reference	1117	(44)	C _L	XTAL1 typical value	6	6	pF	1
17	Modify row by adding Note 1 reference	1117	(44)	C _L	XTAL2 typical value	6	6	pF	1
17	Modify table by adding Note 1 to bottom of table	1117	-	-	-	-	-	-	Note 1: Guaranteed by Design
18	Add this row to the table	1117	(45)	I _{LEAK}	Leakage Current	-	10	μA	-
19	Add this row to the table	1118	(47)	I _{LEAK}	Leakage Current	-	10	μA	-
20	Add this row to the table	1118	(50)	I _{LEAK}	Leakage Current	-	10	μA	-
20	Add this row to the table	1118	(51)	I _{LEAK}	Leakage Current	-	10	μA	-
20	Add this row to the table	1118	(52)	I _{LEAK}	Leakage Current	-	10	μA	-
20	Add this row to the table	1118	(53)	I _{LEAK}	Leakage Current	-	10	μA	-
20	Add this row to the table	1118	(54)	I _{LEAK}	Leakage Current	-	10	μA	-
22	Add this row to the table, including reference to Note 1	1119	(55), (57)	I _{LEAK}	Leakage Current	-	10	μA	1
22	Modify table by adding Note 1 to bottom of table	1119	-	-	-	-	-	-	Note 1: The UART_CLK signal in Group 55 has Max Leakage Current of 100 μA
23	Modify this row by changing note to (3.3V < VIN < 5.0V) as shown.	1120	(58), (59)	I _{LI3}	PCI_5V Hi-Z State Data Line Leakage	-70	70	μA	1, (3.3V < VIN < 5.0V) Max VIN = 2.7 V Min VIN = 0.5 V
24	Modify this row by removing Sig Group (60)	1120	(58), (59), (60) , (61)	I _{LI2}	PCI_3V Hi-Z State Data Line Leakage	-10	10	μA	(0 V < VIN < 3.3V)
25	Add this row to the table	1120	(62)	I _{LEAK}	Leakage Current	-	10	μA	-
	END								

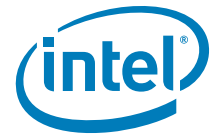
Affected Docs: Intel® 3100 Chipset Datasheet, revision 007.



6. Pairing Intel® 3100 Chipset with Intel® Core™ Duo Processor

Issue: An important reminder that platform developers must use Intel® Core™ Duo Processor production stepping D0 or newer when paired with Intel® 3100 Chipset . Additionally, it is required that BIOS vendors ensure the BIOS has Intel® Core™ Duo Processor Microcode Update M206EC54 and accompanying BIOS algorithm to enable the CPU/ chipset pairing on CPU production D0 stepping. All information has previously been made available to BIOS vendors when the platform was launched and this is a reminder to platform developers. If unsure on details, please contact your BIOS vendor.

Affected Docs: Intel® Core™ Duo Processor and Intel® Core™ Solo Processor on 65-nm Process - NDA Specification Update.



Documentation Changes

1. USB3/2 ports need to be swapped in User's Manuals

Issue: The physical location of the USB3 and USB2 Ports are incorrectly marked in some of the Intel 3100 Chipset-based Development Kit User's Manuals and should be listed as follows:

FROM:

- USB ports (2) 2 top / 3 bottom per Table 3 Component Layout Description
- USB ports (2) 2 top / 3 bottom per Figure 30 Back Panel Connectors

TO:

- USB ports (2) 3 top / 2 bottom per Table 3 Component Layout Description
- USB ports (2) 3 top / 2 bottom per Figure 30 Back Panel Connectors

Affected Docs: Intel® Pentium® M Processor on 90 nm Process and Intel® 3100 Chipset Development Kit User's Manual and Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Development Kit User's Manual