

White Paper  
**Vira Ragavassamy**  
Senior Signal Integrity  
Engineer  
Intel Corporation

# Signal Integrity Pitfalls upon deviation from Intel's SI Guidelines

January 2009



## Executive Summary

---

Intel's product Platform Design Guidelines (PDG) have SI routing rules, applicable only to one of several possible solutions. Any deviations from these rules will require a new set of simulation results.

---

This paper aims to reduce the simulation efforts by better understanding the impacts arising from deviations and focusing design efforts on these deviations.

---

Several impacts are noticed when the layer-stack up is different. It is strongly recommended to meet Intel's recommended impedance (by re-adjusting trace width) when you change Layer Stack up. However avoid trace width below 4mils to reduce skin effect loss.

Cross talk performance changes with reference plane height. Techniques are discussed to re-adjust isolation spacing for all 3 possible trace structures.

Via capacitance can change when the number of reference planes is different on your stack up. Hence re-tune via dimensions especially for interface speeds exceeding 5 Gbps. Via Stub can degrade the high frequency bandwidth of your interconnect structure. Hence when there is a Topology Change, target minimizing Via Stub.

Place the Reference Stitch Via near every high-speed differential signal (HSD) layer transition. Single Ended Interfaces have different SI challenges - minimize Skew between Data and Strobe by symmetrical routing.



# Contents

---

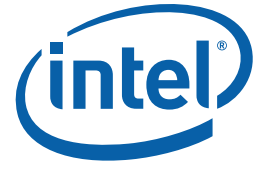
Background .....4

Solution .....4

SI Pitfalls when you deviate .....4

Summary .....17

Conclusion.....18



## ***Background***

---

Intel provides product Platform Design Guidelines (PDG) along with a fully validated Reference Board. Customers who design their boards exactly as the Reference board for any interface can use the SI Guidelines in the PDG, with no changes.

However customers working on Embedded Designs most often have to deviate from the PDG, since their designs can demand different layer stack ups or topologies, form factors etc. Hence they end up having to do their own simulations.

To design new solutions by simulation is tedious and can be very time consuming.

This document details the most often made deviations and the corresponding SI impacts to that interface.

## ***Solution***

---

This paper aims to provide an understanding of the SI impact when a deviation is made.

A thorough understanding of the SI impact can significantly help limit the simulation time by focusing only on the impact areas.

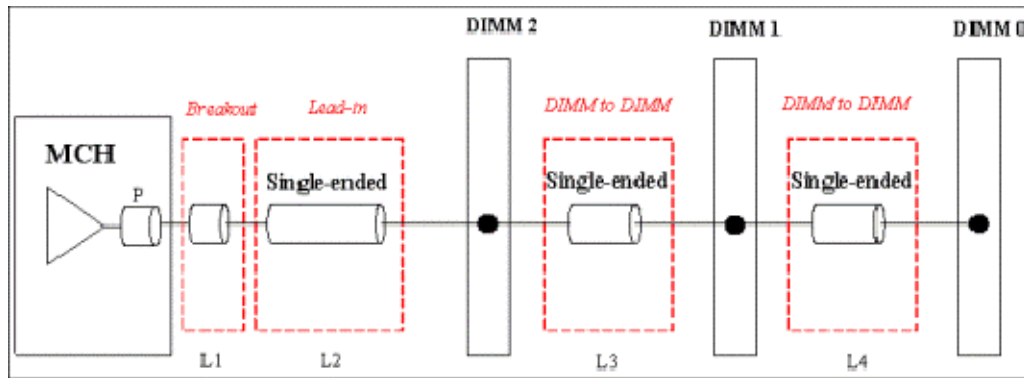
## ***SI Pitfalls upon deviation***

---

Signal Integrity Guidelines are provided as a rule for routing critical interfaces. As an example, Figure 1 shows a section of the typical DDR guidelines.



**Figure 1 Topology of a typical DDR Interface (DATA signal Group)**



The topology shows the Memory Controller Hub (MCH), traces L1 thru L4 and DIMM Connector (where DDR Memory is inserted).

The typical guidelines constrain the trace impedance, spacing to adjacent signal traces and min/max length for each segment for a given PCB Layer stack up. Additional guidelines are given for length matching etc.

Sample Guidelines for the above topology:

**Breakout Segment (L1)**

- Trace Width            4.5 mils
- Min Isolation Spacing   4 mils
- Trace Length            0-1.2 inch

**Lead-in Segment (L2)**

- Impedance Target        37  $\Omega$
- Trace Width            7.5 mils
- Min Isolation Spacing   11 mils
- Trace Length            1.75 to 5.0 inch

**DIMM Field (L3 and L4)**

- Trace Width            5.5 mils
- Min Isolation Spacing 5 mils
- Trace Length            0.4 to 0.9 inch

This guideline is one of the several possible means of achieving the goals.



## Deviations

The deviation can mean any of the rules that cannot be met and hence there is a violation of those rules. As an example, deviating from the maximum length or having only one DIMM connector on the board, instead of 3 connectors, as given in the guidelines.

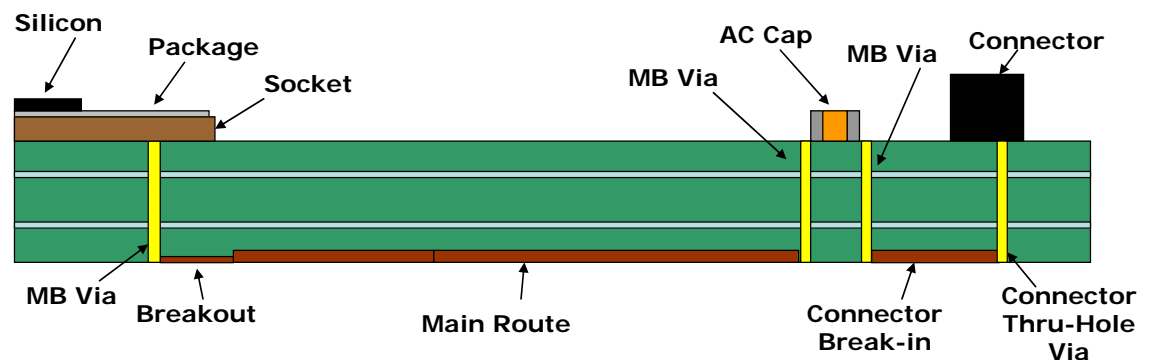
The impact of the deviation varies based on the sensitivity of the parameter to the design margin of that interface. This can be better explained by first explaining the design goals of that interface and how such a deviation will affect the design goal.

Since the design process is a little different for the High Speed Differential Interface and Single Ended Interface, they are explained separately.

## Deviations in High Speed Differential Interface

The typical topology of a High Speed Differential Interface is shown in Figure 2.

Figure 2 Topology of PCIe\* Interface with Connector



### Maximizing Length by Minimizing Losses

Signal Integrity Analysis for the High Speed Differential Interface in Intel's Design Guidelines is aimed to maximize the routing length and still meet the input electrical requirement at the Receiver. This is achieved by minimizing losses in the transmission line and the loss during signal transition, either from layer to layer or through Socket/Connector.

Three electrical phenomena that limit the maximum length are:

- Signal Loss in the PCB Trace
- Reflection, caused by Impedance discontinuities



- Cross-talk from adjacent traces

Any deviation that aggravates the above will reduce the maximum length. If your design does not route the interface for the max length specified in the design guidelines, it can probably tolerate some deviations.

**The impacts of the following deviations are discussed below:**

- 1 Deviation from -Layer Stack-up and Spacing
- 2 Deviation in Trace Impedance and Via
- 3 Topology deviation
- 4 Max, Min Length deviation

### 1. Layer Stack up and Spacing

There are 3 possible impacts that need to be taken care of, with deviations from the PDG stack up.

- a. Impedance and Trace Width Changes
- b. Dielectric Loss
- c. Isolating Spacing – re-adjust

#### a. Meet Target Impedance

Meet the Target Impedance from Intel's Guidelines by adjusting the trace width for the new Stack up. This applies to both Single Ended Impedance and Differential Impedance requirements.

A 2-D field Solver or a PCB Fabrication house can help to determine the right trace-width. This is illustrated in Figure 3 and Figure 4.

**Figure 3 Reference Stack up requires 5 mil for 48 Ohm**

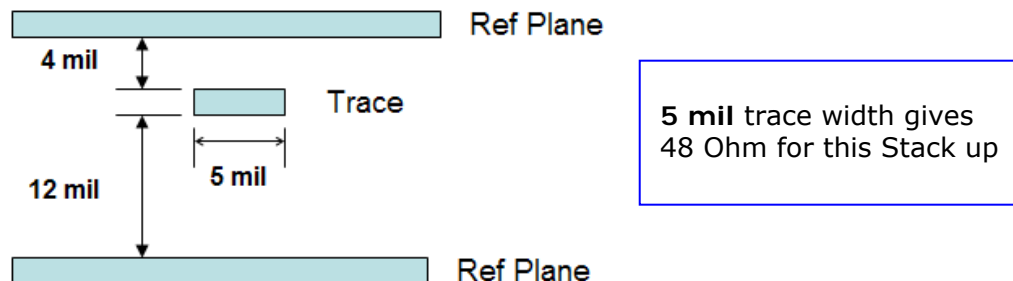
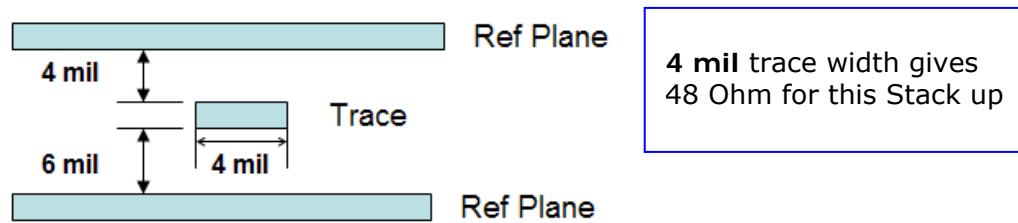




Figure 4 Example Stack up change requires 4 mil for 48 Ohm



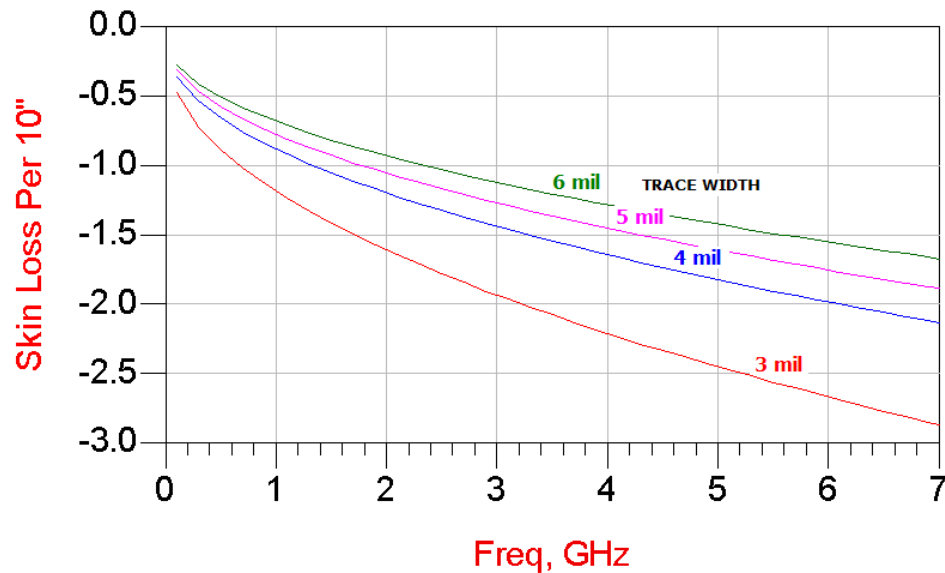
i. Loss increase from reduced Trace Width

When you increase the trace width to meet the impedance, it reduces skin loss and hence is beneficial, as long the spacing is re-adjusted.

However reducing the trace width can cause problems. It is further aggravated by the manufacturing tolerance on smaller trace widths. For example, a 0.5 mil tolerance on 3 mil trace will have a larger impact than on a 5 mil trace width.

Figure 5 shows the skin loss for various trace widths.

Figure 5 Skin Loss (in dB) as a function of trace Width – 85 Ohm Diff Impedance





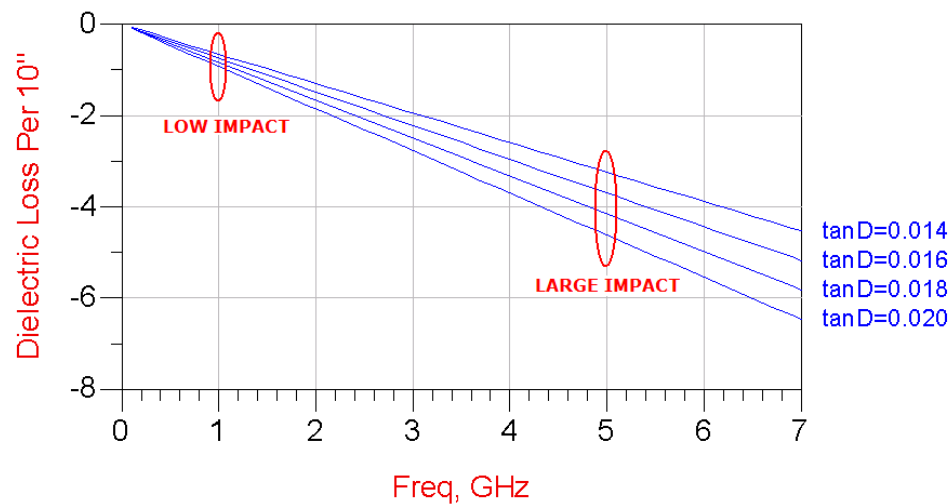
### Min Trace Width

Avoid traces width below 4 mils for HSD Interfaces to reduce loss due to skin effect

### b. Dielectric Loss

Dielectric Loss of the PCB material is another factor that can limit the maximum length of the HSD interface. The impact is higher only on high frequency. For example, PCIe\* Gen1 will have a lower impact due to dielectric loss, when compared to PCIe\* Gen2. Intel® QuickPath Interconnect, which can run at speeds of 6.4GT/S is also very sensitive to the loss-tangent.

Figure 6 Dielectric Loss (in dB) as a function of loss-tangent



### c. Isolation Spacing

Spacing is driven by two factors: Layout and Electrical. Reduced Spacing is desired for Layout to reduce layer-count. However increased Spacing is desired to limit Cross talk. Finding the right balance is the design challenge.

When your stack up deviates from Intel's Guidelines, use the space re-adjusting guidelines as a reference for Spacing rules. Although this does not guarantee similar performance, it can get close to the Reference design, covering the first order effects.



### i. Re-adjusting Spacing

Cross talk is a function of reference plane height. Cross talk increases if the reference plane height increases and vice versa. If your reference plane height is high, increase isolation spacing to get back to similar cross talk performance.

Where Intel's Guidelines recommend, spacing in terms of Reference Plane height, the new spacing for the stack up can be calculated using the following relationship as given below.

The intra Pair Spacing of a differential pair should NOT be adjusted based on this relationship – instead it should be calculated by a 2 D field solver to get the desired impedance. Re-adjusting spacing guidelines is only for Isolation Spacing (Spacing to Aggressor Signals).

Spacing = X times "Effective Reference Plane Height", where

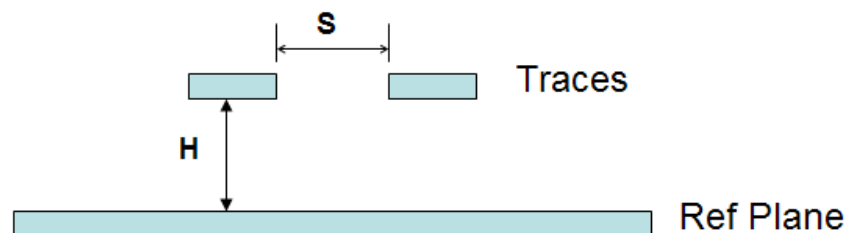
X is decided by simulation and is either available in the PDG or can be calculated from Reference Platform. Effective Reference plane height is explained below for various configurations.

### ii. Spacing for Micro strip Signals

For Micro strip traces (traces routed on the outer surface of the PCB, having only one reference Plane),

Effective Reference Plane Height = Height of Reference Plane from Signal Trace

**Figure 7 Micro strip Example – Spacing in terms of Ref Plane Height**



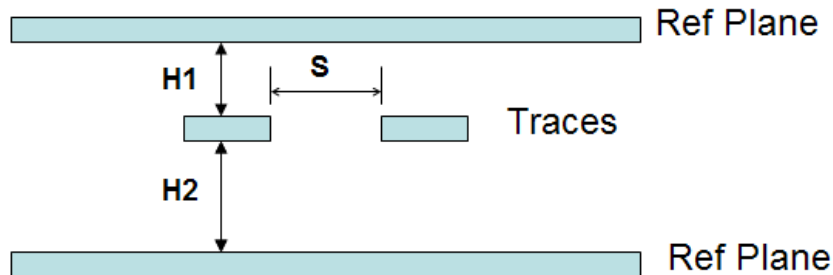


### iii. Spacing for Stripe line Signals

Strip line traces has two reference Plane heights as shown in Figure 8. When there are two variables, H1 and H2,

$$\text{Effective Reference Plane Height} = (H1.H2)/(H1+H2)$$

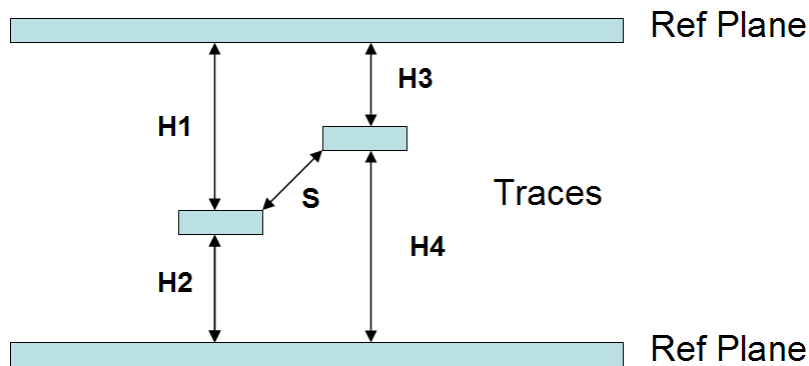
**Figure 8 Strip line Example – Spacing in terms of Ref Plane Height**



### iv. Spacing for Broad side coupled Stripe line Signals

Broad side coupled Strip line traces have four variables in the reference plane height.

**Figure 9 Broadside Strip line Example – Spacing in terms of Ref Plane Height**



Effective Reference Plane Height is given by the geometric mean of Ha and Hb.

$$\text{Effective Ref Plane Height} = \sqrt{(Ha.Hb)}, \text{ where}$$

$$Ha=(H1.H2)/(H1+H2) \text{ and}$$



$$H_b = (H_3 \cdot H_4) / (H_3 + H_4)$$

## 2. Deviation in Trace Impedance and Via

The critical factor in deciding the impedance for the HSD Interface is to minimize reflection due to impedance discontinuity.

The topology in Figure 1 gives the electrical component in the signal path.

The impedance of some components are fixed by design and the Platform designer has little influence on them:

- Connector Impedance fixed by Specification: Measured to be in the range of 80 Ohm (much lower than 100 Ohm)
- Socket Impedance fixed by the Ball/Pin Pitch and Pin Map
- Impedance of the Package Trace

A Platform designer has the following choices:

- Impedance of PCB routing
- Impedance of PCB Via

Hence trace impedances are chosen to match with rest of the components to limit reflection. This is true especially for higher speeds like PCIe Gen2, operating at 5 Gbps and beyond.

*If your design has the same components as Intel's Reference Platform, it is strongly recommended to stay with the same impedance as Intel's recommendation.*

### Via Impedance

Via becomes a critical component for the HSD interface and demands matching the impedance of the Via to the rest of the trace to maximize Eye at the Receiver.

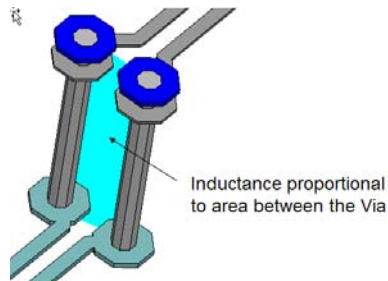
The impedance of the Via is calculated by the equation:  $Z_{via} = \sqrt{L_{via}/C_{via}}$

Inductance is proportional to the area between the Via (See Figure 10). Capacitance is given by Pad Size, Anti Pad Size, the Dielectric Constant and the number of Reference Planes. Larger Inductance of the Via increases the via impedance. Larger Capacitance reduces the impedance.

*If you deviate in any of these factors, it is recommended to re-tune dimensions to match the Via impedance.*

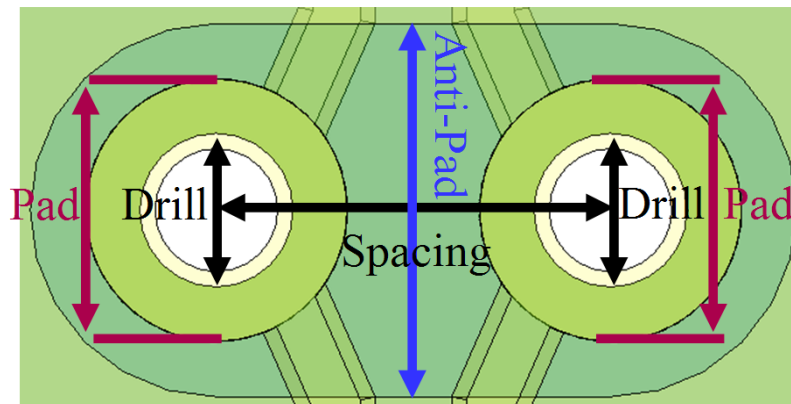
A 3-D field solver will help to compute and help to tune to the desired impedance.

**Figure 10 Inductance proportionate to area between the Via**



As an example, Figure 11 shows the via dimensions for a 4 Layer Board to achieve 80 Ohm Impedance (targeted for PCIe Gen2).

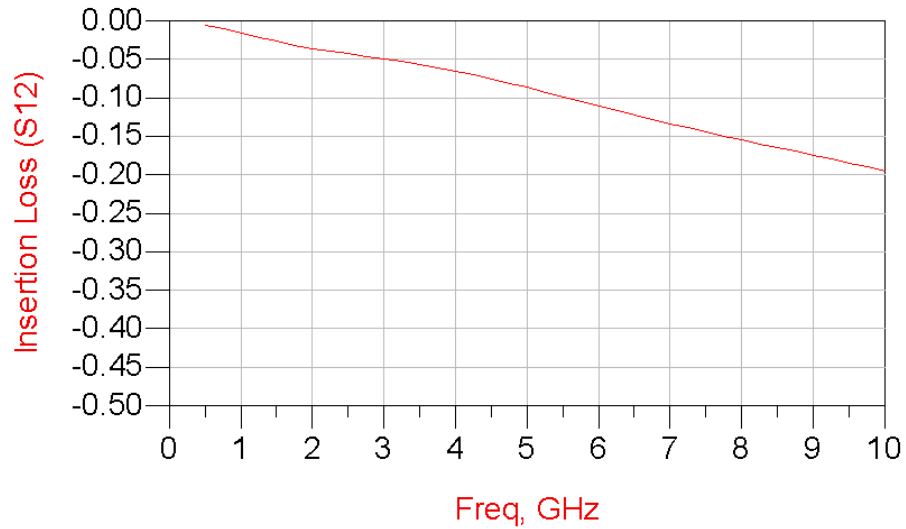
**Figure 11 Via dimension for 80 Ohm Impedance on a 4 Layer Board**



- Drill size = 14mils
- Pad size = 22mils
- Anti-Pad size = 32mils
- Pair center-to-center spacing = 36mils



Figure 12 Performance of an example Via, designed for 80 Ohm

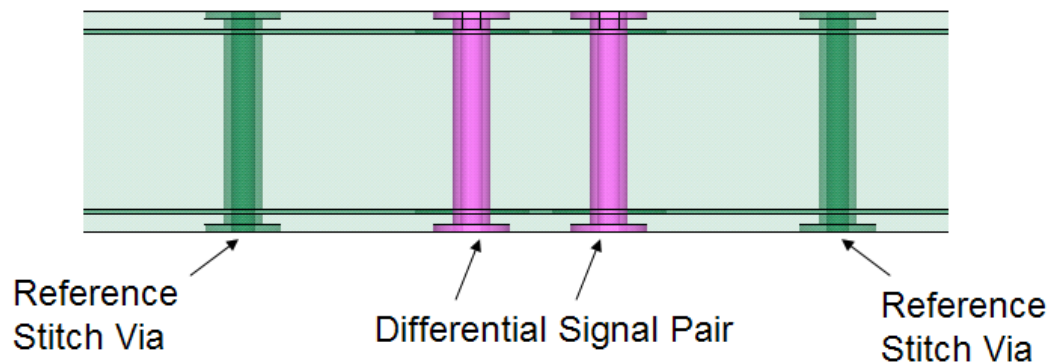


The extremely low loss even at 10 GHz shows how well a Via can be designed for a 4 Layer board.

Another note around via is to keep a Reference Stitching Via, next to the Signal trace, connecting the reference planes together. This provides a good common Mode Return Path and prevents radiation due to loop currents.

*The impact of this deviation may not be obvious in simulation, unless 3 pairs are modeled, but does reflect in the Platform performance.*

Figure 13 Reference Stitch Via for a Differential Signal Pair

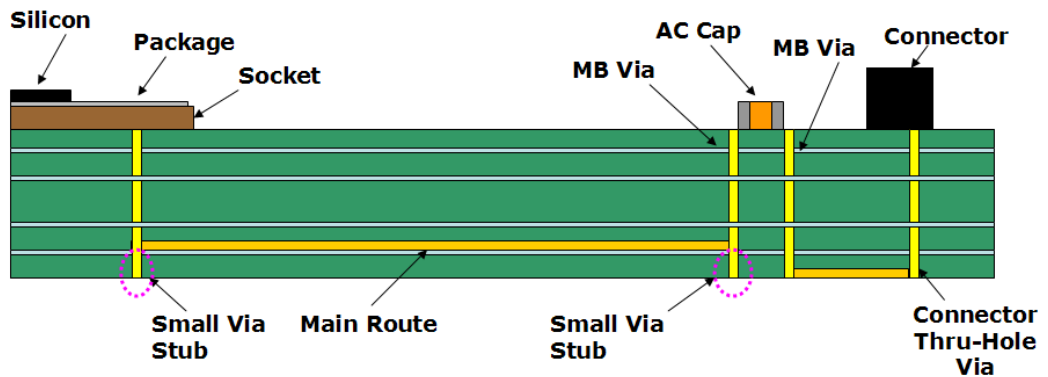




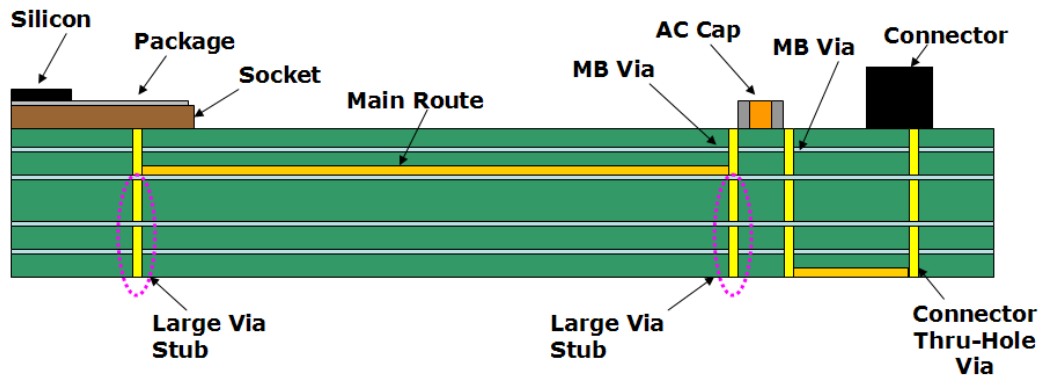
### 3. Topology Deviation

The topology or routing layer for an HSD Interface should be decided to minimize Via stub. It acts like a shunt capacitance at the junction. One of its effects is to reduce the impedance of the via. Figure 14 and Figure 15 show why a proper choice in routing layer is important.

**Figure 14 Good Choice of Routing Layer that Minimized Stub**



**Figure 15 Poor Choice of Routing Layer can cause a Large Via Stub**



#### Reduce Via Stub

When you choose the Topology, choose to minimize Via Stub



#### 4. Min, Max Length Deviation

Violating Min length may cause two major issues at FAST PVT corners (Fast Silicon Process, High Voltage and Low Temperature): Overshoot and Undershoot at the Receiver and High Slew Rate at the Receiver.

Intel's Guidelines are designed for maximizing length for the given assumptions. You can exceed the maximum length by redesigning the channel to mitigate the effects from the following factors:

- Signal Loss in the PCB Trace
- Reflection, caused by Impedance discontinuities
- Cross-talk from adjacent traces

*Doing a simulation to validate that your re-design can support the extended length is strongly recommended.*

## Deviations in Single Ended Interfaces

The impact of deviations in a Single Ended interface can be better explained by taking DDR interface as an example.

The main challenges in the DDR interface are:

- manage Cross talk by separation
- limit Inter-Symbol-Interference – reducing flight time delta
- manage skew between Data and Strobe and
- manage reflection by optimized Termination

Insertion Loss either in traces or transition is not a primary concern as in the HSD interface, since routing lengths are much shorter than the HSD interfaces. Also the multi drop nature of the bus aggravates other Signal Integrity issues than the resistive or dielectric loss.

**The impacts of the following deviations are discussed below:**

- 1 Layer Stack-up and Spacing deviation
- 2 Topology deviation
- 3 Termination deviation

#### 1. Layer Stack up and Spacing

As long as all other recommendations are followed without change, this deviation is a low risk. Single Ended impedance and spacing must be



adjusted to the new stack up. Refer the corresponding section on the HSD interface, for more details.

Meeting Single Ended Impedance is important for differential Signals (both Data Strobe and Clock), even if you violate the differential impedance requirement. However the pair should be routed together, with close enough spacing, as recommended.

## 2. Topology Deviation

*Managing Skew between Data and Strobe:*

When you deviate from the recommended topology, make sure to route Data and Data-Strobe symmetrically enough to reduce the skew between them. This includes routing on same layers and making transitions (via) together. The impact of the deviation should be simulated to find the actual margin.

### Termination Deviation

On Die Terminations are decided to meet both Eye Height and Eye Width across Silicon PVT Corners. Any deviation from the recommendation should be optimized for all Manufacturing variations.

## Summary

---

When there is a Stack up deviation:

- Meet target impedance by adjusting trace width. Reducing below 4 mil trace increases the Skin loss significantly and hence could reduce the max length
- Re-adjust isolation spacing
- Re-tune via impedance to match the impedance of your trace

When there is a topology change

- Minimize Via stub

Always target Intel's recommended trace impedance

Place Reference Stitch Via near every HSD Interface layer transition

Minimize Skew between Data and Strobe in Single Ended interfaces



## ***Conclusion***

---

Customers in the embedded areas have to more often deviate from Intel Signal Integrity guidelines, due to a variety of possible application and form factors.

This paper provides an understanding of the impact of the deviations. This can help to understand the risk and focus on the simulation efforts around the impact area, thus reducing significant simulation efforts. The result section above summarized all the key messages.

Intel plans to provide support with more guidelines on tuning Via Impedance for different stack-ups, as this has been found to be the most challenging for customers and gets a large return for the tuning efforts.



### Author

**Vira Ragavassamy** is a Senior Signal Integrity Engineer with Embedded Communications Group at Intel Corporation

### Acronyms

DDR Dual Data Rate (Memory)  
HSD High Speed Differential (Interface)  
PCB Printed Circuit Board  
PDG Platform Design Guidelines  
PVT Process Voltage and Temperature  
SI Signal Integrity

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

This paper is for informational purposes only. THIS DOCUMENT IS PROVIDED "AS IS" WITH NO WARRANTIES WHATSOEVER, INCLUDING ANY WARRANTY OF MERCHANTABILITY, NONINFRINGEMENT, FITNESS FOR ANY PARTICULAR PURPOSE, OR ANY WARRANTY OTHERWISE ARISING OUT OF ANY PROPOSAL, SPECIFICATION OR SAMPLE. Intel disclaims all liability, including liability for infringement of any proprietary rights, relating to use of information in this specification. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted herein.

Intel, the Intel logo, Intel. leap ahead. and Intel. Leap ahead. logo, are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2009 Intel Corporation. All rights reserved.