White Paper

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DDR Signal Integrity Simulation Process for Intel® Architecture Platforms

Explaining SI goals and approaches for this complex interface

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Executive Summary

SI Engineers providing solutions for the DDR Interface encounter several challenges to deliver a high confidence result, due to the complexity of the interface.

Intel® Architecture is integrated with several powerful Memory Controller Hub features to mitigate the SI Engineers' difficulties. Optimized drive strength, slew rate, Stable Power Integrity Solution, dynamic output and input timing adjustments for varying loads are a few examples of these features.

To take best advantage of these features, an SI Engineer has to have a thorough understanding of the interface and solid simulation strategies..

This white paper covers the Simulation Goals, Preparation stage with Layout Engineers, System Architects and Specification extraction. A Simplified Timing Analysis approach is also covered with examples for DATA and COMMAND Signal Group. In Simulation Steps, the importance of validating each model is emphasized to save debug time. Several low level questions are answered based on frequently asked questions.

Finally the constraints are documented in a simplified way for a layout engineer.

Contents

Business Challenges

Deviations in Guidelines: Intel delivers a fully validated Platform and Platform Design Guidelines for customers. This guideline can be used without any change, if no deviation is made. However, where significant deviations are made, customers have to do their own SI simulation.

Signal Integrity for DDR Interface is complex: It is complex due to several signal groups and topologies involved, several inter-related timings to be solved, finding optimized terminations, impedances for every configuration etc. It is similar to solving 4 or 5 separate interfaces. It gets additionally complex with increasing speed, demanding further expertise of handling the challenges that were unique to High Speed Differential Interface in the past.

Product launch time: The interface complexity takes proportionate effort and time to solve. Any failures in the lab can make matters worse. This could seriously affect the product launch time. Hence every effort should be taken to solve it right the first time.

Solution

Solution from Intel® architecture: Intel's Memory Controller Hub integrates both Hardware and Software features that are designed based on extensive simulation and validation efforts. Examples are optimized Drive Strength to deliver Stable Output Waveform for varying loads, Optimized "On Die Termination" to reduce reflection on the input Signals, Delay Strobe with respect to Data to adjust timings based on variations from board, temperature, Memory Configuration are the few.

These features help make the platform stable and reduce the simulation complexity for SI engineers.

A number of standard documents are available that give developers a general overview of this interface.

This document covers the low level information that is helpful for an SI Engineer -, from an overview to details starting with the preparatory stage and all the way through the entire simulation.

Timing Analysis - what is perceived as complex is simplified with examples and several time saving tips.

Documenting Layout Guidelines is presented by an Intel Layout Engineer's hands on experience.

DDR Signal Integrity Analysis

Overview of DDR Interface

DDR Signal Groups

There are 4 major Signal Groups in the DDR Memory Interface.

1. **Source Synchronous Signals [Data Signals]**

   Data Bus [DQ], ECC Check bits, Data Mask

   One Data Strobe [DQS] for every 8 or 4 bits of Data [DQ]

2. **Source Clocked Signals [Command and Control Signals]**

   Memory Address, Bank Address, Row Address Select, Column Address Select, Write Enable, Memory Address and Command Odd Parity (DDR3 only), Clock Enable, Chip Select, On Die Termination

3. **Differential Clocks**

4. **Miscellaneous Signals**

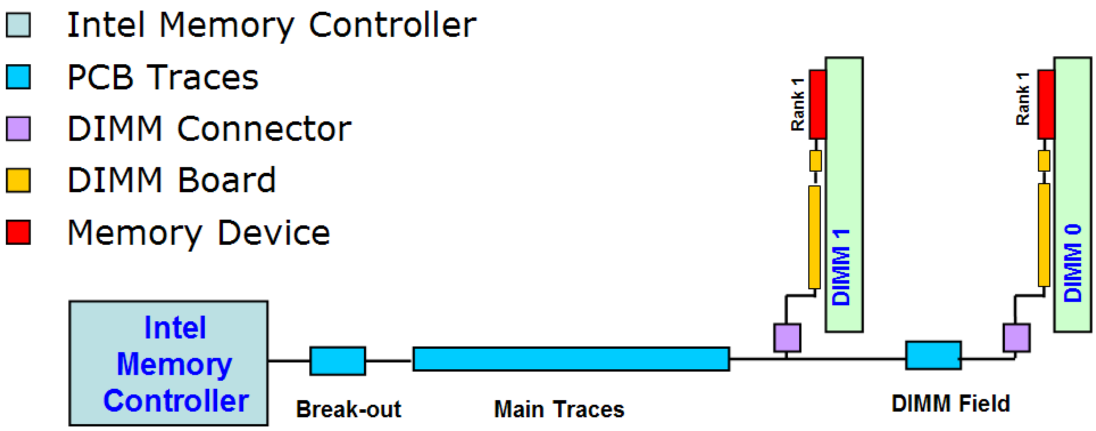
   Compensation Resistor Inputs, Reset

   Parity Error Detected by DIMM (DDR3 only)

Key components in DDR Implementation

There are 5 key components in a typical DDR Implementation, as shown in Figure 1.

Figure 1. Five Key Components in DDR Implementation



Simulation Output Goal

An SI Engineer targets to solve the following 3 key variables to meet the electrical requirement at the receiver:

1. Trace Impedance and Spacing for each Signal Group

Single Ended Impedance for COMMAND, CONTROL and DATA

Differential Spacing/Impedance for DQS and CLK

2. Termination Values

- On Die Termination [ODT] Values for DATA Write and DATA Read and which Devices need termination
- On Board Termination [OBT] Values for COMMAND and CONTROL signals, if needed

Note: Low Power Controllers may not support the ODT feature to save System Power

3. Min/Max Lengths and Length Matching

Min, Max length for all the Signal Groups

Length matching between DQ to DQS; CLK to Command; CLK to Control; CLK to DQS (if needed)

Simulation Preparation

Layout Preference and Constraints

The final solution space for DDR SI analysis is heavily driven by the routing possibilities. Hence it is helpful to complete the routing study, before beginning simulation.

This gives an idea of the boundaries of constraints. Otherwise, the result be a simulation recommendation that is not routable.

Key data to collect *ahead* of simulation are:

- The maximum permissible trace spacing (Center to Center) allowed/preferred for each Signal Group
- Minimum and maximum Breakout Length
- Minimum and maximum total length for each signal group (Controller Pin/Ball to first DIMM)
- DIMM to DIMM distance (minimum and maximum)
- Choice of Micro strip or Strip line routing for each signal group

Platform requirements

Get the information about the supported Memory Configurations for your platform and other possible options/ trade-off, in case, if there are challenges in supporting them.

The key information to collect (from Platform Architects)

- Supported DIMM types

  Example: Single Rank, Dual Rank, Quad Rank, Raw Card A
- Supported DIMM vendors

  Example: Micron, Samsung, All Vendor Support (JEDEC)
- Preferences, if any, in loading DIMM (if more than 1 DIMM connectors supported)

  This choice is heavily driven by Simulation Results. However it is good to know early whether there is a strong preference for one or another.

  Example: Empty-Single Rank-Dual Rank or Empty-Dual Rank–Single Rank in a 3 DIMM per Channel Memory Configuration

Controller Information

Not all controllers offer all the features. For example, Controllers that are designed for Power Saving Applications practically eliminate all the internal delay circuits and hence do not adjust the output timings based on the Memory Configuration. Some do not support any On die termination to further reduce power. Hence it is important to be aware of specific Controller features before beginning simulation.

For example, if the timing relationship between STROBE and CLOCK are already covered by the hardware (Delay Circuits), software (Training algorithm in BIOS) it is possible to significantly reduce efforts in meeting the timing.

Timing Analysis to find available Timing Budget for board

Table 1 shows the 5 timing relationships between different Signal Groups to be analyzed.

Table 1. Timing Relationship in a DDR Memory System

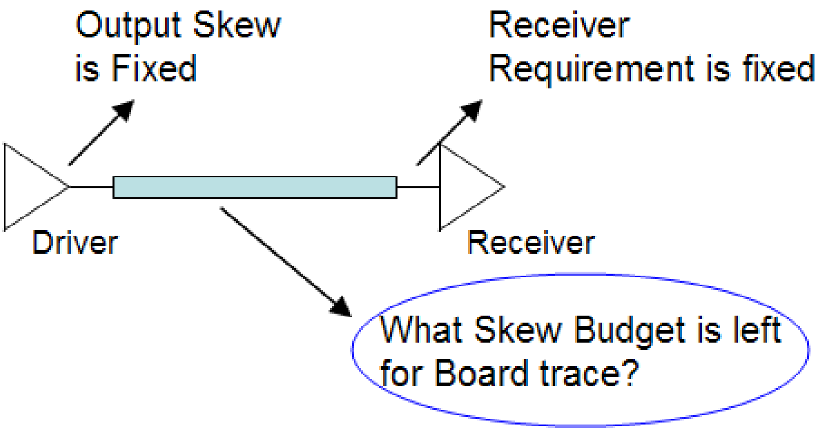
Signal Group	Timing Relation to	Note
DATA/ECC Check bit – WRITE	Associated Data STROBE (DQS) – WRITE	Most Critical (Usually Low Margin)
DATA/ECC Check bit – READ	Associated Data STROBE (DQS) – READ	
Command	CLOCK	
Control	CLOCK	
Data Strobe (DQS)	CLOCK	

Correspondingly, there are 5 simulation topologies for each row in Table 1.

The first step in Timing Analysis is to compile the timing requirements from the data sheet provided by Intel and the Memory JEDEC standard for the memories that will be supported.

The second step is to determine the Timing Budget left for board analysis. It is then easier to analyze the skew contribution from the board and compare it to the available budget to calculate the margin.

Figure 2. Calculating Interconnect Timing Budget



Timing analysis

JEDEC has a lot of timing information in it. Extract the one applicable to SI Engineers. This helps to get the Interconnect Budget. Examples follow to simplify this process.

Note: The flight time calculated by simulation should be de-rated for slew rates, based on the JEDEC spec.

Example 1: Timing for DATA TO its Associated STROBE – WRITE

The timing analysis for DATA Write Timings are simper than other timings, but usually difficult to meet, due to the low available margin.

There are two specs to get from Memory Controller Hub Data Sheet (tVB and tVA) and two from JEDEC (tDS and tDH).

Table 2. DATA to STROBE for WRITE (DDR2-667 example)

DATA Write Budget	Setup	Hold	Symbol	Note
Memory Controller Hub (Output) Driver Skew (Source: MCH Data Sheet)	400 ps	400 ps	tVB, tVA	1
Memory Input (Source: JEDEC) Receiver Requirement	100 ps	175 ps	tDS, tDH	
Interconnect Budget (Calculated)	300 ps	225 ps		

Note 1: Given as an example. Replace with the Spec from your Controller

Interconnect Budget is calculated by subtracting the Input Requirement from the Available Valid Output. Hence it is “tVB-tDS” for Setup and “tVA – tDH” for Hold.

This equation is applicable to all Memory Configurations.

Example 2: Timing for DATA TO its Associated STROBE – READ

Read Timings are a little more complex than Write Timings. There are 2 timings to extract from Memory Controller Hub data sheet (tSUMCH and tHDMCH) and 4 from JEDEC Spec (tHP, tDQSQ, tQHS and tQH).

Table 3. DATA to STROBE - READ (DDR2-667 Example)

DATA READ Budget	Setup Skew	Symbol	Note
Memory Controller Hub (Input)			
Data Input SETUP Time to Strobe Crossing	- 510 ps	tSUMCH	1
Data Input HOLD time after Strobe Crossing	990 ps	tHDMCH	1
INPUT REQUIRED WINDOW	480 ps		tSUMCH+tHDMCH
Memory Output (Source: JEDEC)			
CK Half Period	1350 ps	tHP	
DQS-DQ Skew for DQS and DQ	240 ps	tDQSQ	
DQ Hold Skew factor	340 ps	tQHS	
DQ/DQS Output Hold time from DQS	1010 ps	tQH	tHP-tQHS
OUTPUT VALID WINDOW	770 ps		tQH-tDQSQ
Interconnect Budget	290 ps		Output Window – Input Requirement

Note 1: Given as an example. Replace with the Spec from your Controller

Interconnect Budget is calculated by subtracting the Input Requirement from the Available Valid Output. Hence it is Output Valid Window – Input Required Window.

Unlike Data WRITE Budget, READ budget is not split into Setup and Hold, since most controllers dynamically delay Strobe to best position with respect to Data.

Some Low Power Memory Controller Hubs do not adjust the Strobe delay to save Power. In such cases, the timing should be split between Setup and Hold, like the DATA Write analysis.

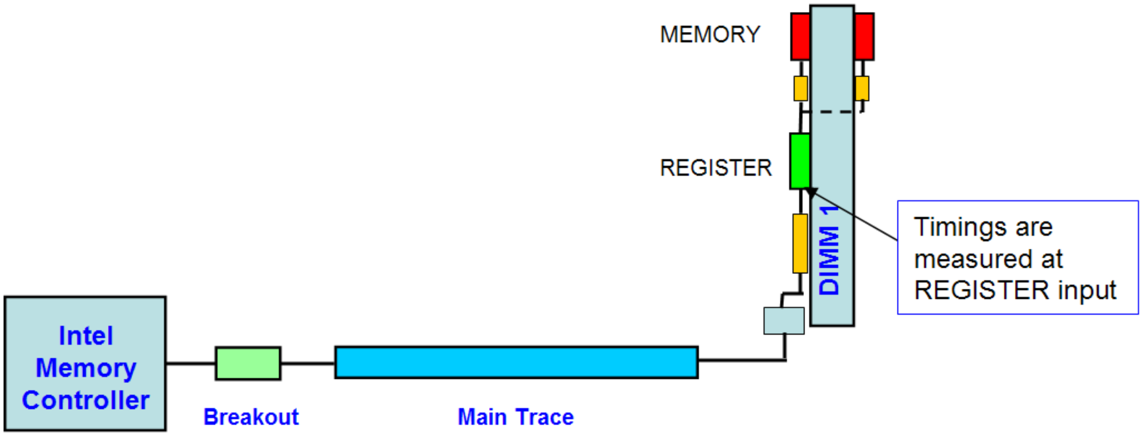
Example 3: Timing for Command/Control to CLOCK

Command/ Control Timing is similar to Data Write. However Registered DIMM timing is more complex, since the Register and Clock PLL device timings are to be considered instead of Memory Devices.

Also note that, in Registered DIMMs, Command and Control Signal Timings are measured at the input of the REGISTER devices. The timing from Output of the Register to the input of the Memory is managed by the JEDEC Spec and hence the Memory Vendor guarantees the timing beyond the register.

If you intend to analyze past registers, it is recommended to do so separately, instead of doing it with the board simulation.

Figure 3. Command/Control Timing Measurement point for RDIMM



Registered DIMM Timings

For Command and Control Timings, target to meet the Timing at Register input, instead of at Memory Input.

Table 4. COMMAND to CLOCK (DDR2-667) for RDIMM

Command Write Budget	Setup	Hold	Symbol	Note
Intel Memory Controller (Output)				
Driver Skew (Source: MCH Data Sheet)	1130 ps	1130 ps	tCVB, tCVA	1
DIMM Input (Source: JEDEC)				
DIMM PLL Jitter (RDIMM Spec)	150 ps	130 ps	tSKEW	
Register Input Requirement (Register Spec)	500 ps	500 ps	tsu, th	
NETT DIMM INPUT REQUIREMENT	650 ps	630 ps		
Interconnect Budget (Calculated)	480 ps	500 ps	Output Skew - Input Requirement	

Note 1: Given as an example. Replace with the Spec from your Controller

Interconnect Budget is calculated by subtracting the Input Requirement from the Available Valid Output. Hence it is "tCVB-NETT DIMM Setup Requirement" for Setup and "tCVA – NETT DIMM Hold Requirement" for Hold.

Timing Measurements

Interconnect Timing Skew from Simulation is calculated as:

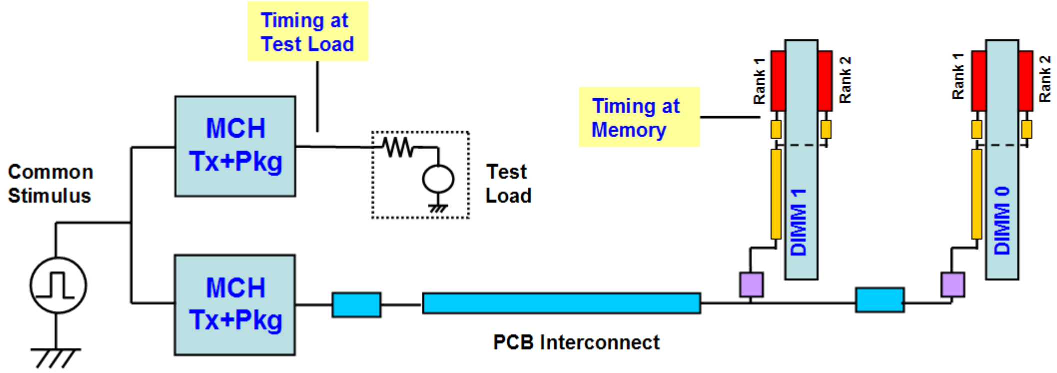
- Setup Skew = Max Flight Time of DATA/COMMAND – Min Flight time for STROBE/CLOCK
- Hold Skew = Max Flight Time of STROBE/CLOCK – Min Flight time for DATA/COMMAND

Timing Goal

Reduce Flight Time variation (Jitter) due to Interconnect.

Flight Time at Receiver is measured with respect to the Waveform at the Test Load. This is true for both for Memory Controller Hub and the Memory Device. Figure 4 illustrates the idea for the Memory Controller Hub.

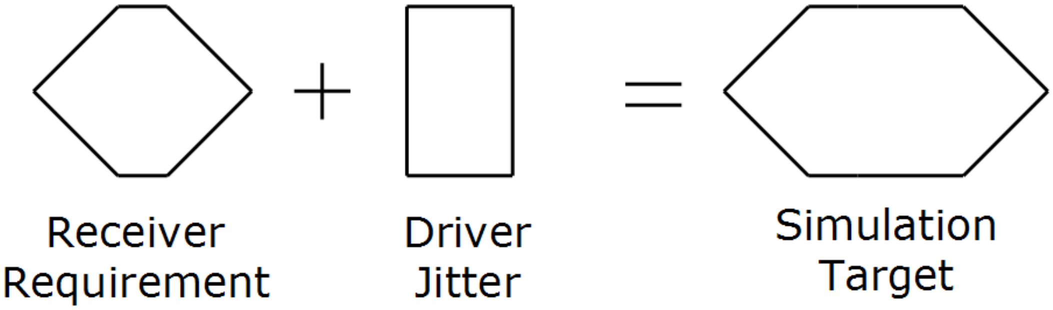
Figure 4. Simulation Topology for Timings Measurement



Add Driver Jitter to the Receiver Eye Target

If you are making eye measurements to verify timing or voltage, include Driver jitter in the eye mask. This idea is illustrated in Figure 5.

Figure 5. Including Driver Jitter in the Receiver Eye Mask



Simulation Steps

The simulations are done to ensure that the electrical specifications are met at the Receivers. The Receivers are Memory, Register or Clock PLL for Write Topologies, and Memory Controller Hub for READ.

Board routing parameters (trace width, spacing, length etc) are optimized to meet the spec requirement and at the same time to meet the layout routing constraints.

Recommended Sequence for DATA Signal Analysis

If you decide to use Intel® Recommended ODT and Trace Impedance, you can skip Steps 1 and 2.

1. ***ODT Simulation***: It is strongly recommended to stay with Intel recommended ODT Values. Refer to the BIOS reference Manual for this information. However if you choose to differ from the recommended values, do this simulation first by fixing the impedance to near the expected values. This is a coarse knob.

It is recommended to target Eye Opening (Eye Width and Eye Height), instead of trying to meet the absolute timing, in this step.

2. ***Trace Impedance:*** Fixing the identified ODT values, find the trace Impedance and spacing to maximize Eye Opening (fine tune knob).

3. **Meeting Timing:** The third simulation to meet the timing can be done, fixing the Optimized ODT and Trace Parameters. This simulation needs to verify spec compliance.

Simulation Strategy

Find variables that make the most impact (coarse control) first, then move to other variables to fine tune the results.

Dialing Coarse and Fine Knobs by separate Simulation has proved to be an efficient approach.

Recommended Sequence of Simulation for COMMAND, CONTROL Signals

1. Optimize the On Board Termination, Impedance within a desired Length in a single Simulation.
2. A second simulation to meet the timing done, using the Optimized ODT and Trace Parameter.

Preparing a Deviation List

It is important to know that the Memory Controller Hub is already proven to be functional in a platform. Make a simple list of deviation from Intel's guidelines to choose the important area of focus.

Save Simulation Efforts

If you know the deviations from Intel's guidelines, you can possibly focus your simulation there and save time.

Validating Models

It is important to validate each model separately before integrating them into your simulation deck. This can potentially save a tremendous amount of debug time later.

Keep a golden deck, (a DDR deck that is verified to produce accurate results) that you are familiar with. Insert one new model at a time into golden deck and verify whether you see the expected result.

Validating Driver Models

Find the Drive Strength and Slew Rate of the driver Model. Compare this figure against any of the previously used models to predict the trend of your results.

Validating Receiver Models

- Compare Input Capacitance of your Receiver model with your golden model.
- Compare On Die Termination Resistance Value with your golden model.

Interconnect Models, which include T-Line and Via Models

Use a standard process to generate T-Line and Via Model. Correlate the process with lab measurements periodically. PCB Fab house TDR/TDT Measurement waveforms is one way to correlate.

Validating Package and Socket Models

Check to see Insertion loss and Return Loss measurements with the termination equal to the targeted impedance (without re-normalizing to 50 ohm standard). S-Parameters looking too good at 50 Ohm impedance may not perform well, when terminated to your System Impedance. Hence always look at them with your trace termination.

Most spice simulators support generating S-Parameter Waveform directly from any Spice Circuit.

Validate Models before Simulation

Validate Models separately before you integrate them into the main deck. This can save a tremendous amount of debug time later.

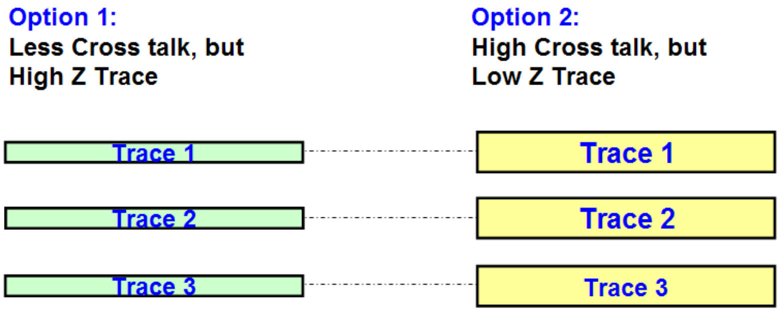
Trade-off between Impedance and Spacing

The maximum permitted center-to-center trace spacing (Pitch) comes from the layout engineer. Exceeding this may come at additional Platform cost (increasing layer count for example).

The Impedance choices for DDR DATA signal group usually trends to be low impedance (in order to drive multiple DIMM, if present).

A careful trade off (through Simulation) is made between meeting impedance (fat trace) and cross talk (more spacing between traces), given the pitch fixed.

Figure 6. Using Routing Space for Low Z or Low Cross talk



Note: Both options use almost same routing space

Documenting Layout Guidelines

Due to the increasing complexity of DDR rule sets, the importance of documenting all of the rules in a clear and concise manner is paramount.

It is recommended you have a template for documenting the rules, possibly for each DDR standard and use that approach for consistency and work with the layout engineer all through.

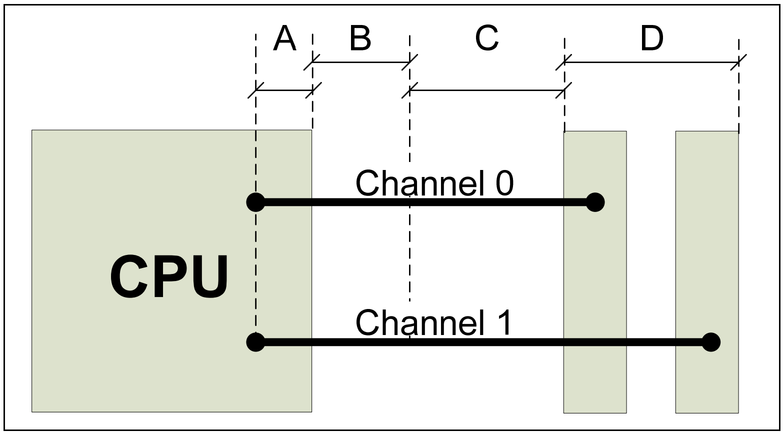
Table 5 shows a sample layout template.

Table 5. Byte Groups – sample template

Data Bits	Associated Strobes
DQ[7:0], DM0	DQS/DQS#[0,9]
DQ[15:8], DM1	DQS/DQS#[1,10]
DQ[23:16], DM2	DQS/DQS#[2,11]
DQ[31:24], DM3	DQS/DQS#[3,12]
DQ[39:32], DM4	DQS/DQS#[4,13]
DQ[47:40], DM5	DQS/DQS#[5,14]
DQ[55:48], DM6	DQS/DQS#[6,15]
DQ[63:56], DM7	DQS/DQS#[7,16]
ECC[7:0], DM8	DQS/DQS#[8,17]

The first thing to consider is which signals are to be covered. The information shown in Table 5 is a breakdown of the data byte groups. The intent is to deny the possibility of signals being overlooked so it is best to include such a guide. The same is true of the other signal groups such as command and control.

Figure 7. Signal Topology



The callouts in Figure 7 are defined as follows: A is the CPU break-out, B is the high-density area, C the open field and D is the DIMM field.

Figure 7 is a typical representation of a signal topology. Such an image provides a quick visual check to the layout engineer and should be included as it pertains to each of the following: data, command, control, clocks and parity error.

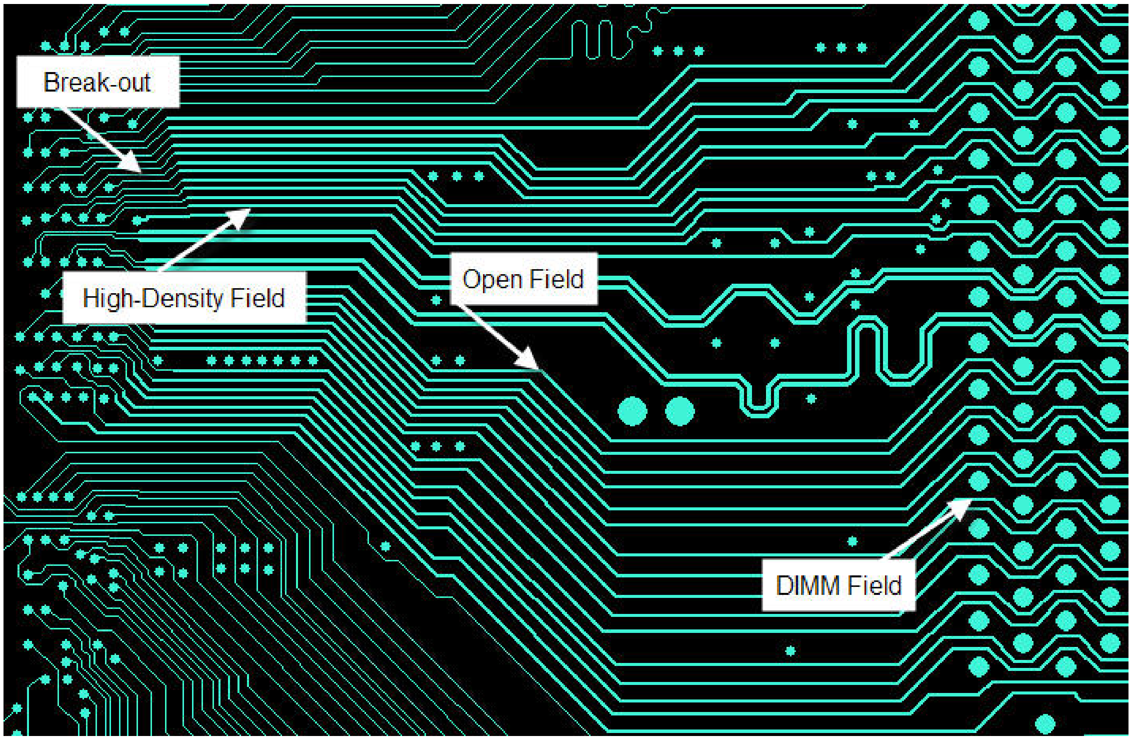
Table 6. Trace Characteristics - template

DQ[63:0], ECC[7:0]	Break-out	High-Density Field	Open Field	DIMM Field
Routing Layer	Layer x	Layer x	Layer x	Layer x
Characteristic Impedance	N/A	TBDΩ ±xx%	TBDΩ ±xx%	TBDΩ ±xx%
Trace Width	TBD mils			
Layer Transitions Allowed	TBD			
Reference Plane	TBD			

Table 6 demonstrates a means of conveying the basic characteristics of the data signals. In most cases, characteristic impedance should be used in lieu of specifying trace width if that is important to meet. The exception to this rule is within the break-out region where the physical limitations imposed by the package force a specific trace width and spacing.

The characteristic impedance should be indicative of the routing layer when multiple layer geometries are allowable.

Figure 8. Segment Identification



Trace Segments Explained

Break-out is identified as the maximum length required in order to exit the pin field and in turn expand to the desired impedance and spacing.

High-Density Field can be thought of as a slightly more constrained break-out region. In other words, the required impedance and/or spacing will likely be more restrictive in this area. Figure 8 shows how the spacing in this area is still close, yet the trace width has increased.

Open Field is the area in which the target trace impedance and spacing must be implemented. It should be noted that this is the only area that is strictly performance based whereas the other regions are constrained due to their physical limitation.

The DIMM Field begins as a trace gets to the edge of the first DIMM. The trace impedance and spacing must be adjusted once again to allow for the traces to be routed between the through-hole pin field.

Table 7. Trace Spacing - template

DQ[63:0], ECC[7:0]	Break-out	High-Density Field	Open Field	DIMM Field
Spacing: Data to Data within a byte group	xx mils	xx mils	xx mils	xx mils
Spacing: Data to Strobe within a byte group	xx mils	xx mils	xx mils	xx mils
Spacing: Byte Group to Byte Group within a channel	xx mils	xx mils	xx mils	xx mils
Spacing: Data to Data in another channel	xx mils	xx mils	xx mils	xx mils
Spacing: Data to any non-Data signal	xx mils	xx mils	xx mils	xx mils

Note: Unless otherwise specified, spacing is provided from trace edge to trace edge.

The spacing sets identified in Table 7 cover all anticipated combinations of signals that one could expect to encounter for DDR Data signals on a board layout. As noted, all relationships should be defined from trace edge to trace edge as this is the common means of setting such variables within a CAD tool.

Listing the relationships in this manner will remove the potential for uncertainty of rules.

Table 8. Length Matching Within a Channel - template

Length Matching (including package length)	
Data to strobe within a byte group	(Strobe - xx mils) ≤ Data ≤ (Strobe + xx mils)
DQS to DQS# individually within each strobe pair	Total delta ≤ xx mils
Strobe pair to strobe pair within a byte group	Total delta ≤ xx mils
Byte group to a byte group	Total delta ≤ xx mils

Note: Total delta is defined as the difference between the shortest and longest signals within a given group.

To avoid misinterpretation of length matching rules, the formats shown in Table 8 should be employed. The first match group provided, data to strobe within a byte group, uses a target which in this case is a particular strobe signal.

The second and third match groups should be setup with the first in mind. That is, regardless of the strobe chosen to be the target in the first group, the spirit of all three rules should be upheld.

Total delta is the favored means of communicating a tolerance. Using the provided format bypasses the common misconception of doubling the allowable tolerance as seen when employing the use of a plus-minus (±) symbol.

Table 9. Trace Length - Template

DQ[63:0], ECC[7:0]	Break-out	High-Density Field	Open Field	DIMM Field
Trace Length	Max = x.xxx”	Max = x.xxx”	Max = x.xxx”	Max = x.xxx”
Total Length (including package length)	x.xxx” – x.xxx”			

It should be noted that although the traces are broken up into segments which provide allowable lengths, the total length may not be a direct sum of these parts.

It is important to be aware that as with length matching, the total length rule should also be inclusive of package length. The significance of this resides within some CAD tools’ inability to utilize package length in just one of these areas at a time. In other words, package compensation is either always on or always off.

Trace Length Example

Break-out:	Max = 0.500”
High-Density Field:	Max = 0.600”
Open Field:	Max = 4.000”
DIMM Field:	Max = 1.200”

Given the above, the maximum motherboard routing is 6.300” (0.500” + 0.600” + 4.000” + 1.200”).

It is feasible however, that the largest package compensation could be 0.845”.

This package length would yield a “Total Length” of 7.145” (6.300” + 0.845”).

Summary

The document is summarized below:

Simulation Goals: All the analysis boils down to recommending trace impedance, spacing and length and length matching for each signal group. It helps during the analysis to be clear about what an SI engineer is trying to solve. Identifying the most optimized ODT values for different memory configurations is crucial. Using the values that Intel recommends is encouraged.

Simulation Preparation: It is recommended to do a routing study ahead of simulation to know the boundaries for every parameter that you are trying to solve. Otherwise, you may end up with simulation results that are not routable. It is important to be familiar with Memory Controller Hub features before simulation. This may change your focus during analysis. Do an extraction of electrical targets, both from JEDEC Standard and Memory Controller Hub Data Sheets. A simplified Timing Analysis approach is suggested with example in this white paper.

Simulation Steps: It is time efficient to split the simulation into small pieces with separate goals. Identifying and fixing the coarse variables, which have a large impact on simulation results, separate from variables that have finer impact is a good idea. A deviation list from Intel's Design Guidelines is helpful to validate the risk and concentrate on them. Validating the models is emphasized to save future debug time.

Documenting Layout Guidelines: Since there are several timing constraints, a layout engineer shows a CAD friendly documenting process.

Conclusion

Intel® Architecture is integrated with a powerful Memory Controller Hub to support several features aimed to reduce the simulation complexity. This document covers high level and low level details with examples to help SI engineers who are involved in providing routing solutions for the platform. In addition, Intel Memory Controller Hub offers a variety of features to reduce simulation complexity and produce a stable platform.

Optimized Driver: The Memory Controller Hub offers a carefully optimized Drive Strength and Slew Rate, the best possible signal quality at the Memory Input, even at the varying loads.

Optimized Receiver: Data Receiver offers an On Die Termination (ODT) to reduce reflection and improve the signal quality and timing of the received Waveforms. The Termination Resistance is chosen based on both extensive simulation and validation.

Timing Optimization: Documenting the complex simulation constraints into an easy to understand document is challenging and is covered in this paper.

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Acronyms

CAS	Column Address Selection
DIMM	Dual In-line Memory Module
EH	Eye Height
EW	Eye Width
PCB	Printed Circuit Board
RAS	Row Address Selection
RDIMM	Registered DIMM
WE	Write Enable

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