Intel® Pentium® 4 Processor-M and Intel® 845E Chipset Platform Design Guide

Addendum for Embedded Applications

April 2003

Order Number: 251319-002

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Contents

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Revision History

Date	Revision	Description
April 2003	002	Add Scalable VRD Schematic.
June 2002	001	Initial release of this document.

1.0 Introduction

This document is an addendum to the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide*. It is targeted for:

- Customers designing with the Intel® Pentium® 4 Processor-M for Applied Computing and Intel® 845E Chipset, and for
- Customers designing a scalable Intel 845E chipset platform, compatible with both the Intel Pentium 4 Processor for Applied Computing and the Intel Pentium 4 Processor-M for Applied Computing.

Designers should refer to the *Intel® Pentium® 4 Processor in 478-Pin Package and Intel® 845E Chipset Platform Design Guide* for the majority of their design. However, for any information pertinent to designing a scalable platform, or for combining the Intel Pentium 4 Processor-M with the Intel 845E chipset, designers should refer to this document. Design issues such as thermal considerations should be addressed using specific design guides or application notes for the processors or chipset, some of which are listed in Section 1.2, "Related Documents".

These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of the two categories:

- *Design Recommendations* are items based on Intel's simulations and lab experience to date and are strongly recommended, if not necessary, to meet timing and signal quality specifications.
- *Design Considerations* are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They should be used as examples, but may not be applicable to particular designs.

Note: The guidelines recommended in this document are based on experience and preliminary simulation work performed at Intel while developing the Intel Pentium 4 processor, Pentium 4 Processor-M and 845E chipset based systems. This work is ongoing, and the recommendations and considerations are subject to change.

1.1 Content Overview

Section 2.0, "Intel® Pentium® 4 Processor-M for Applied Computing Transition Guidelines" contains design guidelines and BIOS guidelines for transitioning the Intel Pentium 4 Processor-M to maximum performance mode at reset.

Section 3.0, "Voltage Regulator Design Guidelines" contains design guidelines for designing in two separate voltage regulator modules (VRMs) or a single voltage regular-down (VRD) in a scalable platform.

Appendix A, "High Frequency Transition Sample Schematic" and Appendix C, "Reference Design Schematics" are references for board designers. While the schematics may cover a specific design, the core schematics will remain the same for most platforms. The schematic set provides a reference schematic for each platform component as well as common motherboard options. The schematics also include the mobile processor transition and voltage regulator design considerations contained herein. Additional flexibility is possible through other permutations of these options and components.

1.2 Related Documents

Reference the following documents for more information. All Intel issued documentation revision numbers are subject to change, and the latest revision should be used. Contact your Intel field representative for information on how to obtain Intel issued documentation.

Table 1. Related Documentation

Related Documents	Order Number
Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide	298652
Mobile Intel® Pentium® 4 Processor - M Datasheet	250686
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 µ Process at 2 GHz, 2.20 GHz, 2.26 GHz, 2.40 GHz, and 2.53 GHz Datasheet	298643
Intel® 845E Chipset: Intel® 82845 Memory Controller Hub (MCH) for DDR Datasheet	290742
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	290744
Mobile Intel® Pentium® 4 Processor-M Thermal Design Guide for Embedded Applications	273729
Intel® Pentium® 4 Processor for Embedded Applications Thermal Design Guide	273704
VRM 9.0 DC-DC Converter Design Guidelines	249205
Intel® Pentium® 4 Processor VR-Down Design Guidelines	249891

Please refer to the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide* for the most complete, up-to-date list of related documentation.

1.3 Conventions and Terminology

This section defines conventions and terminology that are used throughout this document.

Table 2. Conventions and Terminology

Convention/Terminology	Definition
Intel® Pentium® 4 Processor-M for Applied Computing; mobile processor	This part is identical to the Mobile Intel® Pentium® 4 Processor-M.
Intel® Pentium® 4 Processor for Applied Computing; desktop processor, or processor	This part is identical to the Intel® Pentium® 4 Processor.
Chipset	Intel® 845E Chipset
Scalable	As in “scalable platform”, “scalable board”, etc. Used to describe a system that is designed to accommodate either the Intel Pentium 4 processor or the Intel Pentium 4 Processor-M.
MPM	Maximum Performance Mode (enhanced Intel® SpeedStep® technology mode)
BOM	Battery Optimized Mode (enhanced Intel SpeedStep technology mode)
VID	Voltage Identification
VRD	Voltage Regulator-Down
VRM	Voltage Regulator Module

2.0 Intel® Pentium® 4 Processor-M for Applied Computing Transition Guidelines

This section contains design guidelines for transitioning the Intel® Pentium® 4 Processor-M for Applied Computing to maximum performance mode at reset.

2.1 Background

The Mobile Intel Pentium 4 Processor-M features enhanced Intel SpeedStep® technology, which allows the processor to switch between two core frequencies. The mobile processor operates in two modes, the high frequency Maximum Performance Mode (MPM) or the low frequency Battery Optimized Mode (BOM). By default, the mobile processor will boot to the lower frequency. Certain mobile chipsets, such as the mobile Intel® 845MZ or 845MP chipset, can control the transition between the two modes; however, the Intel® 845E chipset is not capable of controlling the transition. Therefore, when designing a system based on the Intel 845E chipset, additional logic is required to transition the mobile processor from BOM to MPM.

The design guidelines in this section should be used for Intel Pentium 4 Processor-M / Intel 845E chipset based platforms, as well as for scalable platforms. The BIOS guidelines provided in Section 2.5, “BIOS Enabling” specify provisions for detecting the presence of either a desktop processor or mobile processor, and only initiating transition sequence when a mobile processor is present.

Note: The Embedded Intel Architecture Group, which supports the combination of the Intel Pentium 4 Processor-M for Applied Computing and Intel 845E Chipset, does not provide full support for enhanced Intel SpeedStep technology. The only supported aspect of this feature is the transition from battery optimized mode to maximum performance mode at reset. Designers are encouraged to follow the guidelines in this document to ensure proper product support.

2.2 Enabling the Mobile Processor Transition

Figure 1 depicts a block diagram for enabling the transition of the mobile processor from BOM to MPM. The additional logic, external to the processor and chipset, required to accomplish this transition is depicted as the shaded block labeled External Logic.

Figure 1. Mobile Processor Transition Block Diagram

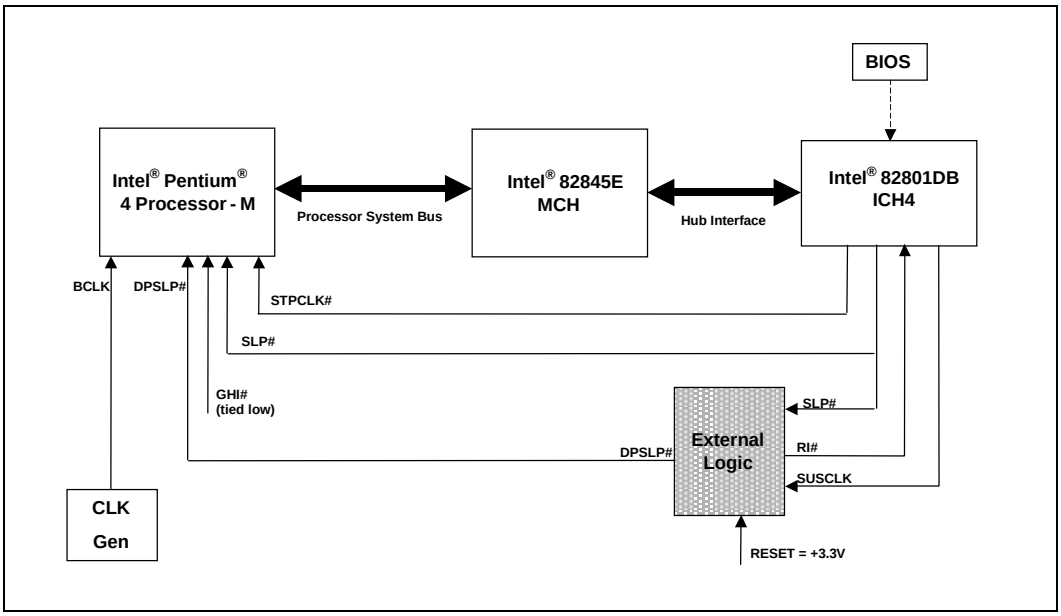


Table 3 explains the various signals involved with the mobile processor transition. Additional details on these signals and the transition sequence follow in later sections.

Table 3. Frequency Transition Signal Overview (Sheet 1 of 2)

Signal	Component(s)/Pin(s)	Definition/Usage
GHI#	CPU (pin A6)	At the transition, GHI# is sampled to determine the mode of the processor. GHI# high = Battery Optimized Mode; GHI# low = Maximum Performance Mode. GHI# must be tied low to correctly transition to MPM. (On the desktop processor, pin A6 is called TESTHI11.)
STPCLK#	CPU (pin Y4) ICH4 (ball V23)	After the BIOS initiates the process, the ICH4 asserts this signal. As a result, the CPU enters Stop Grant state.
SLP# / CPUSLP#	CPU (SLP#, pin AB26) ICH4 (CPUSLP#, ball U21) External logic input	After the CPU is in Stop Grant state, the ICH4 asserts SLP#. As a result, the CPU enters Sleep state. The external logic intercepts this signal as a trigger to continue the transition sequence.
DPSLP#	CPU (AD25) External logic output	After the CPU is in Sleep state, the external logic asserts DPSLP#. As a result, the CPU enters Deep Sleep state. After a specified length of time, the external logic de-asserts DPSLP# and the CPU re-enters Sleep state. (On the desktop processor, pin AD25 is called TESTHI12.)

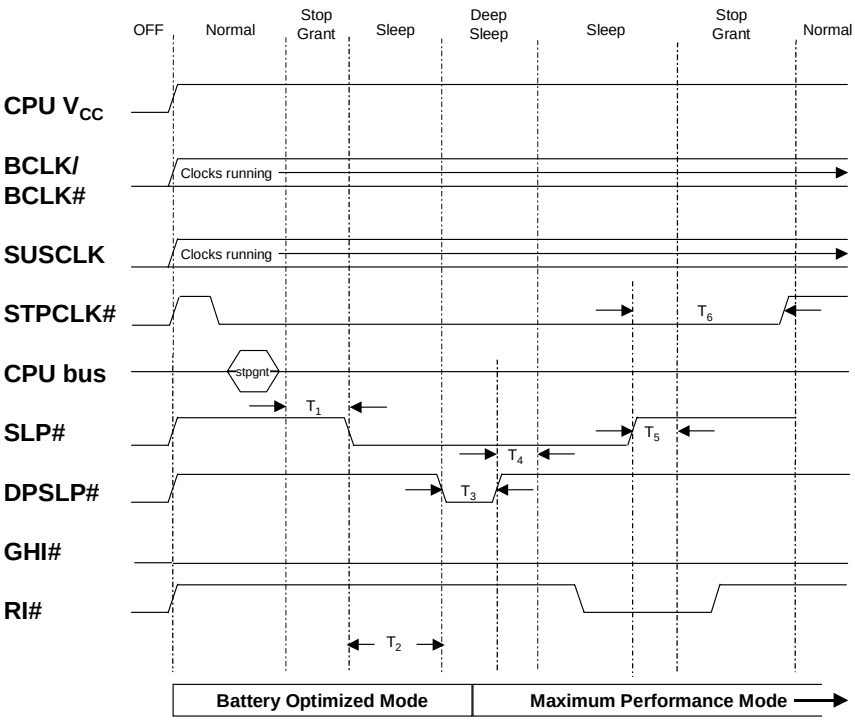
Table 3. Frequency Transition Signal Overview (Sheet 2 of 2)

Signal	Component(s)/Pin(s)	Definition/Usage
RI#	ICH4 (ball Y1) External logic output	The external logic asserts RI# (ring indicator) to wake the ICH4. From that point, the ICH4 controls the return of the system to Normal state.
SUSCLK	ICH4 (ball AA4) External logic input	This is the 32.7 KHz clock used to synchronize the external logic.
BCLK	CPU (pins AF22, AF23) Clock generator	The differential BCLK (bus clock) determines the system bus frequency.

2.3 Frequency Transition Sequence

Figure 2 depicts the timing diagram for the mobile processor frequency transition sequence from BOM to MPM.

Figure 2. Transition Sequence Timing Diagram



The steps in the mobile processor frequency transition sequence are as follows:

1. **From Normal to Stop Grant** (in-sync with BCLK) – The BIOS enables S1 sleep state. The ICH4 asserts STPCLK#, which causes the processor to initiate a special bus cycle, Stop Grant Acknowledge. 20 BCLKs after the response phase of Stop Grant Acknowledge, the processor enters Stop Grant state.
2. **From Stop Grant to Sleep** (in-sync with BCLK) – The ICH4 asserts SLP#, which places the processor in Sleep state. SLP# is also an input to the external transition logic, and the assertion

of SLP# triggers the transition logic to begin its execution. Note that the external logic is synchronized with SUSCLK.

3. **From Sleep to Deep Sleep and back to Sleep** (in-sync with SUSCLK) – The external logic asserts DPSLP# after T2. After T3, the external logic deasserts DPSLP#. The system enters Sleep state after T4. Because GHI# is tied low, the mobile processor will transition to MPM and the high frequency.
4. **From Sleep to Stop Grant** (in-sync with SUSCLK, BCLK) – The external logic asserts RI# (ring indicator) to the ICH4, which will take over from here for the wake portion of the sequence. The external logic deasserts RI# in the next SUSCLK cycle. The ICH4 deasserts SLP#, and after T5, the system enters Stop Grant state.
5. **From Stop Grant to Normal** (in-sync with BCLK) – The ICH4 deasserts STPCLK#, and the system enters Normal state.

Table 4 provides timing details for the timings noted in Figure 2.

Table 4. Timing Details

T#	Description	Min	Max	Unit
T1	Input signals stable to SLP# assertion requirement	10		BCLKs
T2	SLP# to DPSLP# assertion	10		BCLKs
T3	DPSLP# hold time	1		BCLKs
T4	Deep Sleep PLL lock latency, time required to enter Sleep state after DPSLP# has been deasserted. External logic can assert RI# anytime after this.	0	30	us
T5	Input signal hold time from SLP# deassertion, time required to enter Stop Grant state after SLP has been deasserted	10		BCLKs
T6	STPCLK# hold time from SLP# deassertion	10		BCLKs

Note: To avoid compromising signal integrity, the DPSLP# input to the CPU must not sink more than 4mA. In the schematic in Appendix A, "High Frequency Transition Sample Schematic", the values of resistors R4 and R6 must be selected to properly translate the voltage of this signal, while meeting this sink requirement.

2.4 External Logic

System designers must select hardware to fulfill the requirements of the external logic, as stated above. The external logic must accommodate three inputs (SLP#, RESET, SUSCLK) and two outputs (DPSLP#, RI#). Designers may select a PLD, FPGA, or other logic device of their choice and use the state diagram in Figure 3, the simulation timing diagram in Figure 4, and logic diagram and equations shown in Figure 5.

Figure 3. External Logic State Diagram

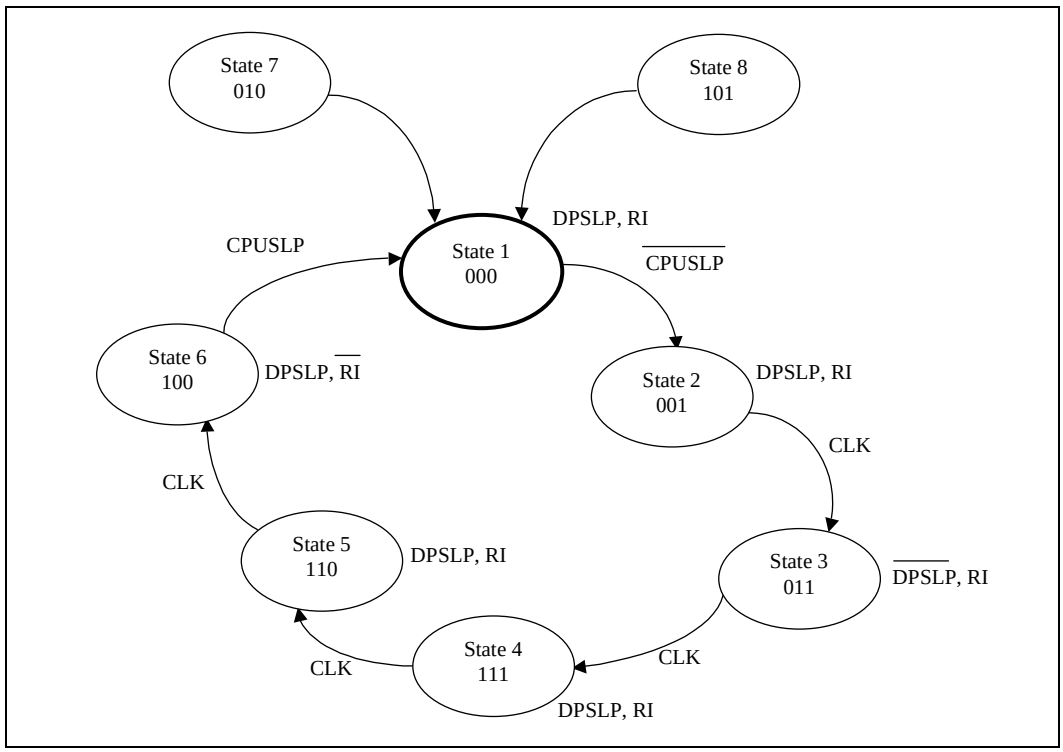


Figure 4. External Logic Timing Diagram

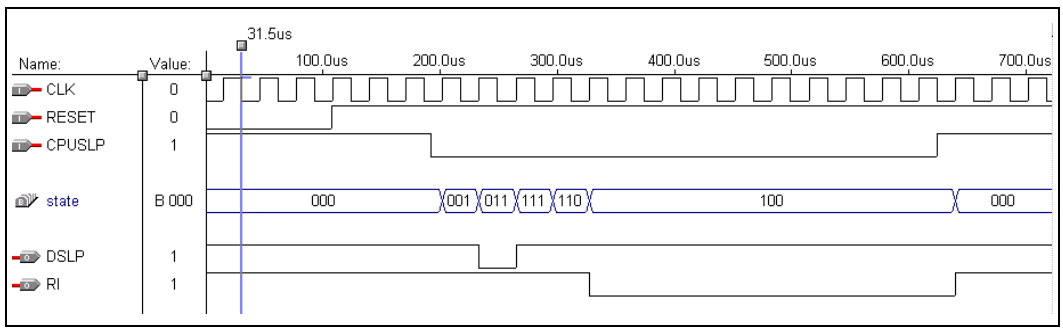
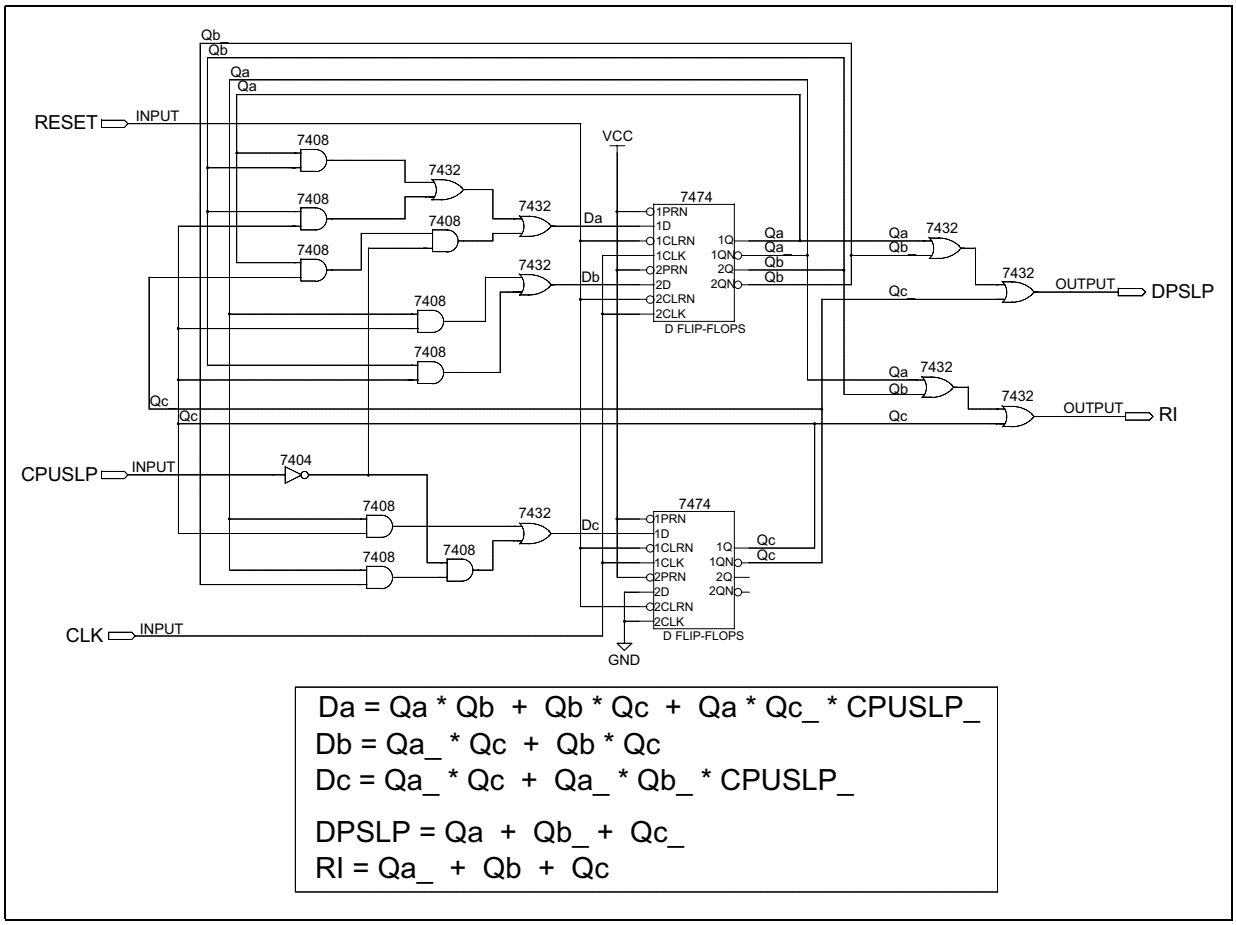


Figure 5. External Logic Diagram



In addition, designers may utilize the following VHDL code to program their external logic device:

```
library ieee;
use ieee.std_logic_1164.all;
entity speed_transition is port(
    clk, rst:   in std_logic;
    cpuslp:     in std_logic;

    dslp:       out std_logic;
    ri:         out std_logic
);
end speed_transition;

architecture speed of speed_transition is

signal state: std_logic_vector(2 downto 0);
-- State assignment is such that the logic is reduced
constant state1: std_logic_vector(2 downto 0) := "000";
constant state2: std_logic_vector(2 downto 0) := "001";
constant state3: std_logic_vector(2 downto 0) := "011";
constant state4: std_logic_vector(2 downto 0) := "111";
constant state5: std_logic_vector(2 downto 0) := "110";
constant state6: std_logic_vector(2 downto 0) := "100";
constant state7: std_logic_vector(2 downto 0) := "010";
constant state8: std_logic_vector(2 downto 0) := "101";
```

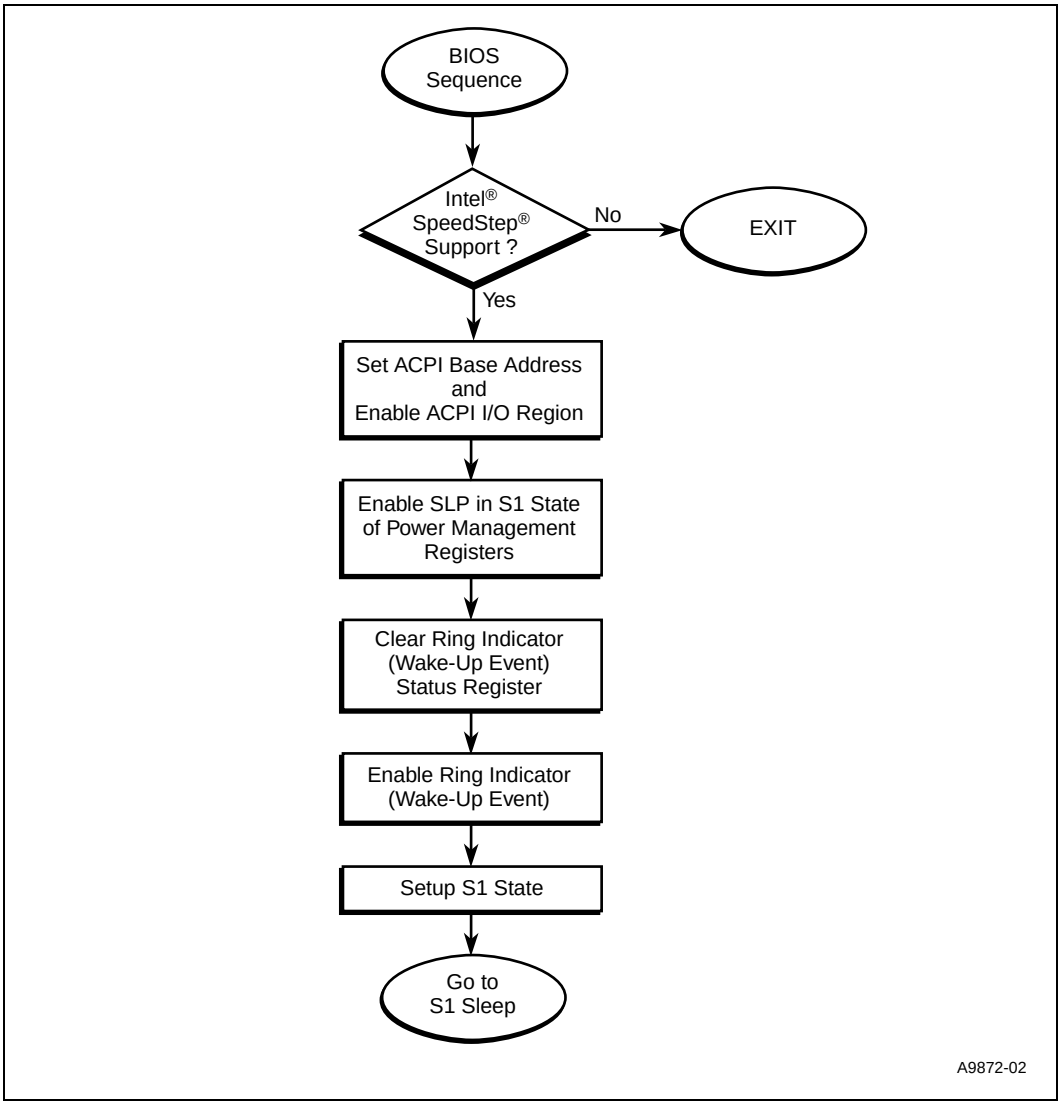
```
begin
-- If reset is low the state machine will be stable and in state1
process (clk, rst)
    begin
        if rst='0' then
            state <= state1;
        elsif (clk'event and clk='1') then
            case state is
                when state1 =>
                    if cpuslp = '0' then
                        state <= state2;
                    end if;
                    dslp <= '1';
                    ri <= '1';

                when state2 =>
                    state <= state3;

                when state3 =>
                    state <= state4;
                    dslp <= '0';

                when state4 =>
                    state <= state5;
                    dslp <= '1';

                when state5 =>
                    state <= state6;
                    ri <= '0';

                when state6 =>
                    if cpuslp = '1' then
                        state <= state1;
                    else
                        state <= state6;
                    end if;

                when others =>
                    state <= state1;

            end case;
        end if;
    end process;

end speed;
```

2.5 BIOS Enabling

2.5.1 Initiating the Transition Sequence in BIOS

BIOS designers must follow the design guidelines referenced in the *Intel® Pentium® 4 Processor in 478-Pin Package and 845E Chipset Platform for DDR Design Guide*. However, additional BIOS modifications are required to initiate the transition sequence. Figure 6 depicts a flow chart of the required BIOS modifications.

Figure 6. Required BIOS Modifications



The "Intel® SpeedStep® Support?" step above controls whether or not the transition sequence actually takes place. If a desktop processor is present in the socket (as in the case of a scalable platform), the BIOS first checks the processor for enhanced Intel SpeedStep technology support. If enabled (as in a mobile processor), the transition sequence continues; if disabled (as in a desktop processor), the transition sequence does not execute.

The BIOS must run the equivalent of the following psuedo-code during POST, immediately following the initialization of the ICH4:

```
// Initiate an Intel(R) SpeedStep(R) technology sequence.
// This sequence is used to trigger the external logic on board.
// The external logic is triggered by CPUSLP# assertion.
// The external logic asserts the Wake event (Ring Indicator) to wake system.

IF ( SpeedStep-Supported )
{
    Ring Indicator Status, GPE0_STS[8] = Clear
    Ring Indicator Event, GPE0_EN[8] = Enable
    Mask Interrupts
    CPUSLP# signal assert in S1 Sleep, GEN_PMCON_1 [5] = Enable
    Sleep Type, PM1_CNT [12:10] = Desktop S1 State (001h)
    Sleep, PM1_CNT [13] = Enable
}
```

To obtain details on the register utilized to check whether Intel SpeedStep technology is supported, please contact your Intel field representative.

Note: The system must not contain an external bus master that could possibly interrupt the above sequence. If so, the BIOS must disable that external bus master.

2.5.2 Microcode Updates in BIOS

The Intel® Pentium® 4 processor and Intel® Pentium® 4 Processor-M contain different microcode. If the BIOS contains code to update the processor microcode, the BIOS must be modified to first detect which processor is present in the socket, and then load the appropriate microcode.

3.0 Voltage Regulator Design Guidelines

Because scalable platforms do not require advanced power management support, the primary differences between mobile and desktop requirements are the loadline specification and VID table translation. As such, for a scalable platform, Intel recommends one of the two following voltage regulator solutions:

- Design the board to accommodate two voltage regulator modules (VRMs), or
- Design the board with a scalable voltage regulator-down (VRD) on the board.

3.1 Scalable Platform Voltage Regulator Modules

For this solution, one connector should be designed onto the board to support either a desktop or mobile VRM. Refer to the *VRM 9.0 DC-DC Converter Design Guidelines* for specifications and design guidelines for the VRM connector. Intel has enabled third party vendors to manufacture the two VRMs. The vendors are listed in Table 5.

Table 5. VRM Vendors

Mobile VRM Vendor	Desktop VRM Vendor
Powercube, A Natel Company 9340 Owensmouth Ave Chatsworth, California 91311 USA Contact: Mr. Shree Ramadas Tel: (818) 734-6500 Toll-free: (800) 866-3590 FAX: (818) 734-6540 Toll-free FAX: (800) 866-3589 Email: shree@powercube.com www.powercube.com Powercube Part Number: VRMP-91-12-40 Sales representatives are located in Japan, China, India, Taiwan, Korea, UK, France, Germany, Norway, Sweden, Finland, Denmark, Austria, Italy, and Israel.	Celestica 4607 S.E. International Way Milwaukie, Oregon 97222 USA Tel: 971-206-2800 FAX: 503-786-5011 Email: power@celestica.com www.celestica.com Celestica Part Number: 073-20816-01 Sales representatives are located in North America, Japan, Taiwan, and Malaysia.

NOTE: These vendors are listed by Intel Corporation as a convenience to Intel's general customer base. Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

Caution: The proper VRM must be plugged into the connector before powering on the board. If the processor and VRM do not match, the VRM will deliver an incorrect voltage level, which may cause damage to the board and components.

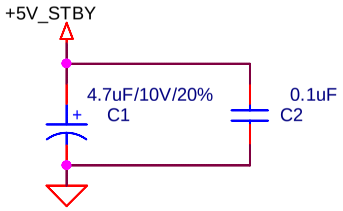
3.2 Scalable Platform Voltage Regulator Down

A reference design for a VRD for a scalable platform is included in Appendix B, "Scalable Platform VRD Schematic".

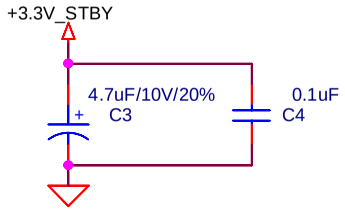
Appendix A High Frequency Transition Sample Schematic

This appendix includes a schematic diagram for one example implementation of the Intel® Pentium® 4 Processor-M transition requirements.

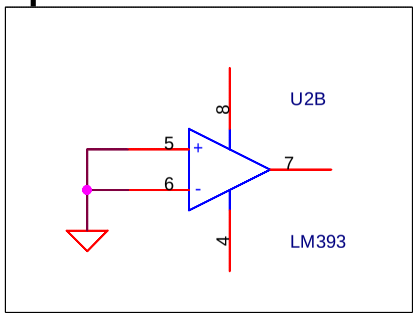
FOR LM393



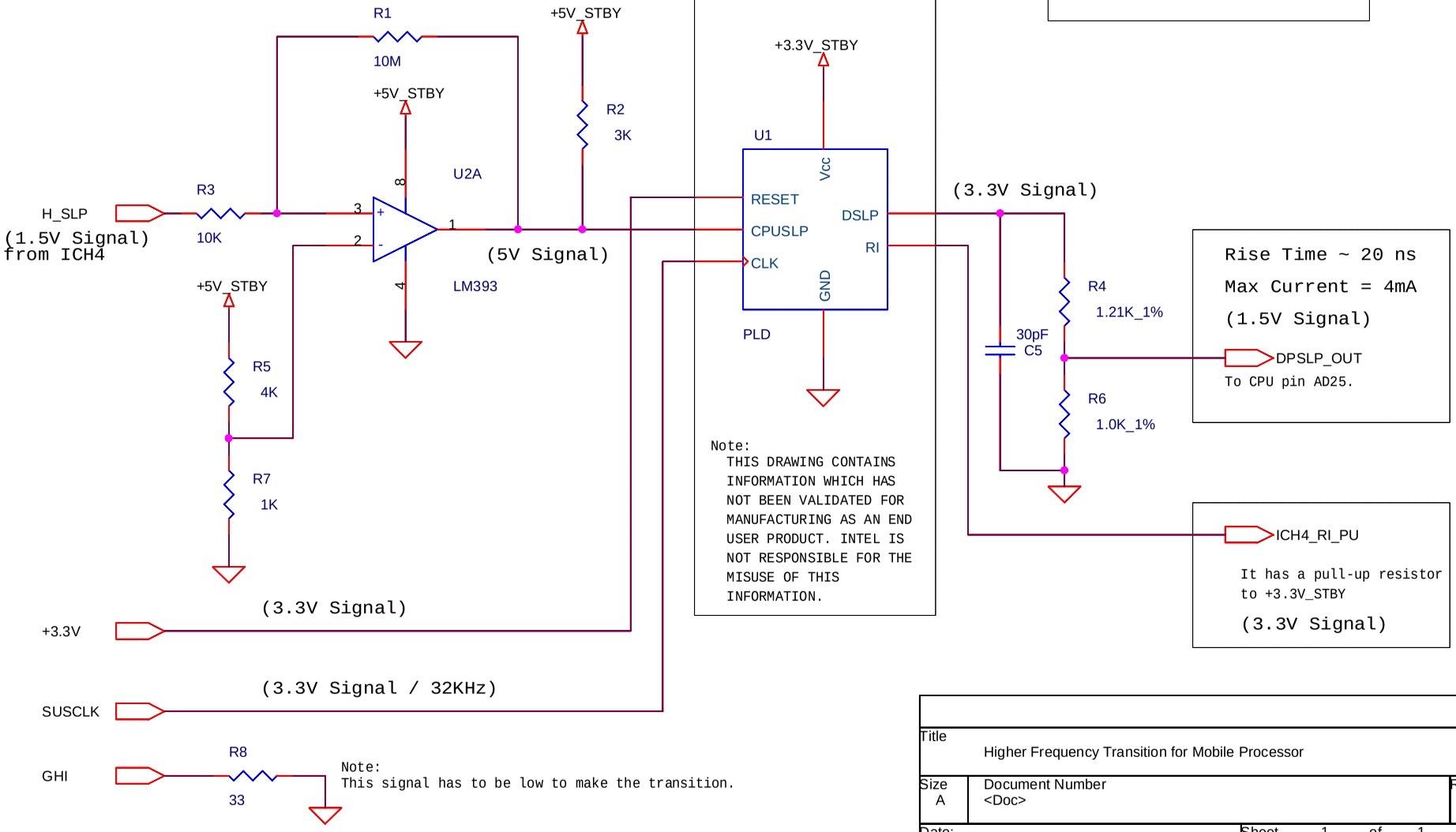
PLD DECOUPLING



Spare Parts



PLD



Title: Higher Frequency Transition for Mobile Processor		
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Appendix B Scalable Platform VRD Schematic

This appendix includes a reference schematic for a voltage regulator-down (VRD), compatible with both the Intel® Pentium® 4 processor and the Intel® Pentium® 4 Processor-M.

APPENDIX B

VIN is the 12V input from ATX power supply before input inductor. It is the prefered way to power drivers.

Driver Vcc and PVCC can also be connected to 12V after input inductor if it's difficult to connect them to Vin in the layout.

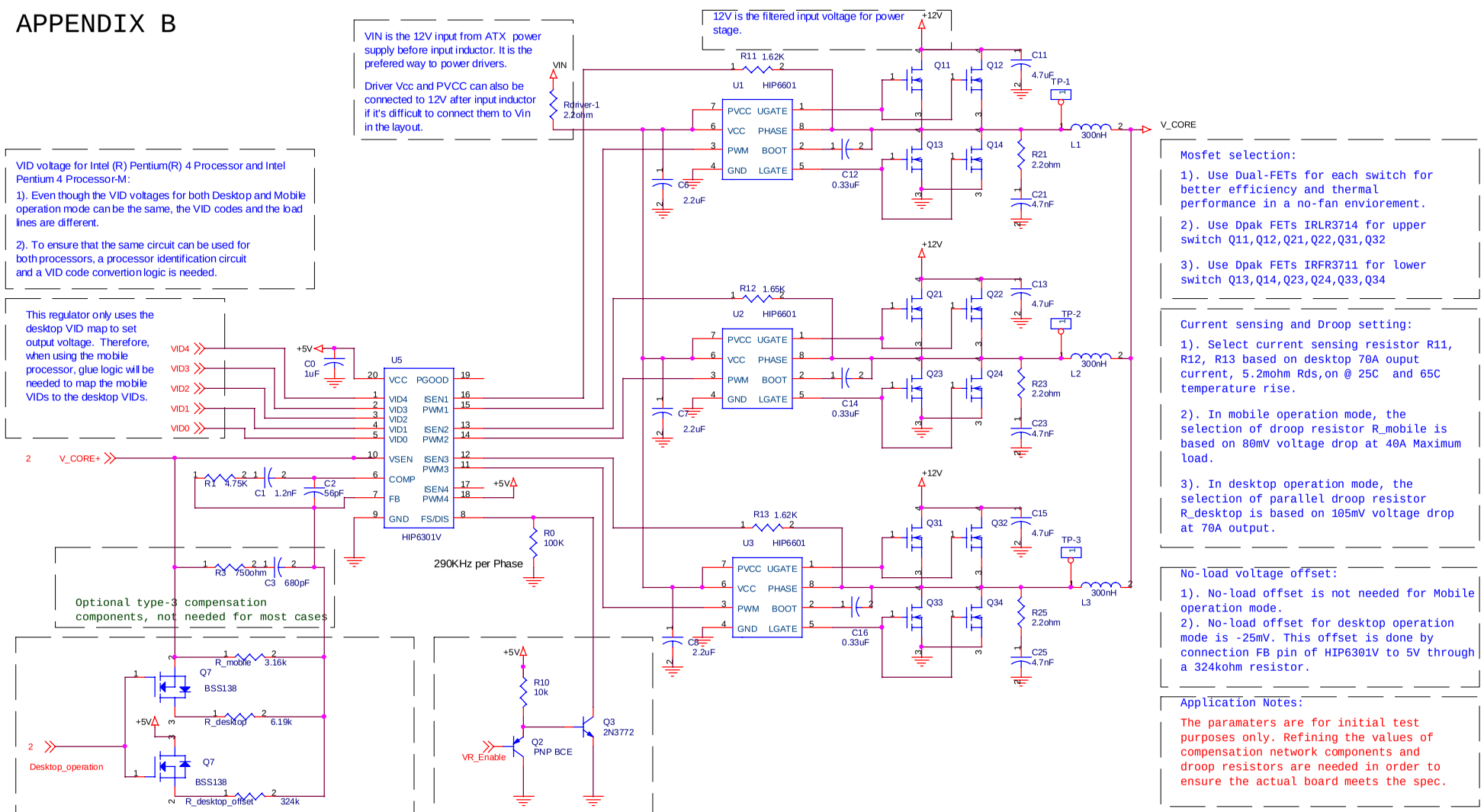
12V is the filtered input voltage for power stage.

VID voltage for Intel (R) Pentium(R) 4 Processor and Intel Pentium 4 Processor-M:

1). Even though the VID voltages for both Desktop and Mobile operation mode can be the same, the VID codes and the load lines are different.

2). To ensure that the same circuit can be used for both processors, a processor identification circuit and a VID code convertion logic is needed.

This regulator only uses the desktop VID map to set output voltage. Therefore, when using the mobile processor, glue logic will be needed to map the mobile VIDs to the desktop VIDs.



Load-line switching circuit: When Desktop_operation control signal is High, the VR will operate to the load line.

The equivalent resistor of R_mobile in parallel with R_desktop determines Desktop operation mode load line.

VR enable circuit is for reference only. Please refer to reference design schematics.

Mosfet selection:

1). Use Dual-FETs for each switch for better efficiency and thermal performance in a no-fan enviorement.

2). Use Dpak FETs IRLR3714 for upper switch Q11,Q12,Q21,Q22,Q31,Q32

3). Use Dpak FETs IRFR3711 for lower switch Q13,Q14,Q23,Q24,Q33,Q34

Current sensing and Droop setting:

1). Select current sensing resistor R11, R12, R13 based on desktop 70A ouput current, 5.2mohm Rds,on @ 25C and 65C temperature rise.

2). In mobile operation mode, the selection of droop resistor R_mobile is based on 80mV voltage drop at 40A Maximum load.

3). In desktop operation mode, the selection of parallel droop resistor R_desktop is based on 105mV voltage drop at 70A output.

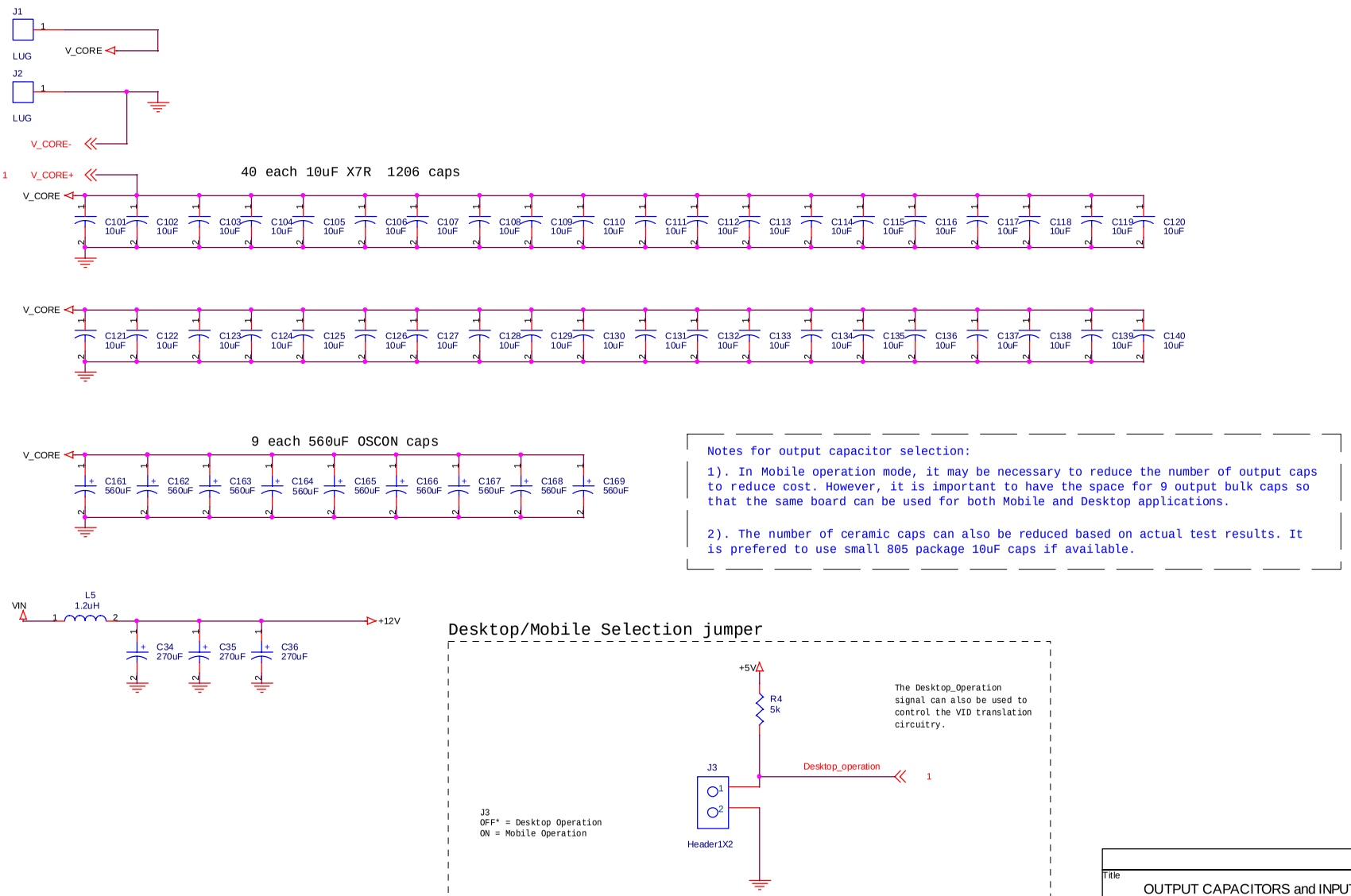
No-load voltage offset:

1). No-load offset is not needed for Mobile operation mode.
2). No-load offset for desktop operation mode is -25mV. This offset is done by connection FB pin of HIP6301V to 5V through a 324kohm resistor.

Application Notes:

The paramaters are for initial test purposes only. Refining the values of compensation network components and droop resistors are needed in order to ensure the actual board meets the spec.

Title	PWM Control and Power Stage	
Size: B	Document Number: Intel (R) Pentium (R) 4 Processor and Intel Pentium 4 Processor-M Scalable VRD	Rev: 1.5
Date: Monday, April 21, 2003	Sheet 1 of 2	


J1
LUG
V_CORE
J2
LUG
V_CORE-
V_CORE+
40 each 10uF X7R 1206 caps
C101 10uF
C102 10uF
C103 10uF
C104 10uF
C105 10uF
C106 10uF
C107 10uF
C108 10uF
C109 10uF
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C138 10uF
C139 10uF
C140 10uF
9 each 560uF OSCON caps
C161 560uF
C162 560uF
C163 560uF
C164 560uF
C165 560uF
C166 560uF
C167 560uF
C168 560uF
C169 560uF
VIN
L5
1.2uH
+12V
C34 270uF
C35 270uF
C36 270uF
Notes for output capacitor selection:
1). In Mobile operation mode, it may be necessary to reduce the number of output caps to reduce cost. However, it is important to have the space for 9 output bulk caps so that the same board can be used for both Mobile and Desktop applications.
2). The number of ceramic caps can also be reduced based on actual test results. It is prefered to use small 805 package 10uF caps if available.
Desktop/Mobile Selection jumper
+5V
R4
5k
The Desktop_Operation signal can also be used to control the VID translation circuitry.
J3
Desktop_operation
J3
OFF* = Desktop Operation
ON = Mobile Operation
Header1X2
Title
OUTPUT CAPACITORS and INPUT FILTER
Size
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Document Number
Intel (R) Pentium (R) 4 Processor and Intel Pentium 4 Processor-M Scalable VRD
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Appendix C Reference Design Schematics

This appendix includes a complete set of board schematics for a scalable Intel® 845E chipset platform, which supports both the Intel® Pentium® 4 processor and Intel® Pentium® 4 Processor-M.

APPENDIX C

Intel (R) 845E Interactive Client Reference Design

Revision X2

Last Change : 2002-09-26

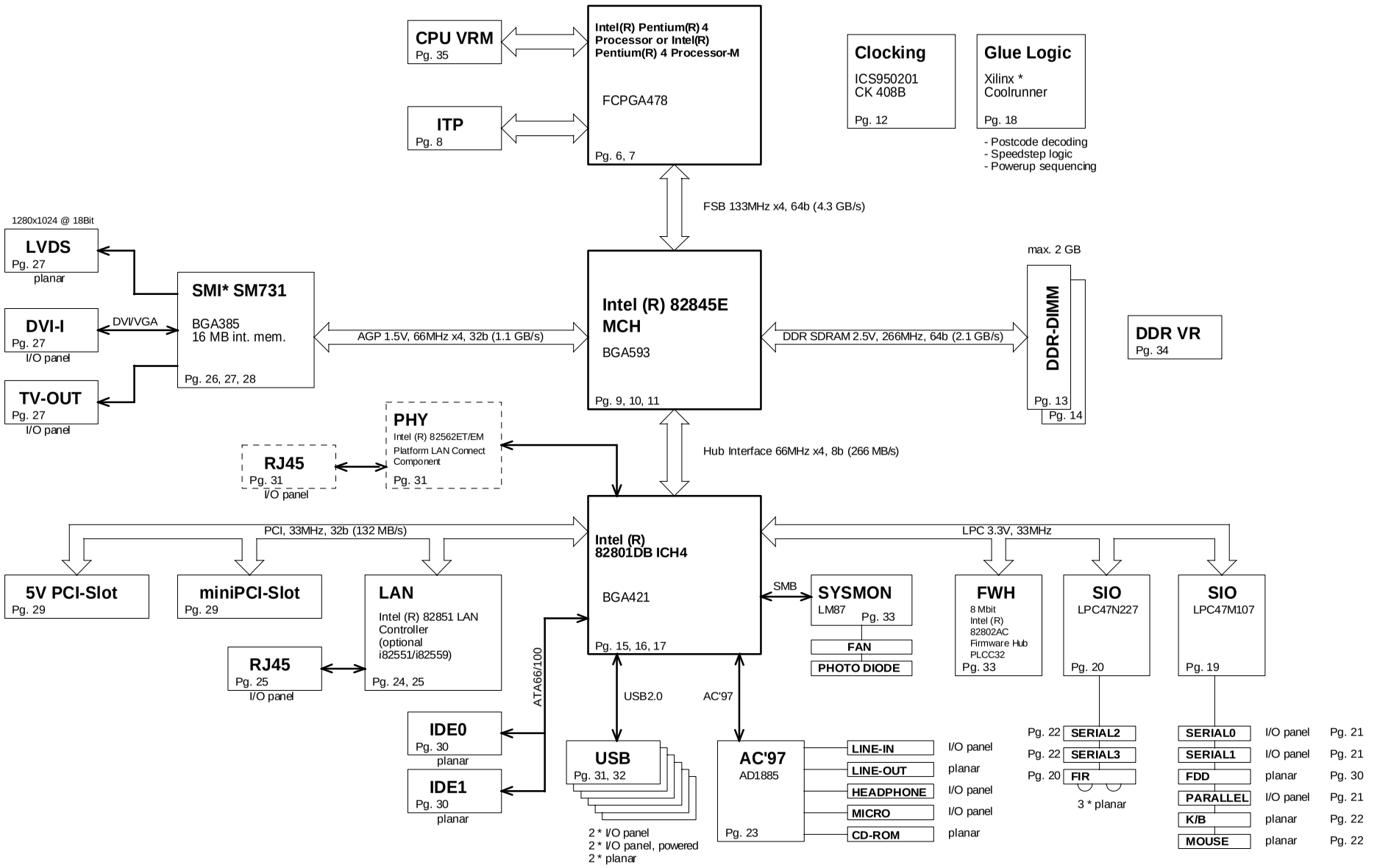
#	Schematic Page
1	COVER SHEET
2	BLOCK DIAGRAM
3	BLOCK-POWER
4	MECH-ROUTE
5	NOTES
6	CPU-P4 BUS
7	CPU-P4 POWER
8	CPU-ITP
9	MCH-SYSBUS & CLOCK
10	MCH-AGP & DDR
11	MCH-POWER
12	CLK-ICS950201
13	DDR-DIMM 0
14	DDR-DIMM 1
15	ICH4-SYSBUS & PCI
16	ICH4-LPC & IDE & USB
17	ICH4-POWER
18	GLUE LOGIC
19	SIO0-LPC47M107
20	SIO1-LPC47N227
21	CONN-COM1/COM2/LPT
22	CONN-COM3/COM4/KBC
23	AC97-AD1885
24	LAN-10/100/1000 BUS
25	LAN-10/100/1000 CONN
26	VGA-COUGAR-01
27	VGA-COUGAR-02
28	VGA-COUGAR-03
29	CONN-PCI
30	CONN-01 IDE-FLOPPY
31	USB0-USB1-LAN0
32	USB2-USB5
33	SYSTEM CONTROL
34	DDR-POWER
35	POWER

Prefix	Netobject
A_	CRITICAL ANALOG TRACES
AC_	AC97 SIGNAL
APIC_	APIC SIGNAL
AUD_	ANALOG AUDIO SIGNAL
CK_	CLOCK SIGNAL
EEn_	SERIAL EEPROM LANn
EN_	ENABLE FOR POWER SOURCES
F_	FLOPPY DISK SIGNAL
FWH_	FIRMWARE HUB SIGNAL
G_	AGP BUS SIGNAL
GND_	GND SIGNAL DERIVED
GND	GND POWER
H_	P4 HOSTBUS SIGNAL
I2C_	I2C BUS SIGNAL
IDE_	IDE SIGNAL
INT_	INTERRUPT SIGNAL
KB_	KEYBOARD SIGNAL
L_	LPC BUS SIGNAL
LANn_	LAN CONTROLLER n SIGNAL
LP_	LPT1284 SIGNAL
M_	MEMORY BUS SIGNAL
MIDI_	MIDI SIGNAL
MS_	MOUSE SIGNAL
P_	PCI BUS SIGNAL
SPn_	SERIAL PORT n SIGNAL
USB_	USB PORT SIGNAL
V_	POWER
ZV_	ZV VIDEO PORT SIGNAL

	Changes from X1 to X2
1	All BAT54A (0-0031-1261) changed to BAT54 (0-0031-1104) due to wrong polarity
2	R712 changed from 10k to 15k to adjust voltage
3	PU R756 and R757 added @ U38.15 (PG_VDDR) and U38.16 (PG_V1V5)
4	Net on pins U3.54 and U3.55 separated (BSEL[0..1]) due to naming error
5	PU R758 added at CN34.7 (SYS_RESET#)
6	PU R759 added at U39.4 (VIDPWRGD)
7	C717 changed from 4u7 to 1u
8	R607 not populated
9	R571 and R572 not populated (FWH Test Pins)
10	R585 and R586 not populated (for LVDS 18 Bit)
11	R760 and C741 added to U7.50 to generate a V_3V3SB input delay for resume reset
12	R501 and R494 not populated due to PCI config of LAN 82540
13	U36 FWH symbol changed due to wrong pinout (Pin 23, 24 and 25)
14	R496 changed to 4k7 and set to GND (PD M66EN)
15	R525 and R499 is now populated
16	R530 not populated due to wrong V_2V5LAN voltage
17	U20.G4 is now 51R Pulldown to GND
18	U20.H4 is now 33R Pullup to V_3V3LAN
19	AC97 Fixup (AC_SDIN0 -> Changed to AC_SDIN2 on ICH4)
20	Swap ICH4 Pin N20 and P21 (H_HISTB+ / H_HISTB-) due to wrong info in yellow cover
21	LAN 82540 Fixup (R519 populated with 0R, R517 changed to 2K49 and R513 changed to 330R)
22	R615 changed to 4K32 due to Cougar Bug
23	HW Rev changed to 2 at Glue Logic
24	R373 is now populated with 10M
25	CN12.4 must be isolated cause of shortcut of AUD_MIC_BIAS to GND
26	PU R761-R765 added to VID[0:4]
27	PU R766 added to U23.15, PD R767 added to U23.14 (Panellink strapping options)
28	HD-LED-power connected to V_5V0 instead of V_5V0SB
29	PD R768 added to PS_ON
30	PU R769 added to U3.28 (PGOOD408#)
31	PD R770, R771, R772 added to power enables (default off, if CPLD not configured)
32	PD R773-R776 added to serial port shut down pins
33	Splitted SMI# and PME# signals of SIO0 and SIO1 on ICH4-GPIOs
34	Removed R383, R384, R385
35	Added D25 to avoid crossvoltages from VGA Monitor
36	Added D26 to avoid crossvoltages LPT Port
37	Alternative population of L7 to L12 with resistors (0R)
38	PME# Signal of Cougar (PinB7) is set to V_3V3 via 0R
39	U29 (LP3965EMP) can be replaced by an 0R_1206 to power 3V3 on Cougar
40	Possibility to PullDown Pin D8(MD24) on Cougar to enable SDRAM
41	CN41 (JUMPER 3x1) added to connect to MPCI Pins (TIP and RING)
42	V_5V0 input at V_DDR supply is now controlled by XILINX CPLD (Pin 25)
43	Delay of PWRGOOD# (LAN 82540EM Pin A9) to enable correct EEPROM detection

General Note:
All Parts marked 'XXX1' will not be assembled in V1.
All Parts marked 'XXX2' will not be assembled in V2.

Block Diagram



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Title	BLOCK-DIAGRAM
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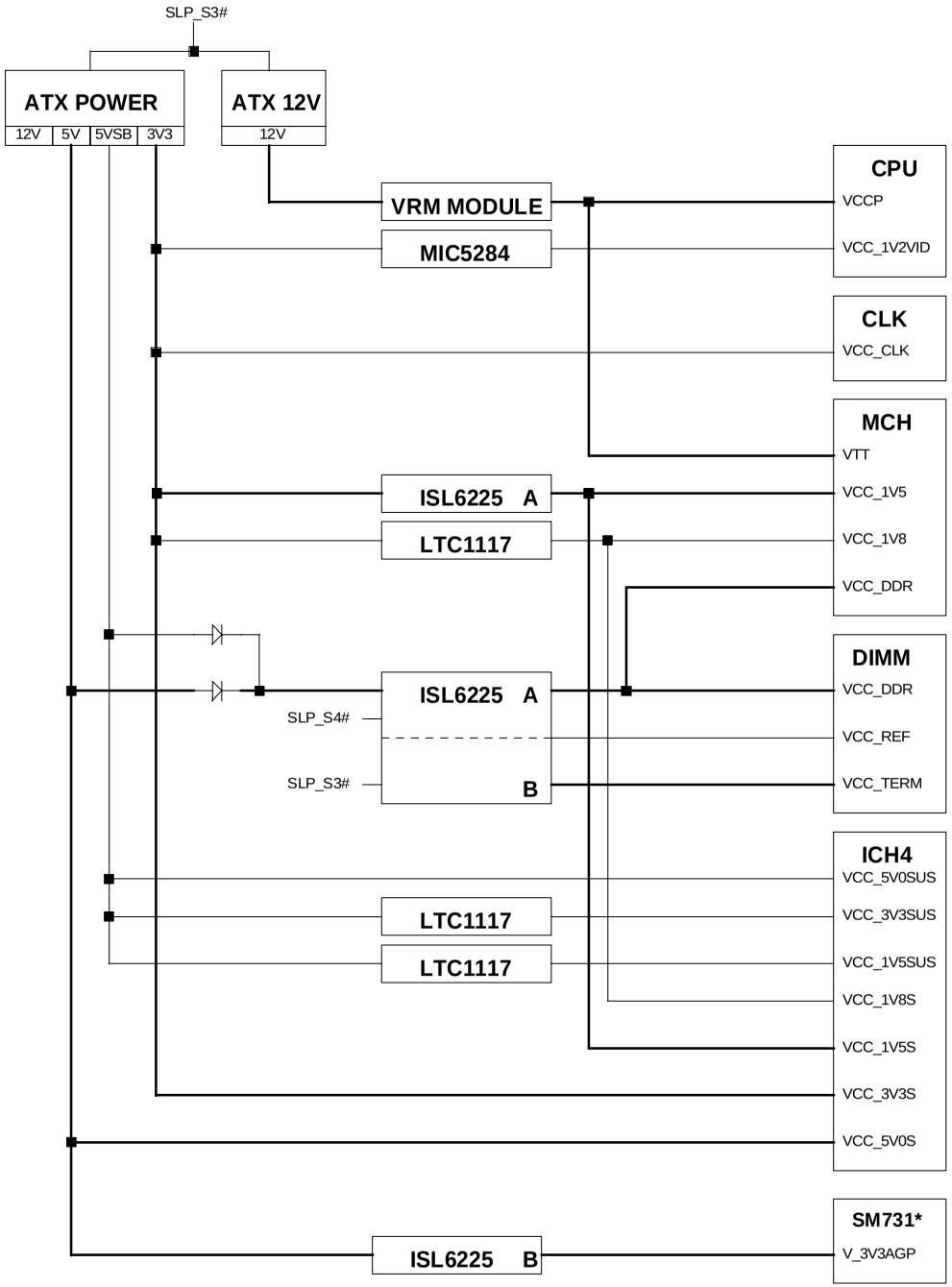

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Title	BLOCK-POWER
Size: C	Document Number: B444B-W
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B1 BOHR4.0
B2 BOHR4.0
B3 BOHR4.0
B4 BOHR4.0
B5 BOHR4.0
B7 BOHR4.0
B8 BOHR4.0
B9 BOHR4.0

DK1 DK204060
DK2 DK204060
DK3 DK204060
DK4 DK204060
DK5 DK204060
DK6 DK204060
DK7 DK204060
DK8 DK204060
DK9 DK204060
DK10 DK204060
DK11 DK204060
DK12 DK204060
DK13 DK204060
DK14 DK204060
DK15 DK204060
DK16 DK204060
DK17 DK204060
DK18 DK204060

MARKE1 MARKETOP
MARKE2 MARKETOP
MARKE3 MARKETOP
MRKF1 MARKFPIT

TP1 TP2 TP3 TP4 GND

M29 MACADRESS
M30 MACADRESS XXX1 XXX2
M31 M E C H BAT_CR2032
M32 M E C H JMP_2mm54

M10 FWH 82802AC
BRD1 PCB B444B

M7 B4441000.01
BIOS IN Firmware-Hub

M1 P4_RETENT
M2 BGA593A/COOL
M23 SM02/RD
M24 SM02/RD
M25 SM02/RD
M26 SM02/RD

M11 HS_MCH_PIN_FIN XXX1 XXX2
M12 HS_MCH_INTERFACE XXX1 XXX2
M15 HS_MCH_LEVER XXX1 XXX2
M16 HS_MCH_CLIP XXX1 XXX2
M17 HS_MCH_PORON XXX1 XXX2

6..8,11,17,33,35 V_CORE → V_CORE

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Title	MECH-ROUTE
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INPUT VOLTAGES	DERIVED VOLTAGES -->		
V_12V0VRM	V_12V0VRMF	V_CORE	V_VCCA V_VCCIOPLL
V_12V0	V_FAN1 V_FAN1S V_FAN1SF V_FAN2 V_FAN2S V_FAN2SF V_12USB2 V_12USB2F V_12USB2S V_12USB3 V_12USB3F V_12USB3S V_12VAUD V_AUDOUT V_5VAUD V_BLI		
V_5V0SB	V_3V3SB	V_3V3LAN V_3V3LAN0	V_1V5LAN V_2V5LAN
	V_1V5SB V_KB V_KBF		
	V_DDR	V_DDRREF	
V_5V0	V_USB0 V_USB1 V_USB2 V_USB3 V_USB4 V_USB5 V_USB0X V_USB1X V_USB2X V_USB3X V_USB4X V_USB5X V_DDRVTT		
	V_1V5	V_1V5A1 V_1V5A2 V_HVDD V_ICHPLL	
	V_3V3AGP	V_2V5_LVD	V_2V5_LVD1 V_LVDD1 V_LVDD2 V_PLLVDD V_2V5_LVD2 V_CVDD
		V_2V0_2V5	V_VDD1
		V_2V5_VDD	V_VDD2 V_VDD3
		V_VCC1 V_AVCC1 V_PVCC1 V_VREF_SII V_DBL V_DL_CL V_DL_CLF V_AVDD V_FPVDD V_TVDD V_VPVDD	
	V_5DVI V_PIDE V_SIDE V_FIR V_IR V_5V0CF V_5DVIF V_IOLAN V_GAME V_GAMEF V_AMP V_AMPIN V_AMPINX V_AMPOUT V_5V0REF		
V_3V3	V_1V2VID V_1V8 V_CLK		
V_3V3SB			
	V_RTC		
V_BAT	V_RTCBIAS		
V_-12V0			
V_-5V0			

POWER STATES

ON IN STATE	POWER PLANE
S5 (SOFT OFF)	V_*SB, V_KB, V_*LAN, V_USB*
S3 (SUS. TO RAM)	V_DDR, V_DDRREF
S0 (FULL ON)	OTHERS

I2C DEVICES

DEVICE	ADDRESS	BUS
CLOCK GENERATOR	1101001x	SM BUS
SO-DIMM0	1010000x	SM BUS
SO-DIMM1	1010001x	SM BUS
ICH4 SLAVE	1000100x	SM LINK
LAN CONTROLLER	N/A	SM LINK
LM87 HW MONITOR	0101110x	SM BUS

PCI/AGP DEVICES

DEV	IDSEL	DEVICE	IRQ	REQ/GNT
00	AD16	SM731 AGP	A	AGP
01	AD17	LAN10/100/1000T	G	4
02	AD18			
03	AD19			
04	AD20			
05	AD21			
06	AD22			
07	AD23			
08	AD24	INTERNAL LAN	N/A	N/A
09	AD25	MINI PCI SLOT	E-F	3
10	AD26	STD PCI SLOT	A-B-C-D	0
11	AD27	RISER SLOT1	B-C-D-A	0
12	AD28			
13	AD29	RISER SLOT2	C-D-A-B	1
14	AD30			
15	AD31	RISER SLOT3	D-A-B-C	2

ICH4 GPIOs

GPIO	DEVICE	SIGNAL NAME
GPI6	SUPER I/O 0	SIO0_SMI#
GPI7	SUPER I/O 1	SIO1_SMI#
GPI8	SUPER I/O 0	SIO0_PME#
GPI12	SUPER I/O 1	SIO1_PME#
GPI13	CPLD	XC_GPIO2
GPIO25	LAN0 KINNERETH	LAN0_ENA
GPIO27	MINI PCI	MPCI_ACT#
GPIO28	CPLD	XC_GPIO1
GPIO32	PRIMARY IDE	IDE_PPDIAG#
GPIO33	SECONDARY IDE	IDE_SPDIAG#
GPIO34	POWERED USB	USB_PWR2ENA#
GPIO35	POWERED USB	USB_PWR3ENA#
GPIO36	FIRMWARE HUB	FWH_WP#
GPIO37	FIRMWARE HUB	FWH_TBL#
GPIO38	PCI RISER	RISER_ID1
GPIO39	PCI RISER	RISER_ID2
GPIO40	AUDIO AMPLIFIER	AMP_SHDN
GPIO41	PCI RISER	NOGO
GPIO42	PCI SLOT	P_PRSNT1#
GPIO43	PCI SLOT	P_PRSNT2#

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Title: NOTES

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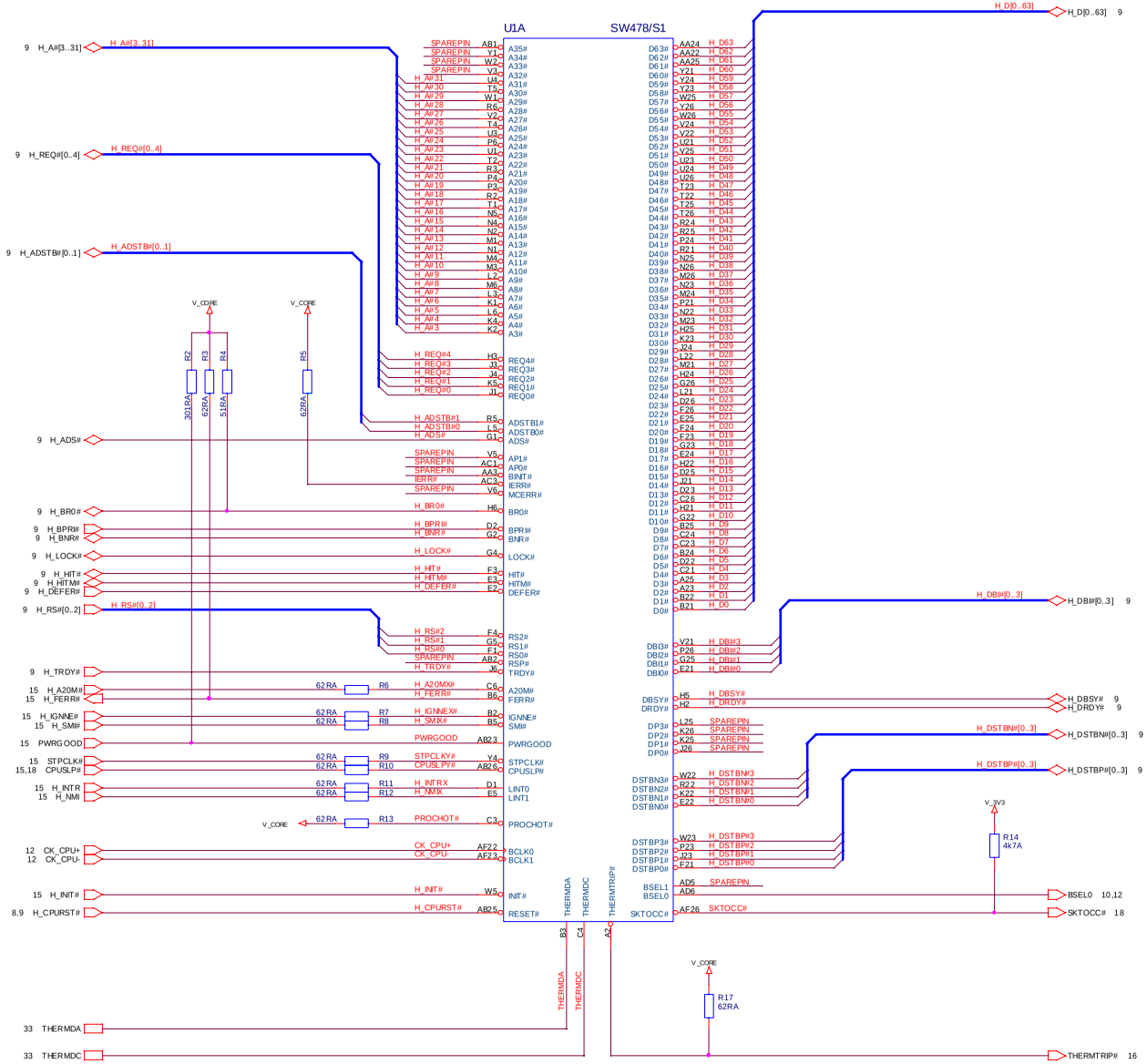

7,9,11,15,16,24..27	SPAREPIN
8,12,15..17,19,20,23,26..29,33,35	V_3V3
4,7,8,11,17,33,35	V_CORE
4,7,8,10..35	GND

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Title: CPU BUS

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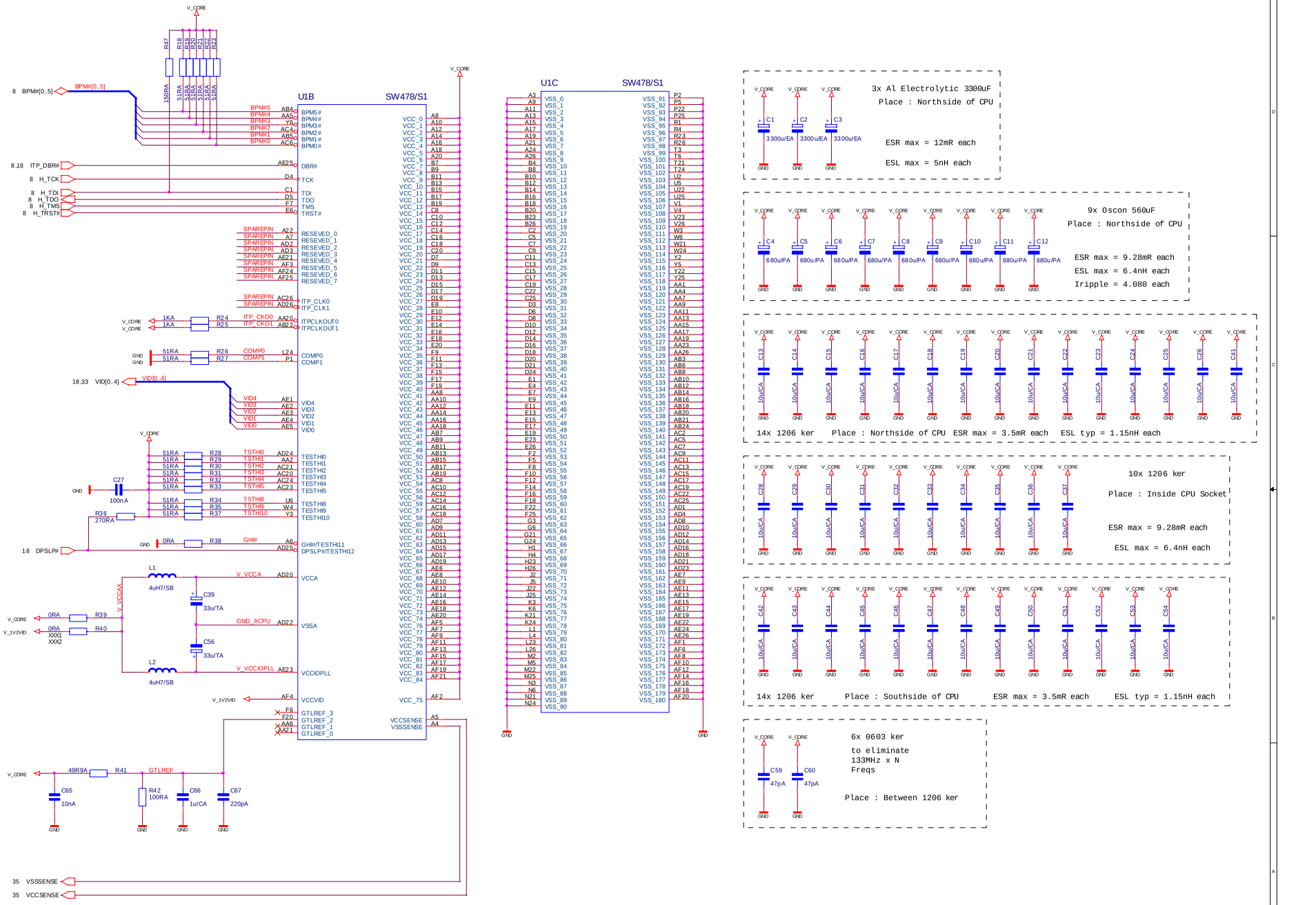
U1B
SW478/S1
U1C
SW478/S1
3x Al Electrolytic 3300uF
Place : Northside of CPU
ESR max = 12mR each
ESL max = 5nH each
9x Oscon 560uF
Place : Northside of CPU
ESR max = 9.28mR each
ESL max = 6.4nH each
Iripple = 4.080 each
14x 1206 ker
Place : Northside of CPU
ESR max = 3.5mR each
ESL typ = 1.15nH each
10x 1206 ker
Place : Inside CPU Socket
ESR max = 9.28mR each
ESL max = 6.4nH each
14x 1206 ker
Place : Southside of CPU
ESR max = 3.5mR each
ESL typ = 1.15nH each
6x 0603 ker
to eliminate
133MHz x N
Freqs
Place : Between 1206 ker
Intel (R) 845E Interactive Client Reference Design
CPU POWER
B444B-W
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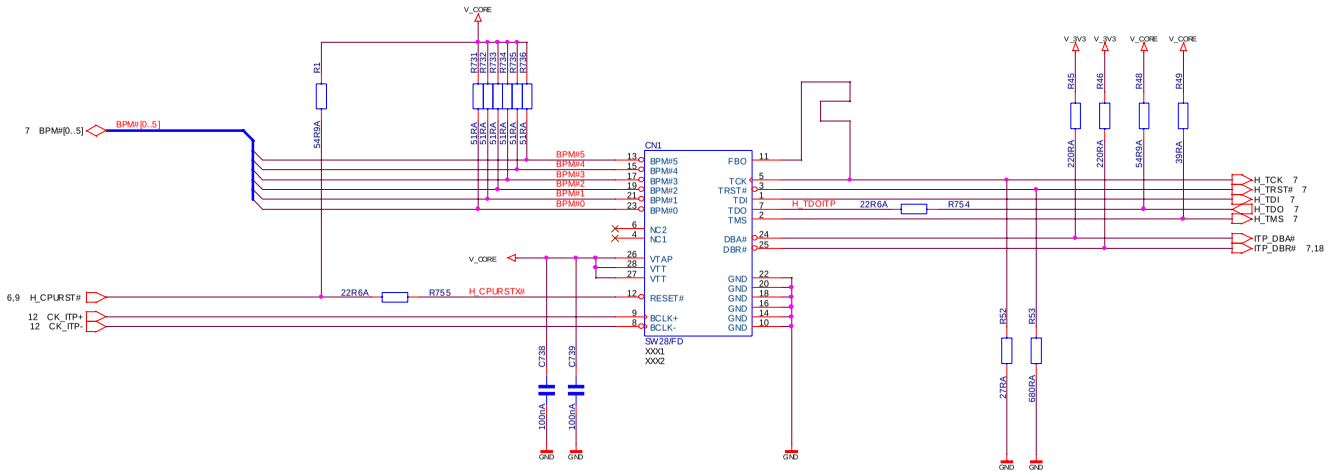
7
35



6,12,15..17,19,20,23,26..29,33,35 V_3V3
4,6,7,11,17,33,35 V_CORE
4,7,10..35 GND

	Intel (R) 845E Interactive Client Reference Design	
Title	CPU-ITP	
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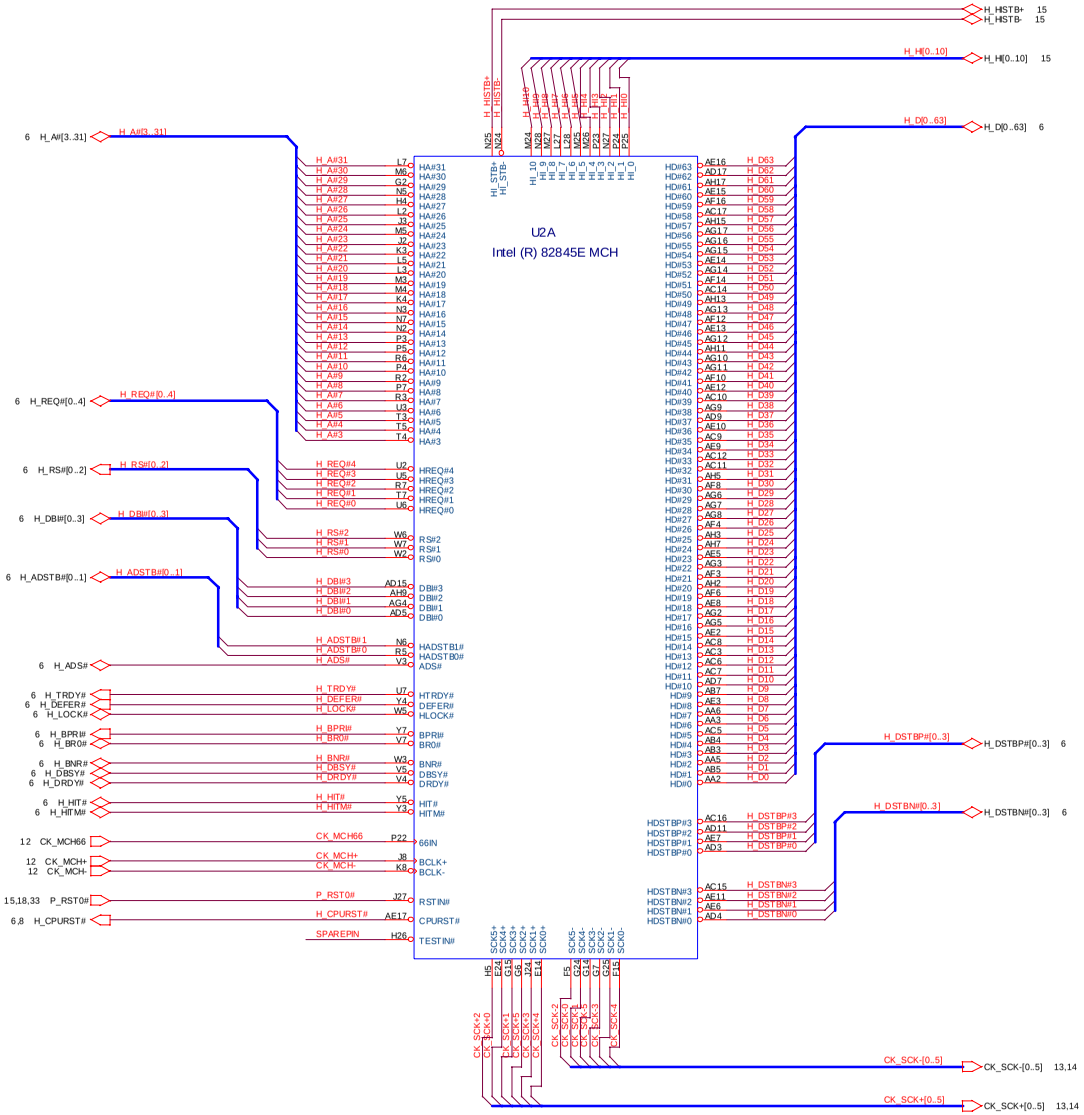

	Intel (R) 845E Interactive Client Reference Design
Title	MCH-SYSBUS & CLOCK
Size	C
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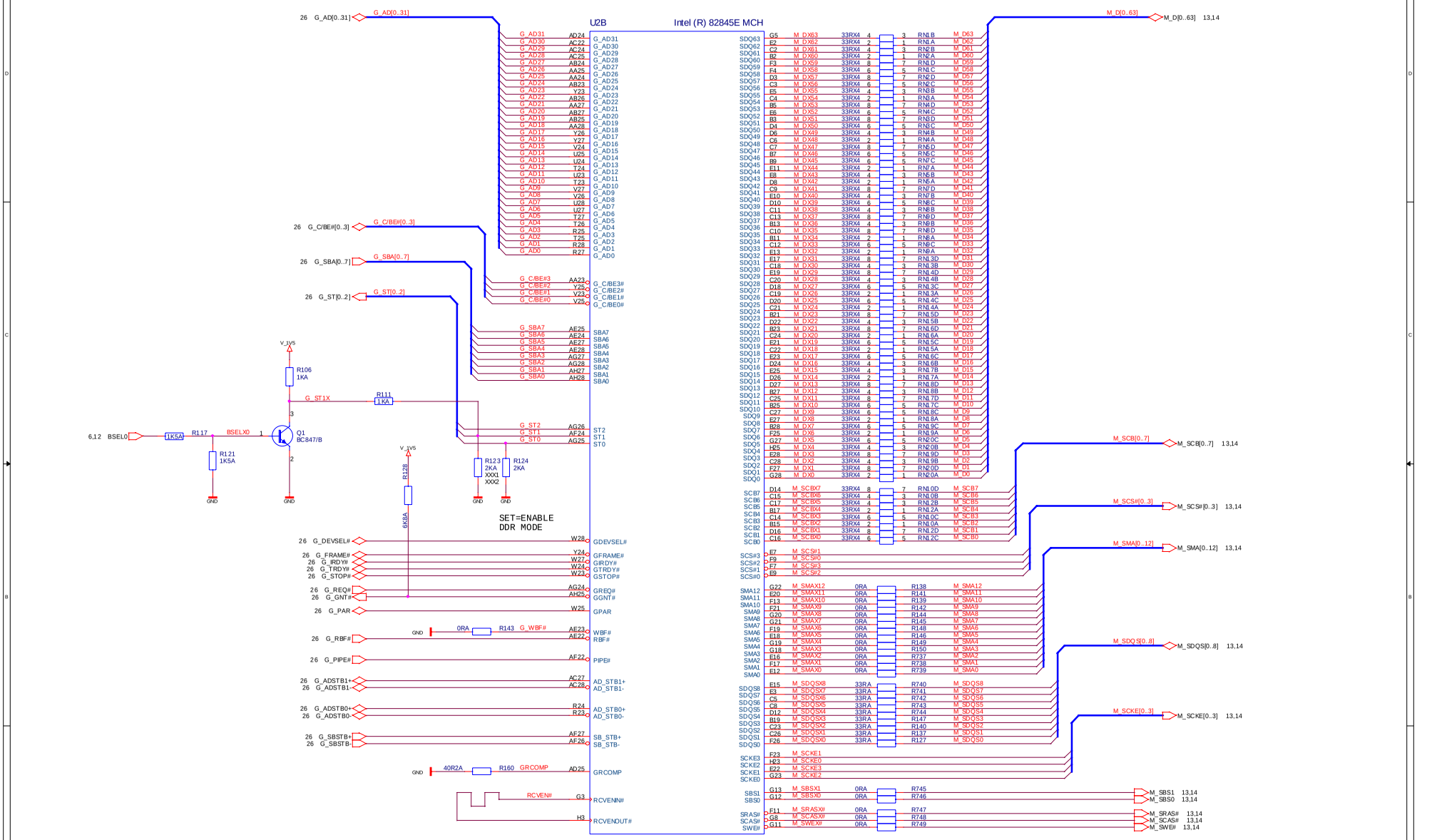

	Intel (R) 845E Interactive Client Reference Design	
Title	MCH-AGP & DDR	
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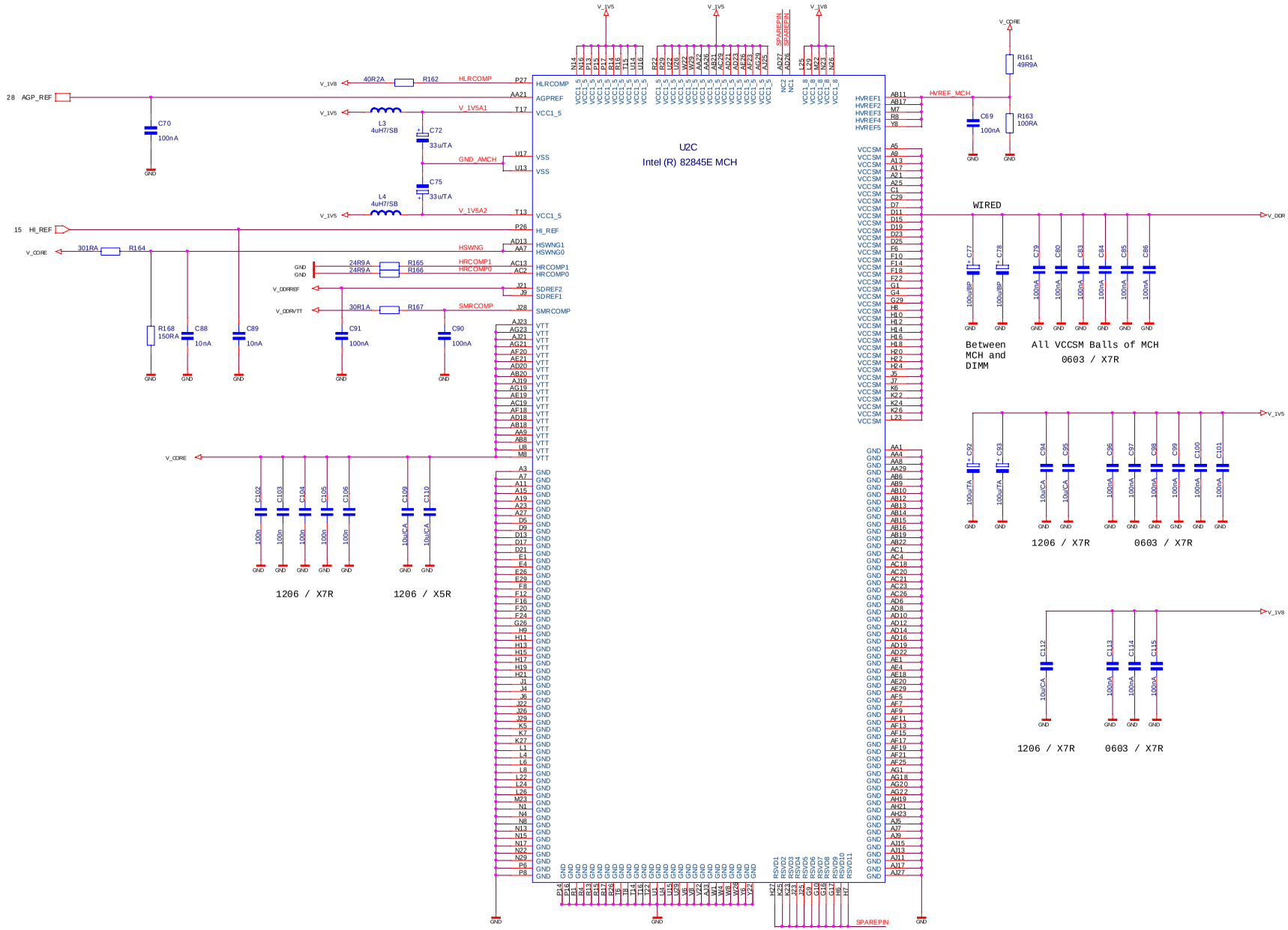

6,7,9,15,16,24..27 SPAREPIN
13,14,33,34 V_DDR
13,14,34 V_DDREF
14,34 V_DDRVTT
4,6..8,17,33,35 V_CORE
15,17,33,35 V_1V8
10,17,28,33,34 V_1V5
4,7,8,10,12..35 GND

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Title	MCH-POWER	
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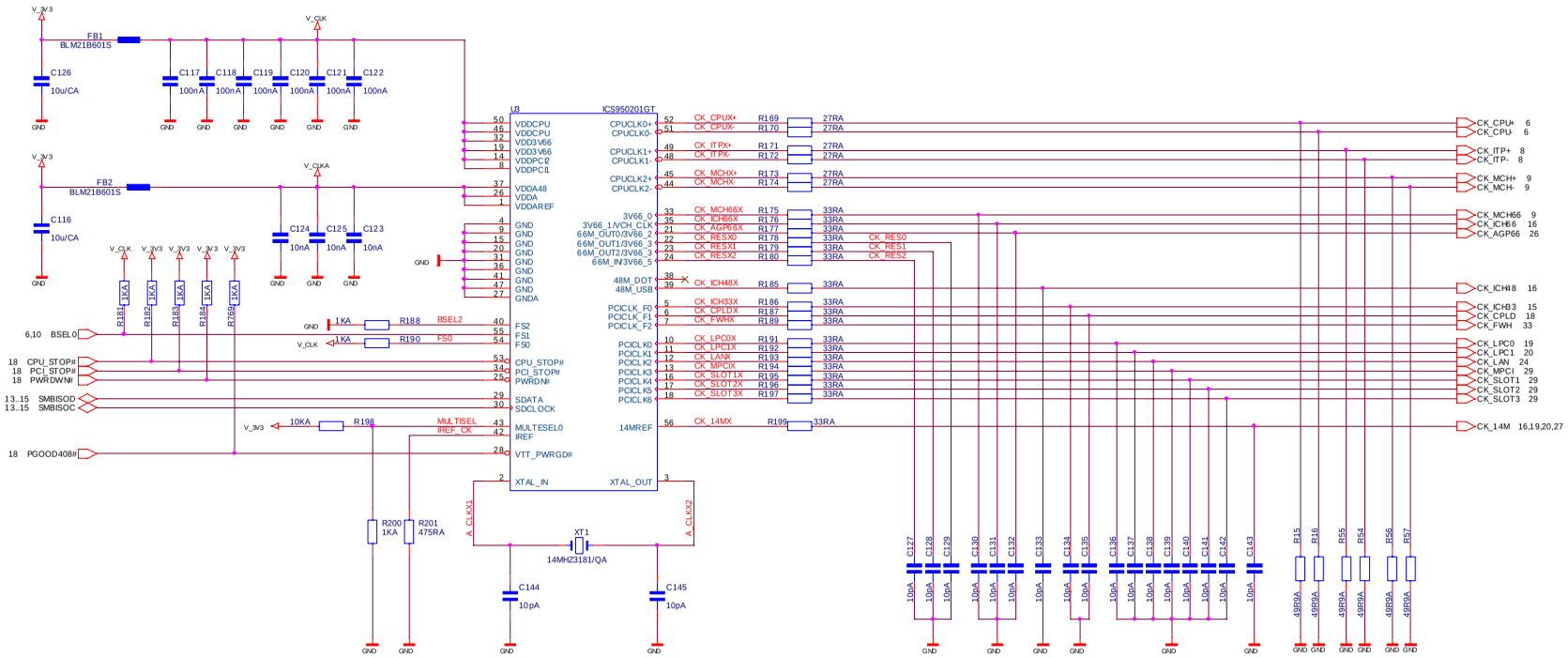

V_CLK 6,8,15..17,19,20,23,26..29,33,35
V_3V3 6,8,15..17,19,20,23,26..29,33,35
GND 4,7,8,10,11,13..35

	Intel (R) 845E Interactive Client Reference Design
Title	CLK ICS950201
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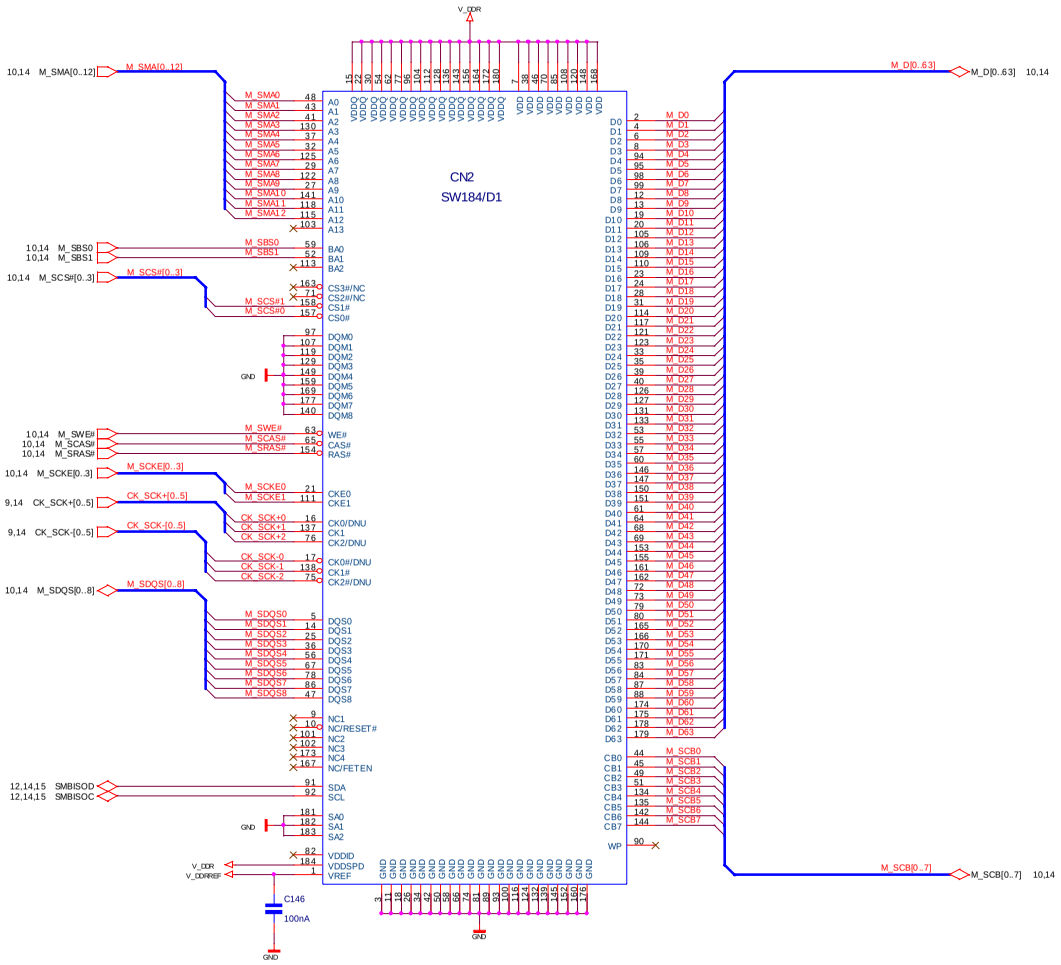
DIMM 0



11,14,34 V_DDRREF
11,14,33,34 V_DDR
4,7,8,10..12,14..35 GND

	Intel (R) 845E Interactive Client Reference Design
Title	DDR DIMM 0
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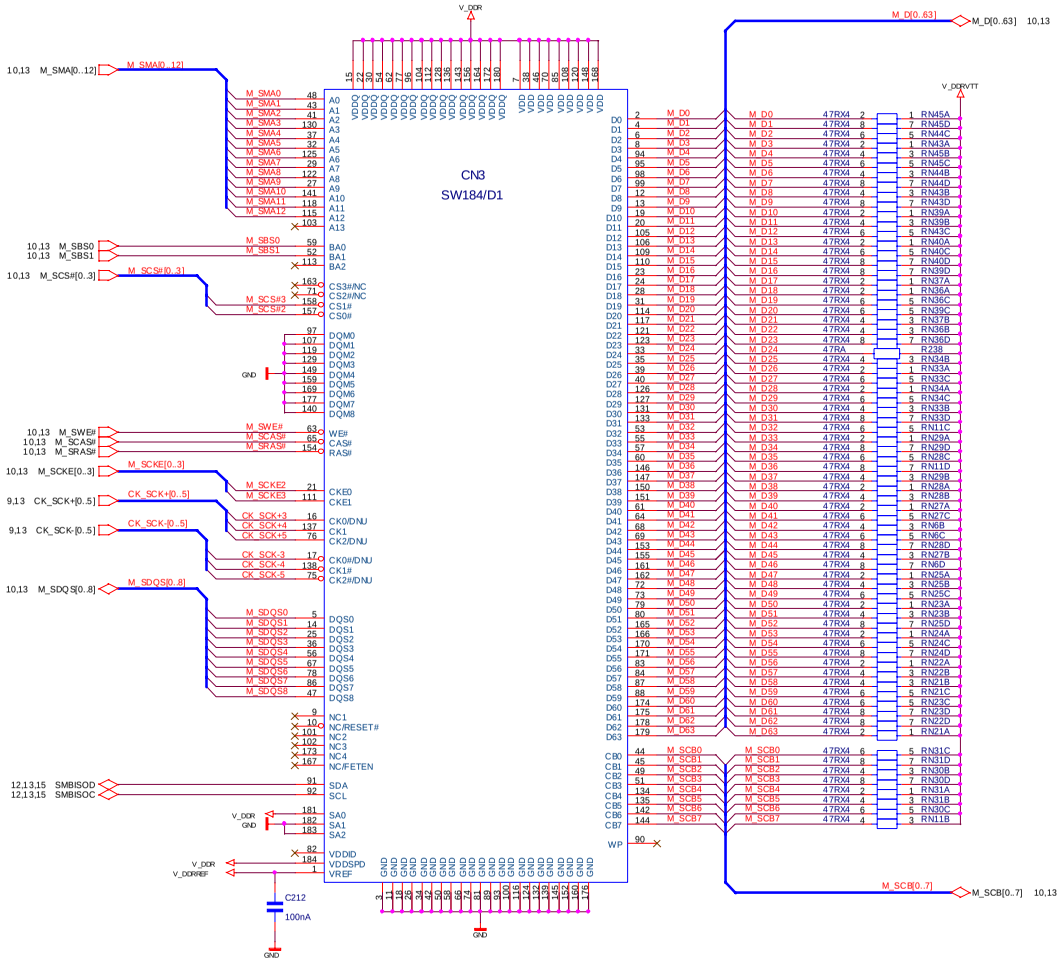
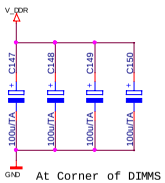
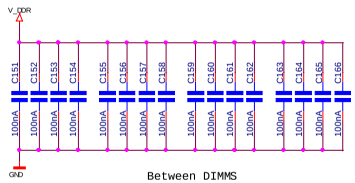
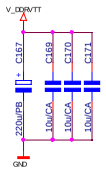
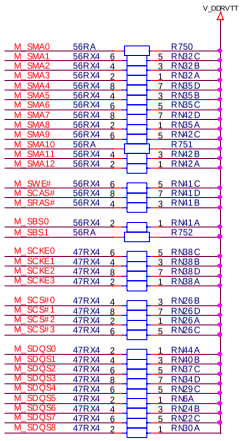
DIMM 1

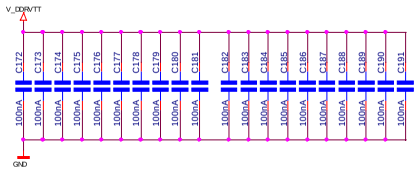


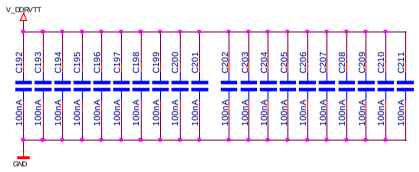


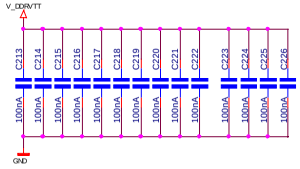


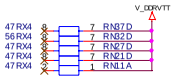












	Intel (R) 845E Interactive Client Reference Design
Title	DDR DIMM 1
Size: C	Document Number: B444B-W
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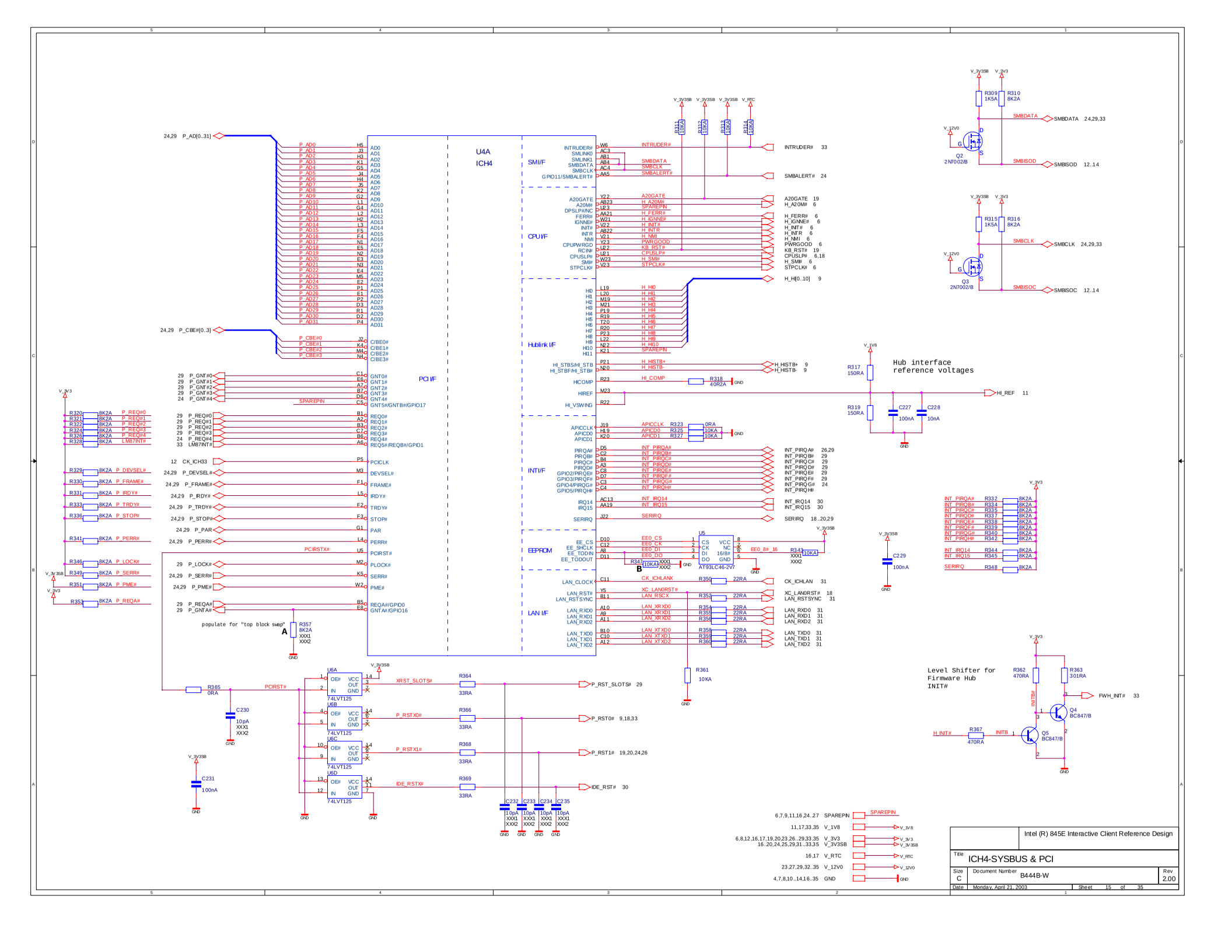
U4A
ICH4
SMI/F
CPU I/F
Hublink I/F
PCI I/F
INTI/F
EEPROM
LAN I/F
Hub interface
reference voltages
Level Shifter for
Firmware Hub
INIT#
populate for "top block swap"
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ICH4-SYSBUS & PCI
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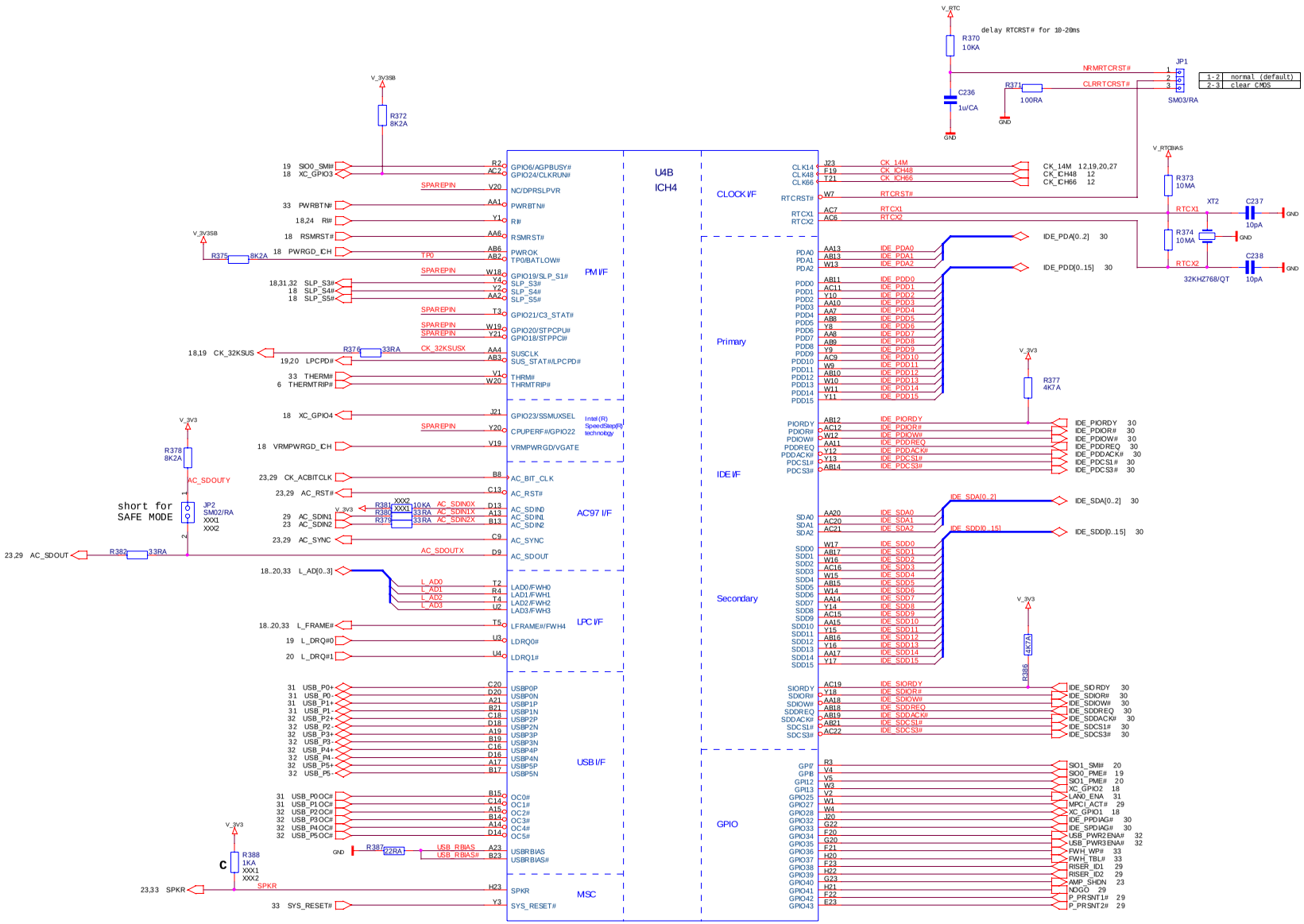

ICH4 Strapping Options

R	Signal	Function	Default
A	P_GNTA#	top block swap	NO STUFF
B	EE_DOUT	reserved	NO STUFF
C	SPKR	no reboot mode	NO STUFF
JP	AC_SDOUTX	safe mode	OPEN

6,7,9,11,15,24..27 SPAREPIN
6,8,12,15,17,19,20,23,26..29,33,35 V_3V3
15,17..20,24,25,29,31..33,35 V_3V3SB
15,17 V_RTC
17 V_RTCBIAS
4,7,8,10..15,17..35 GND

Title	ICH4-LPC & IDE & USB
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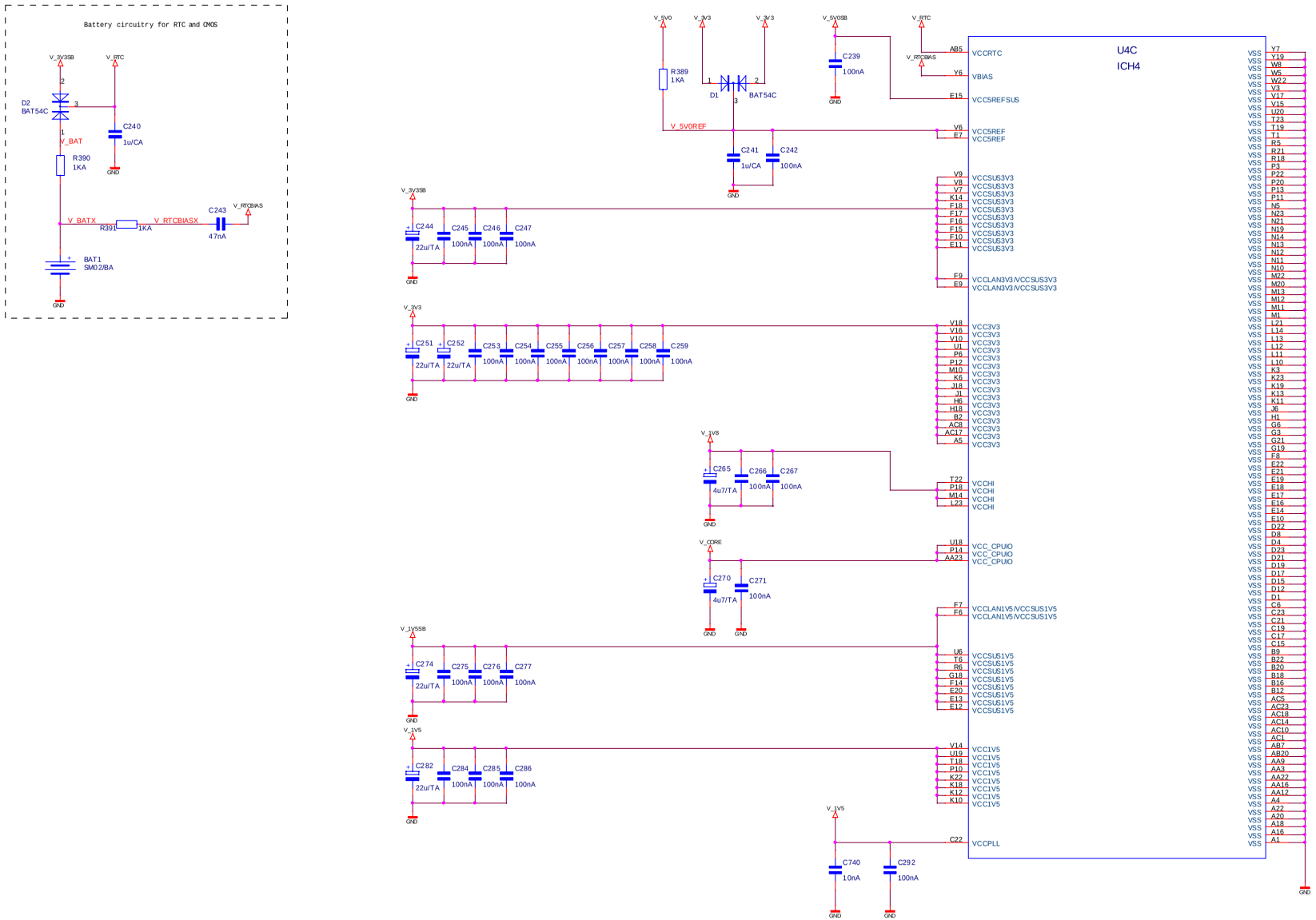
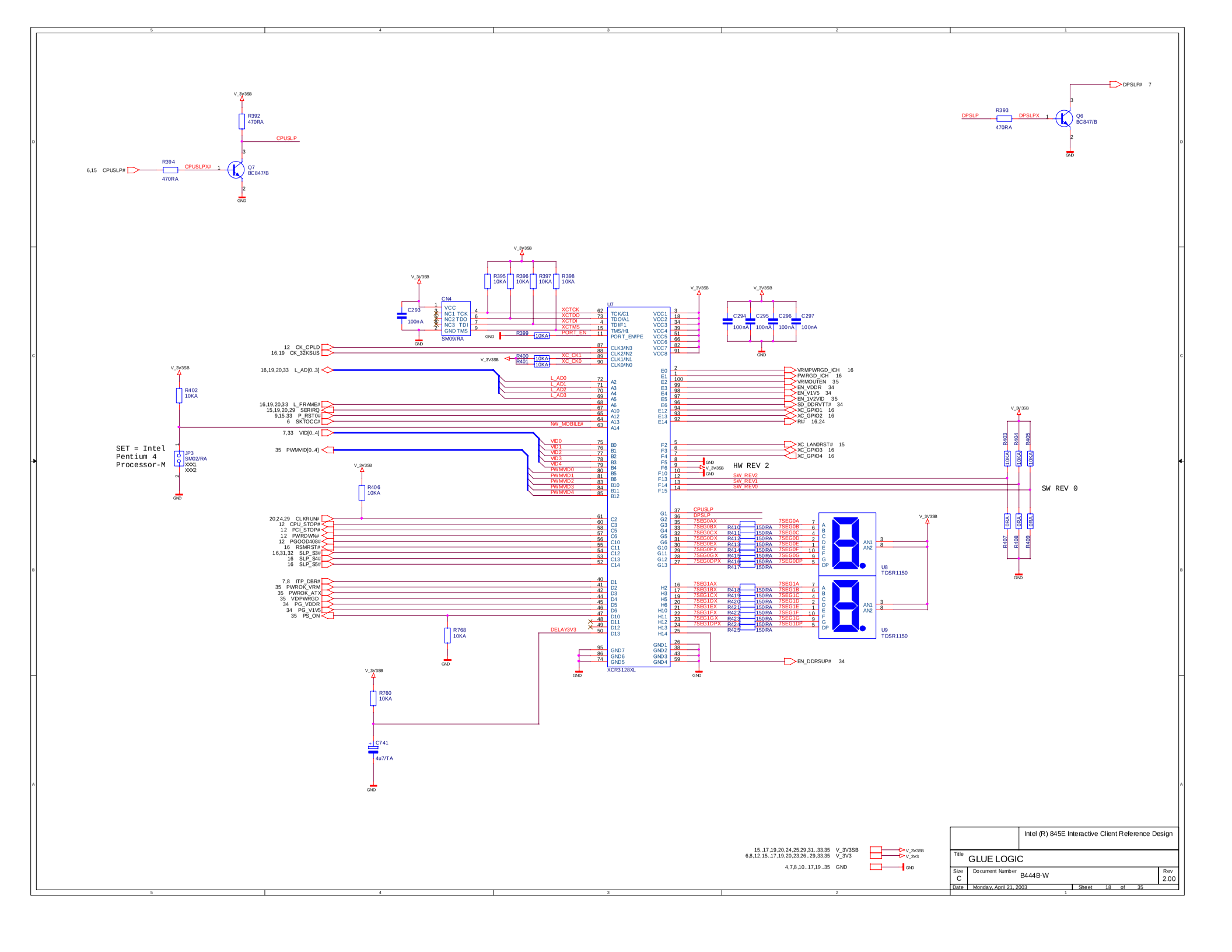


35	V_1V5SB	V_1V5SB
10,11,28,33,34	V_1V5	V_1V5
11,15,33,35	V_1V8	V_1V8
15,16,18..20,24,25,29,31..33,35	V_3V3SB	V_3V3SB
6,8,12,15,16,19,20,23,26..29,33,35	V_3V3	V_3V3
19,21,22,31..35	V_5V0SB	V_5V0SB
19..21,23,25..27,29..35	V_5V0	V_5V0
4,6..8,11,33,35	V_CORE	V_CORE
15,16	V_RTC	V_RTC
16	V_RTCBIAS	V_RTCBIAS
4,7,8,10..16,18..35	GND	GND

	Intel (R) 845E Interactive Client Reference Design	
Title	INTEL ICH4 - 03	
Size: C	Document Number: B444B-W	Rev: 2.00
Date: Monday, April 21, 2003	Sheet 17 of 35	


R392 470RA
CPUSLP
6,15 CPUSLP#
R394 470RA
CPUSLPX#
Q7 BC847/B
DPSLP
R393 470RA
DPSLPX
Q6 BC847/B
DPSLP# 7
R395 10KA
R396 10KA
R397 10KA
R398 10KA
C293 100nA
CN4
SM09/RA
R399 10KA
U7
XCR3128XL
C294 100nA
C295 100nA
C296 100nA
C297 100nA
12 CK_CPLD
16,19 CK_32KSUS
R400 10KA
R401 10KA
XC_CK1
XC_CK0
16,19,20,33 L_AD[0..3]
L_AD0
L_AD1
L_AD2
L_AD3
16,19,20,33 L_FRAME#
15,19,20,29 SERIRQ
9,15,33 P_RST0#
6 SKTOCC#
NW_MOBILE#
7,33 VID[0..4]
35 PWMVID[0..4]
VID0
VID1
VID2
VID3
VID4
PWMVID0
PWMVID1
PWMVID2
PWMVID3
PWMVID4
R402 10KA
JP3 SM02/RA XXX1 XXX2
SET = Intel Pentium 4 Processor-M
R406 10KA
20,2,4,29 CLKRUN#
12 CPU_STOP#
12 PCI_STOP#
12 PWRDWN#
12 PGOOD408#
16 RSMRST#
16,31,32 SLP_S3#
16 SLP_S4#
16 SLP_S5#
7,8 ITP_DBR#
35 PWROK_VRM
35 PWROK_ATX
35 VIDPWRGD
34 PG_VDDR
34 PG_V1V5
35 PS_ON
R768 10KA
DELAY3V3
R760 10KA
C741 4u7/TA
VRMPWRGD_ICH 16
PWRGD_ICH 16
VRMOUTEN 35
EN_VDDR 34
EN_V1V5 34
EN_LV2VID 35
SD_DDRVTT# 34
XC_GPIO1 16
XC_GPIO2 16
R# 16,24
XC_LAN0RST# 15
XC_GPIO3 16
XC_GPIO4 16
HW REV 2
SW_REV2
SW_REV1
SW_REV0
SW REV 0
R403 10KA
R404 10KA
R405 10KA
R407 0RA
R408 0RA
R409 0RA
CPUSLP
DPSLP
7SEG0AX
7SEG0BX
7SEG0CX
7SEG0DX
7SEG0EX
7SEG0FX
7SEG0GX
7SEG0DPX
R410 150RA
R411 150RA
R412 150RA
R413 150RA
R414 150RA
R415 150RA
R416 150RA
R417 150RA
7SEG0A
7SEG0B
7SEG0C
7SEG0D
7SEG0E
7SEG0F
7SEG0G
7SEG0DP
U8 TDSR1150
7SEG1AX
7SEG1BX
7SEG1CX
7SEG1DX
7SEG1EX
7SEG1FX
7SEG1GX
7SEG1DPX
R418 150RA
R419 150RA
R420 150RA
R421 150RA
R422 150RA
R423 150RA
R424 150RA
R425 150RA
7SEG1A
7SEG1B
7SEG1C
7SEG1D
7SEG1E
7SEG1F
7SEG1G
7SEG1DP
U9 TDSR1150
EN_DDRSUP# 34
15..17,19,20,24,25,29,31..33,35 V_3V3SB
6,8,12,15..17,19,20,23,26..29,33,35 V_3V3
4,7,8,10..17,19..35 GND
Intel (R) 845E Interactive Client Reference Design
GLUE LOGIC
Size C
Document Number B444B-W
Rev 2.00
Date Monday, April 21, 2003
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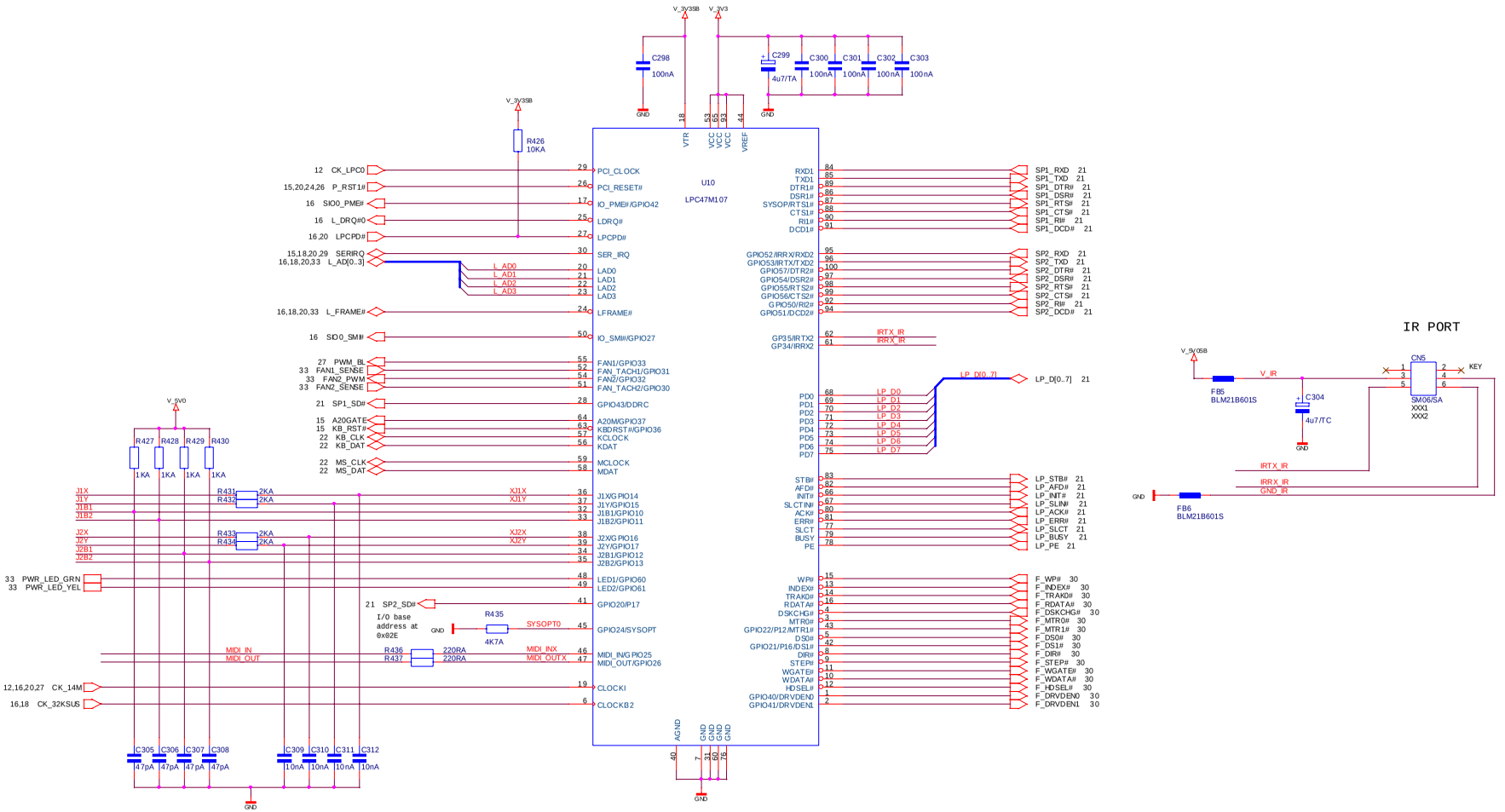
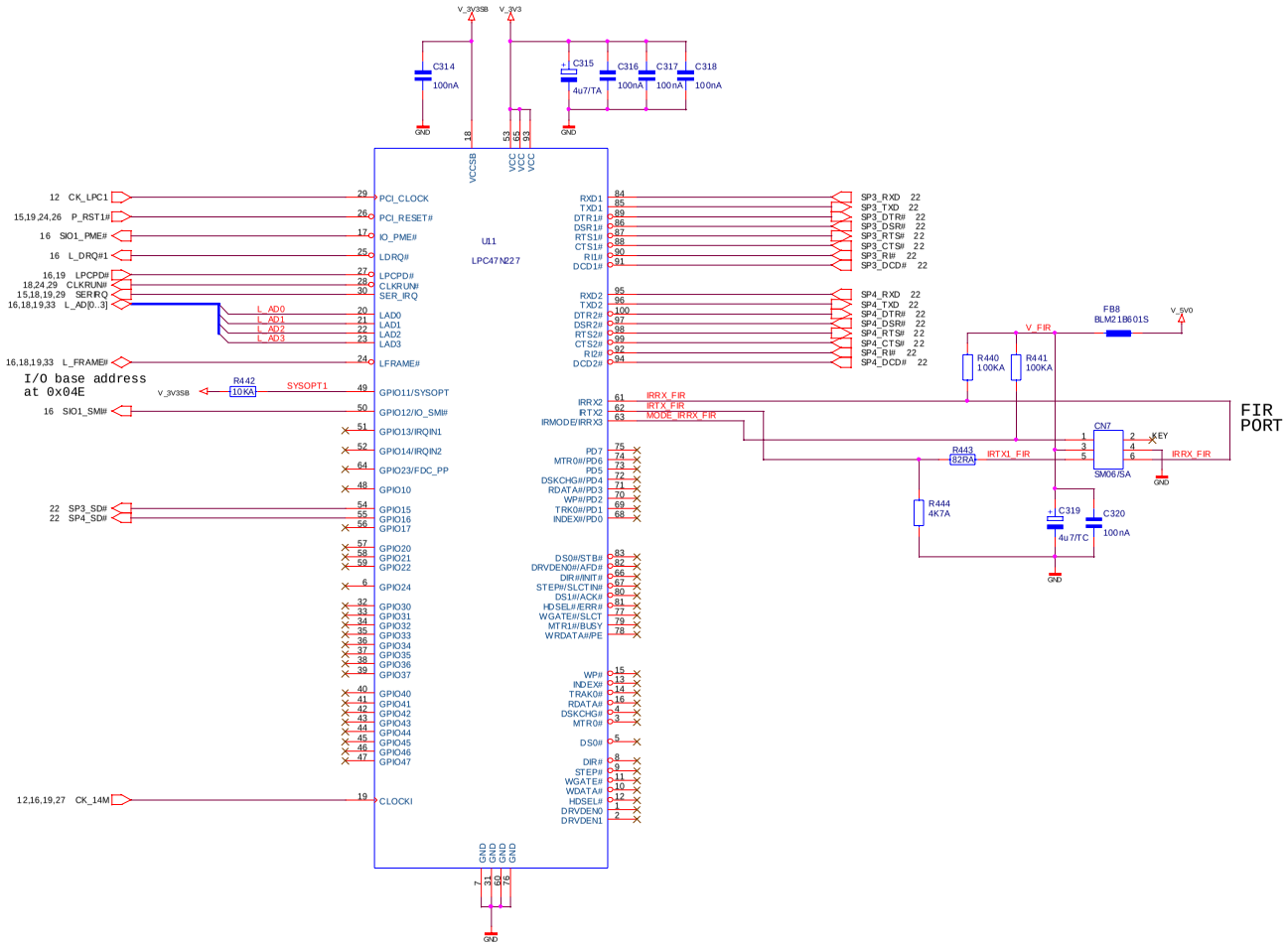

U10
LPC47M107
C298 100nA
C299 4u7/TA
C300 100nA
C301 100nA
C302 100nA
C303 100nA
R426 10KA
R427 R428 R429 R430 1KA
C305 C306 C307 C308 47pA
C309 C310 C311 C312 10nA
R431 R432 R433 R434 2KA
R435 4K7A
R436 R437 220RA
I/O base address at 0x02E
PCI_CLOCK
PCI_RESET#
IO_PME#/GPIO42
LDRQ#
LPCPD#
SER_IRQ
LAD0
LAD1
LAD2
LAD3
LFRAME#
IO_SMI#/GPIO27
FAN1/GPIO33
FAN_TACH1/GPIO31
FAN2/GPIO32
FAN_TACH2/GPIO30
GPIO43/DDRC
A20M/GPIO37
KBDRST#/GPIO36
KCLOCK
KDAT
MCLOCK
MDAT
J1X/GPIO14
J1Y/GPIO15
J1B1/GPIO10
J1B2/GPIO11
J2X/GPIO16
J2Y/GPIO17
J2B1/GPIO12
J2B2/GPIO13
LED1/GPIO60
LED2/GPIO61
GPIO20/P17
GPIO24/SYSOPT
MIDI_IN/GPIO25
MIDI_OUT/GPIO26
CLOCKI
CLOCKB2
RXD1
TXD1
DTR1#
DSR1#
SYSOP/RTS1#
CTS1#
RI1#
DCD1#
GPIO52/IRRX/RXD2
GPIO53/IRTX/TXD2
GPIO57/DTR2#
GPIO54/DSR2#
GPIO55/RTS2#
GPIO56/CTS2#
GPIO50/RI2#
GPIO51/DCD2#
GP35/IRTX2
GP34/IRRX2
PD0 PD1 PD2 PD3 PD4 PD5 PD6 PD7
STB#
AFD#
INIT#
SLCTIN#
ACK#
ERR#
SLCT
BUSY
PE
WP#
INDEX#
TRAK0#
RDATA#
DSKCHG#
MTR0#
GPIO22/P12/MTR1#
DS0#
GPIO21/P16/DS1#
DIR#
STEP#
WGATE#
WDATA#
HDSEL#
GPIO40/DRVDEN0
GPIO41/DRVDEN1
IR PORT
FB5 BLM21B601S
C304 4u7/TC
CN5 SM06/5A
FB6 BLM21B601S
F1 SMD075-2
FB7 BLM21B601S
C313 4u7/TC
CN6 SM16/WA
R439 R438 2KA
GAME PORT/MIDI
Intel (R) 845E Interactive Client Reference Design
SIO0-LPC47M107
B444B-W
Monday, April 21, 2003



17,19,21,23,25..27,29..35 V_5V0
15..19,24,25,2 9,31..33,35 V_3V3SB
6,8,12,15..17,19,2 3,26..29,33,35 V_3V3
4,7,8,10..19,21..35 GND

	Intel (R) 845E Interactive Client Reference Design
Title	SIO1-LPC47N227
Size: C	Document Number: B444B-W
Rev	2.00
Date	Monday, April 21, 2003
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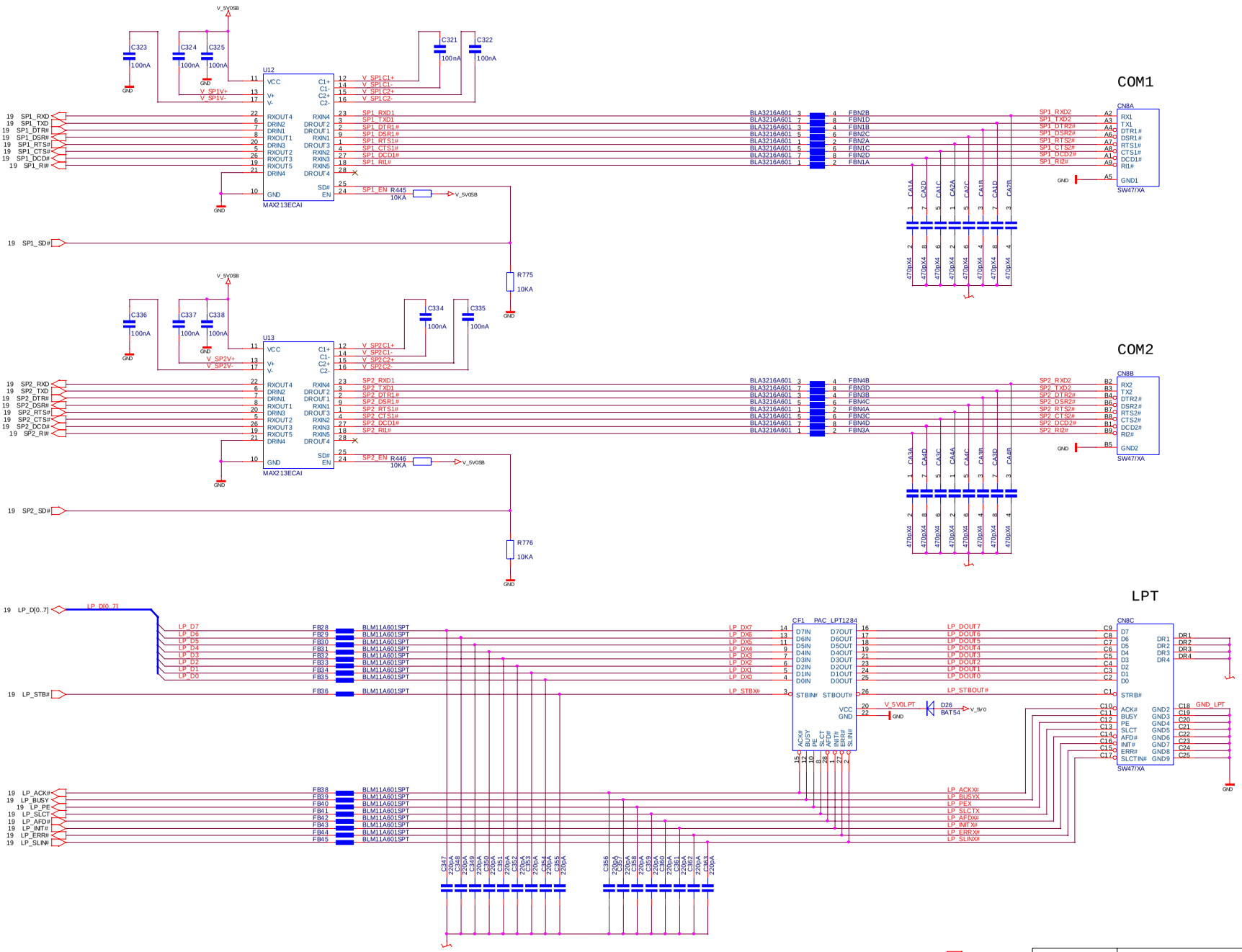
COM1
COM2
LPT
U12
U13
MAX213ECAI
CN8A
CN8B
CN8C
SW47/XA
CF1 PAC_LPT1284
V_5V0SB
V_5V0
GND
SP1_EN
SP2_EN
R445 10KA
R446 10KA
R775 10KA
R776 10KA
BLM11A601SPT
470pX4
100nA
220pA
D26 BAT54
V_5VOLPT
LP_STBOUT#
LP_D[0..7]
LP_STB#
LP_ACK#
LP_BUSY
LP_PE
LP_SLCT
LP_AFD#
LP_INIT#
LP_ERR#
LP_SLIN#
Intel (R) 845E Interactive Client Reference Design
CONN COM1/COM2/LPT
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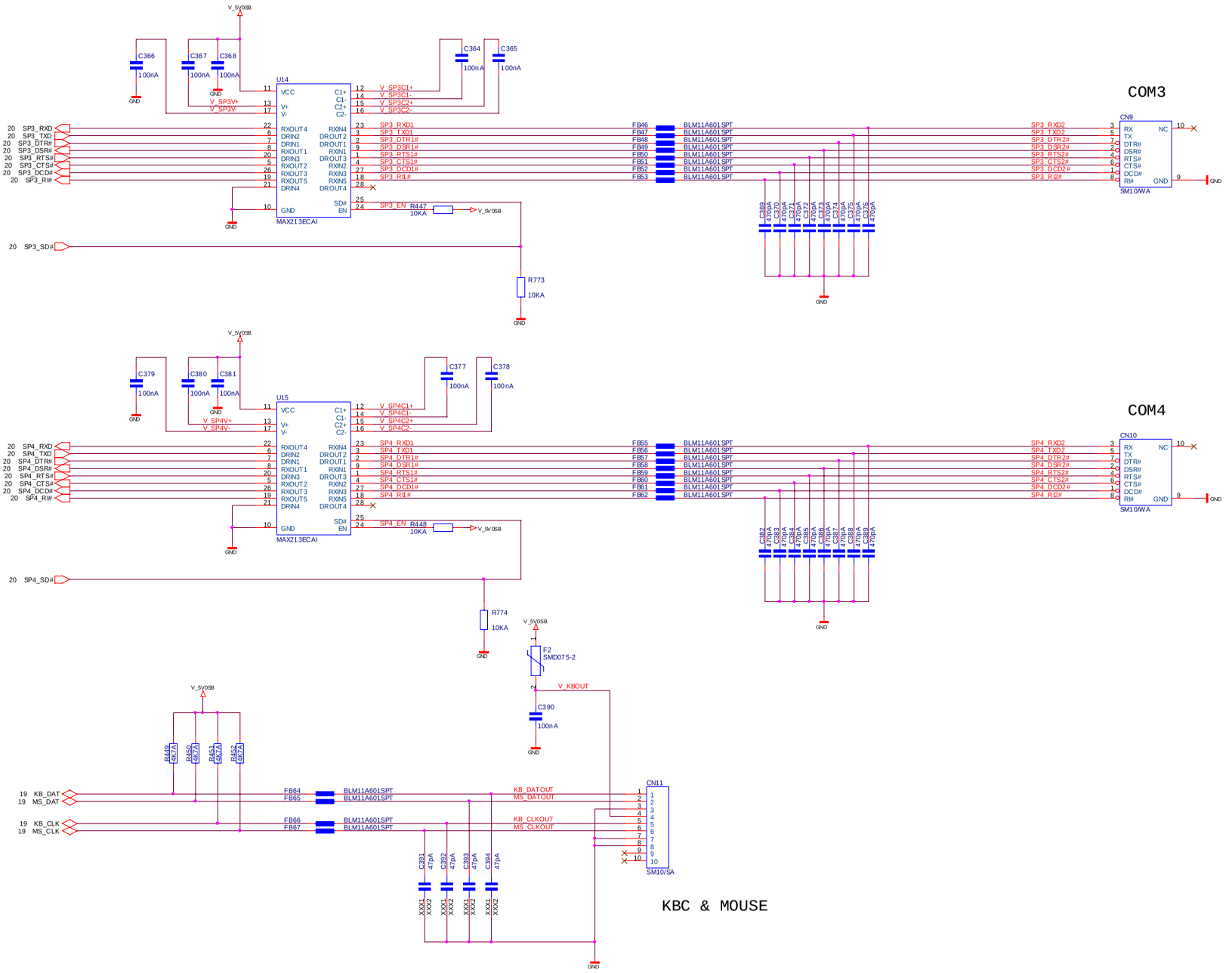

17,19,21,31..35 V_5VOSB
4,7,8,10..21,23..35 GND
2,1,23,25,27,31,32 SHIELD

	Intel (R) 845E Interactive Client Reference Design
Title	CONN COM3/COM4/KBC
Size: C	Document Number: B444B-W
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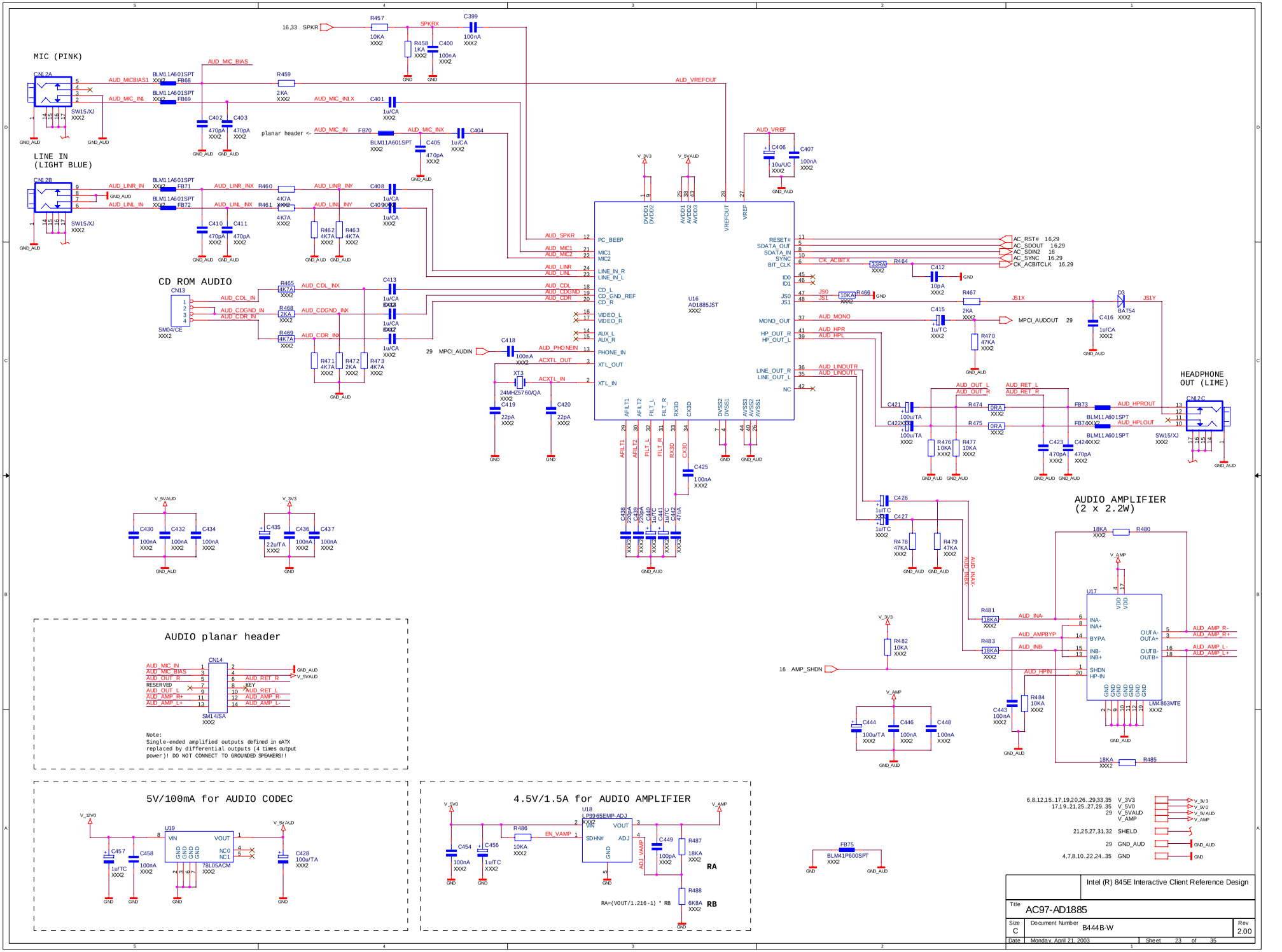
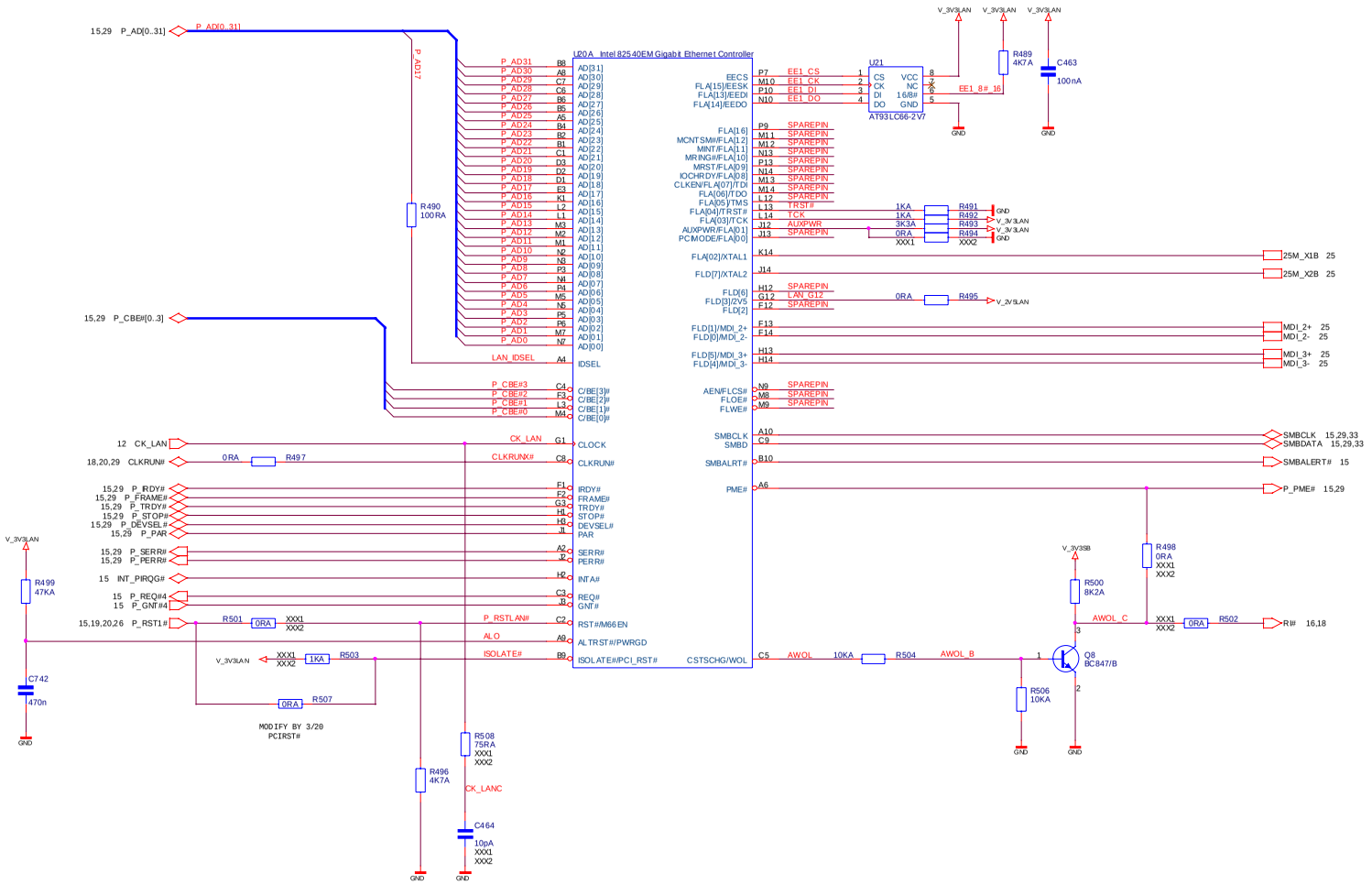
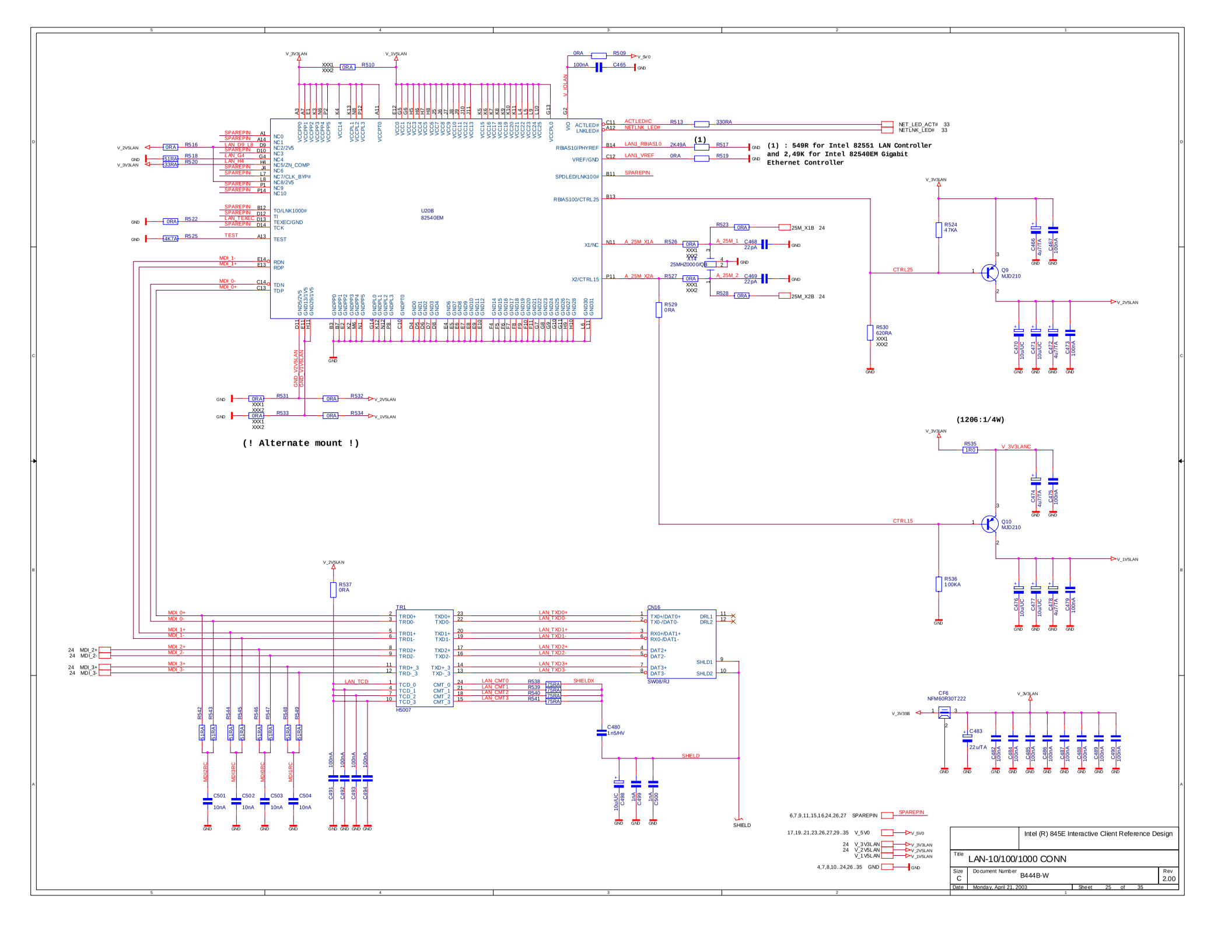

MIC (PINK)
LINE IN
(LIGHT BLUE)
CD ROM AUDIO
HEADPHONE
OUT (LIME)
AUDIO AMPLIFIER
(2 x 2.2W)
AUDIO planar header
5V/100mA for AUDIO CODEC
4.5V/1.5A for AUDIO AMPLIFIER
U16
AD1885JST
XXX2
Note:
Single-ended amplified outputs defined in eATX
replaced by differential outputs (4 times output
power)! DO NOT CONNECT TO GROUNDED SPEAKERS!!
RA=(VOUT/1.216-1) * RB
Intel (R) 845E Interactive Client Reference Design
AC97-AD1885
B444B-W
Monday, April 21, 2003
Sheet 23 of 35



	Intel (R) 845E Interactive Client Reference Design
Title	LAN-10/100/1000 BUS
Size C	Document Number B444B-W — Rev 2.00
Date Monday, April 21, 2003	Sheet 24 of 35


U20B
82540EM
(1) : 549R for Intel 82551 LAN Controller and 2,49K for Intel 82540EM Gigabit Ethernet Controller
(! Alternate mount !)
(1206:1/4W)
TR1
H5007
CN16
SW08/RJ
CF6
NFM60R30T222
Intel (R) 845E Interactive Client Reference Design
LAN-10/100/1000 CONN
B444B-W
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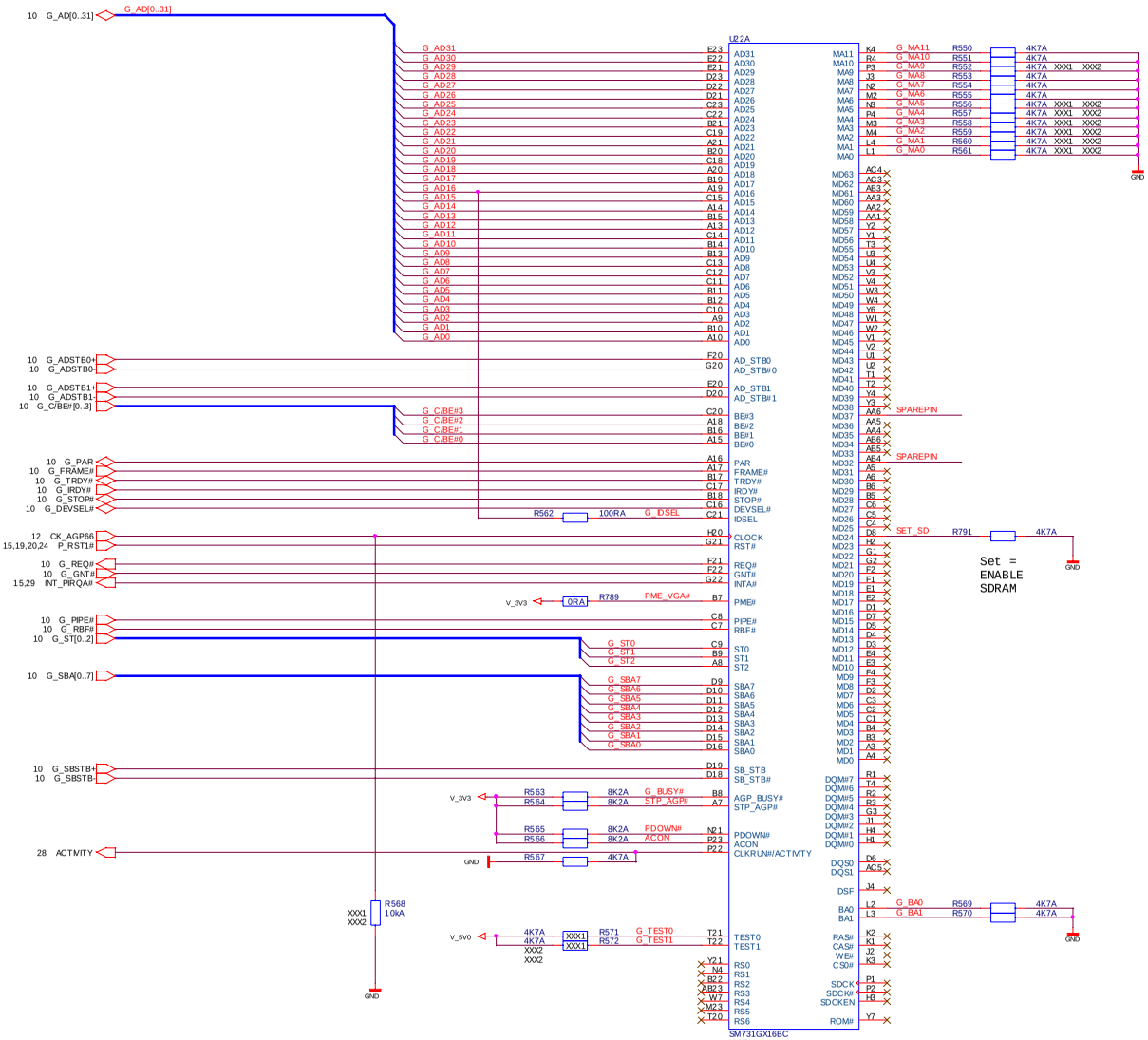

	Intel (R) 845E Interactive Client Reference Design
Title	VGA SM731 - 01
Size C	Document Number B444B-W
Rev	2.00
Date	Monday, April 21, 2003
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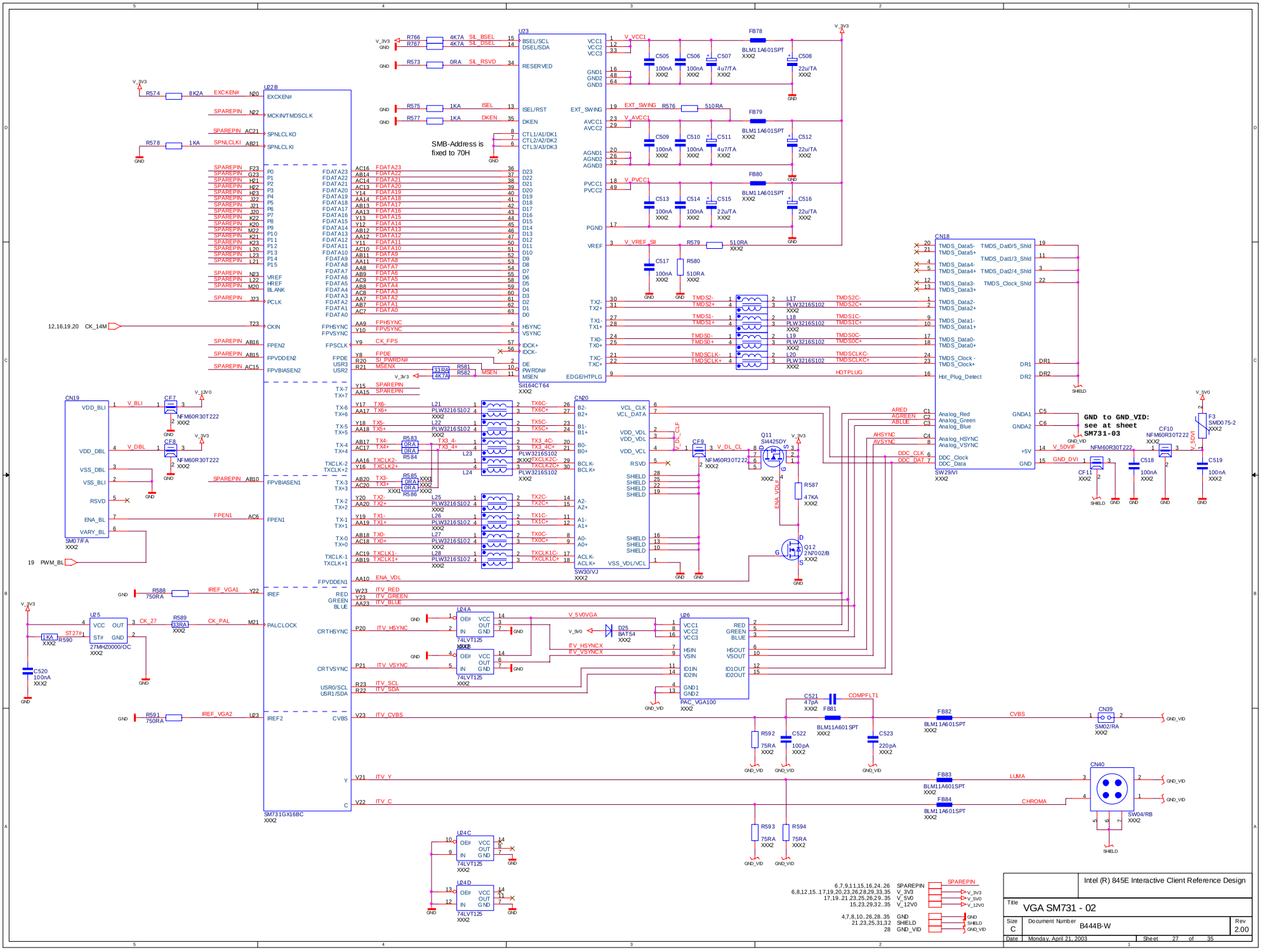
U23
BSEL/SCL
DSEL/SDA
RESERVED
CTL1/A1/DK1
CTL2/A2/DK2
CTL3/A3/DK3
ISEL/RST
DKEN
SMB-Address is fixed to 70H
Sii164CT64
XXX2
U22B
EXCKEN#
MCKIN/TMDSCLK
SPNLCLKO
SPNLCLKI
SM731GX16BC
XXX2
CN18
TMDS_Data5-
TMDS_Data5+
TMDS_Data4-
TMDS_Data4+
TMDS_Data3-
TMDS_Data3+
TMDS_Clock -
TMDS_Clock+
Hot_Plug_Detect
TMDS_Dat0/5_Shld
TMDS_Dat1/3_Shld
TMDS_Dat2/4_Shld
TMDS_Clock_Shld
SW29/VI
XXX2
CN19
VDD_BLI
VDD_DBL
VSS_DBL
VSS_BLI
RSVD
ENA_BL
VARY_BL
SM07/IFA
XXX2
CN20
VCL_CLK
VCL_DATA
VDD_VDL
VDD_VCL
RSVD
SHIELD
BCLK-
BCLK+
SW30/VJ
XXX2
U25
27MHZ0000/OC
XXX2
U24A
U24B
U24C
U24D
74LVT125
XXX2
U26
HSIN
VSIN
ID1IN
ID2IN
HSOUT
VSOUT
ID1OUT
ID2OUT
PAC_VGA100
XXX2
CN39
SM02/RA
XXX2
CN40
SW04/RB
XXX2
Q11
SI4425DY
Q12
2N7002/B
XXX2
CF7
CF8
CF9
CF10
CF11
NFM60R30T222
XXX2
L17
L18
L19
L20
L21
L22
L23
L24
L25
L26
L27
L28
PLW3216S102
XXX2
F3
SMD075-2
XXX2
GND to GND_VID:
see at sheet
SM731-03
Intel (R) 845E Interactive Client Reference Design
VGA SM731 - 02
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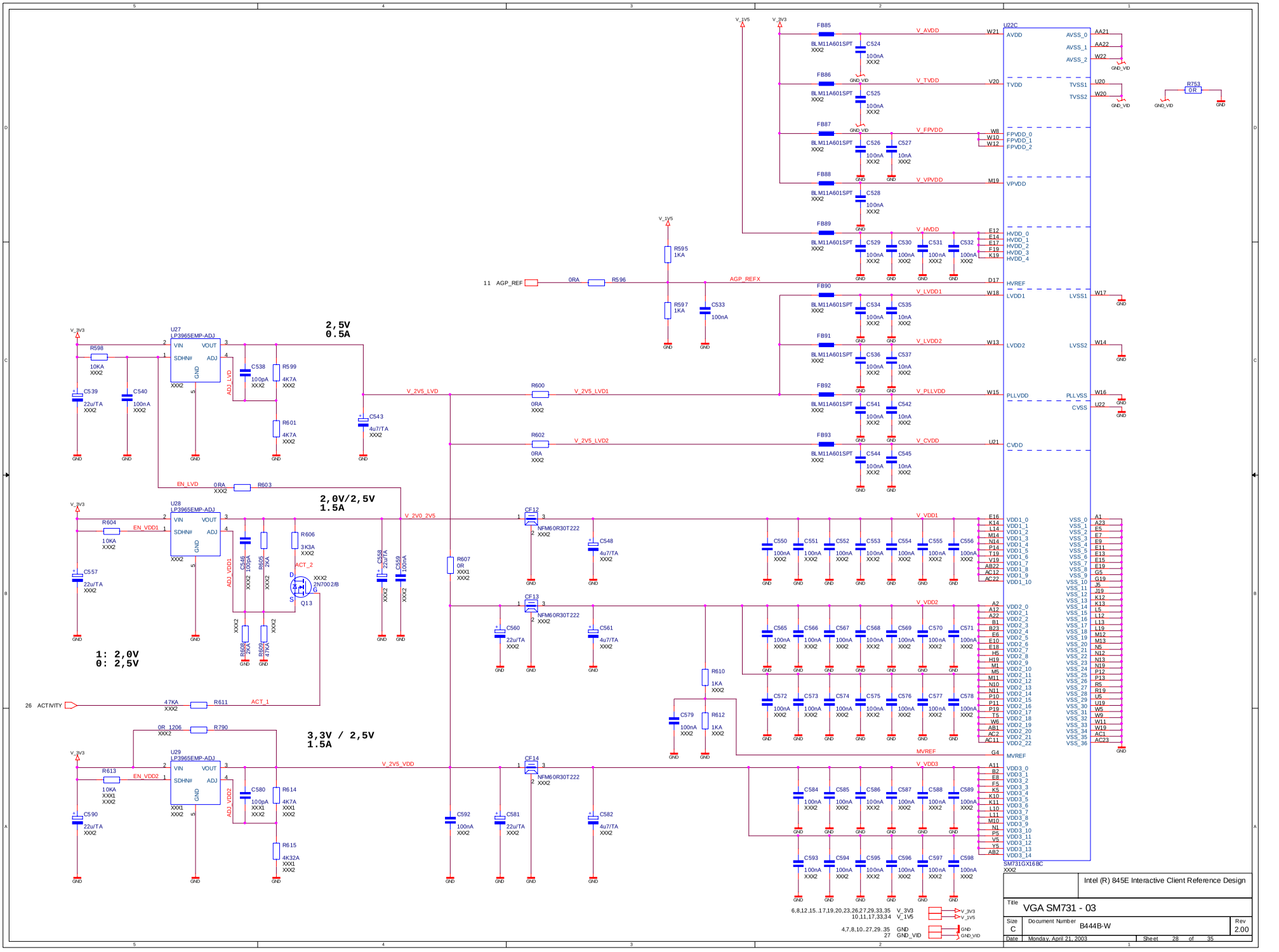
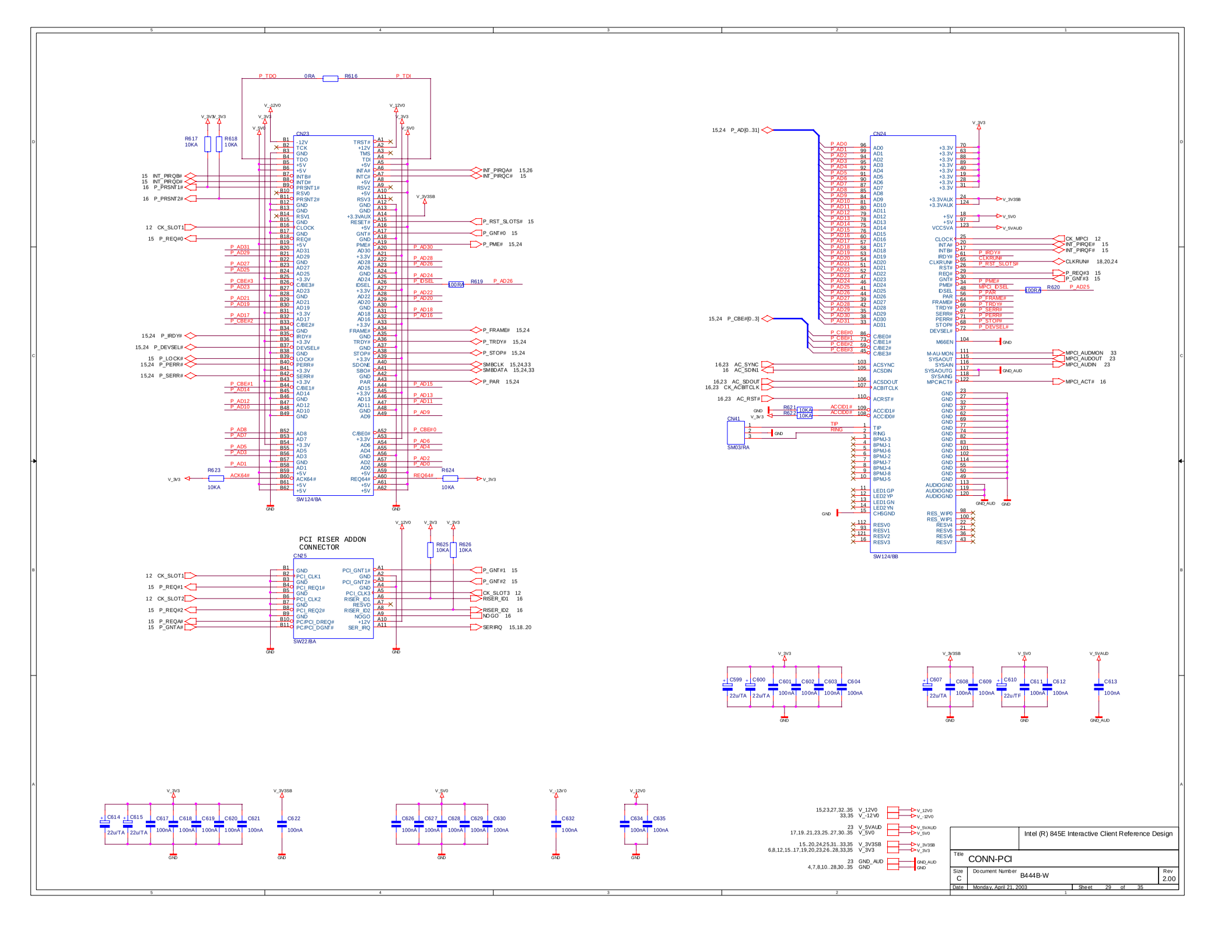

2,5V
0.5A
2,0V/2,5V
1.5A
3,3V / 2,5V
1.5A
1: 2,0V
0: 2,5V
U27
LP3965EMP-ADJ
U28
LP3965EMP-ADJ
U29
LP3965EMP-ADJ
U22C
SM731GX16BC
V_3V3
V_1V5
V_AVDD
V_TVDD
V_FPVDD
V_VPVDD
V_HVDD
V_LVDD1
V_LVDD2
V_PLLVDD
V_CVDD
V_VDD1
V_VDD2
V_VDD3
MVREF
AGP_REF
AGP_REFX
V_2V5_LVD
V_2V5_LVD1
V_2V5_LVD2
V_2V0_2V5
V_2V5_VDD
EN_LVD
EN_VDD1
EN_VDD2
ACTIVITY
ACT_1
ACT_2
Intel (R) 845E Interactive Client Reference Design
VGA SM731 - 03
B444B-W
Monday, April 21, 2003


P_TDO
0RA
R616
P_TDI
CN23
SW124/BA
PCI RISER ADDON CONNECTOR
CN25
SW22/BA
CN24
SW124/BB
CN41
SM03/RA
Intel (R) 845E Interactive Client Reference Design
CONN-PCI
B444B-W
2.00
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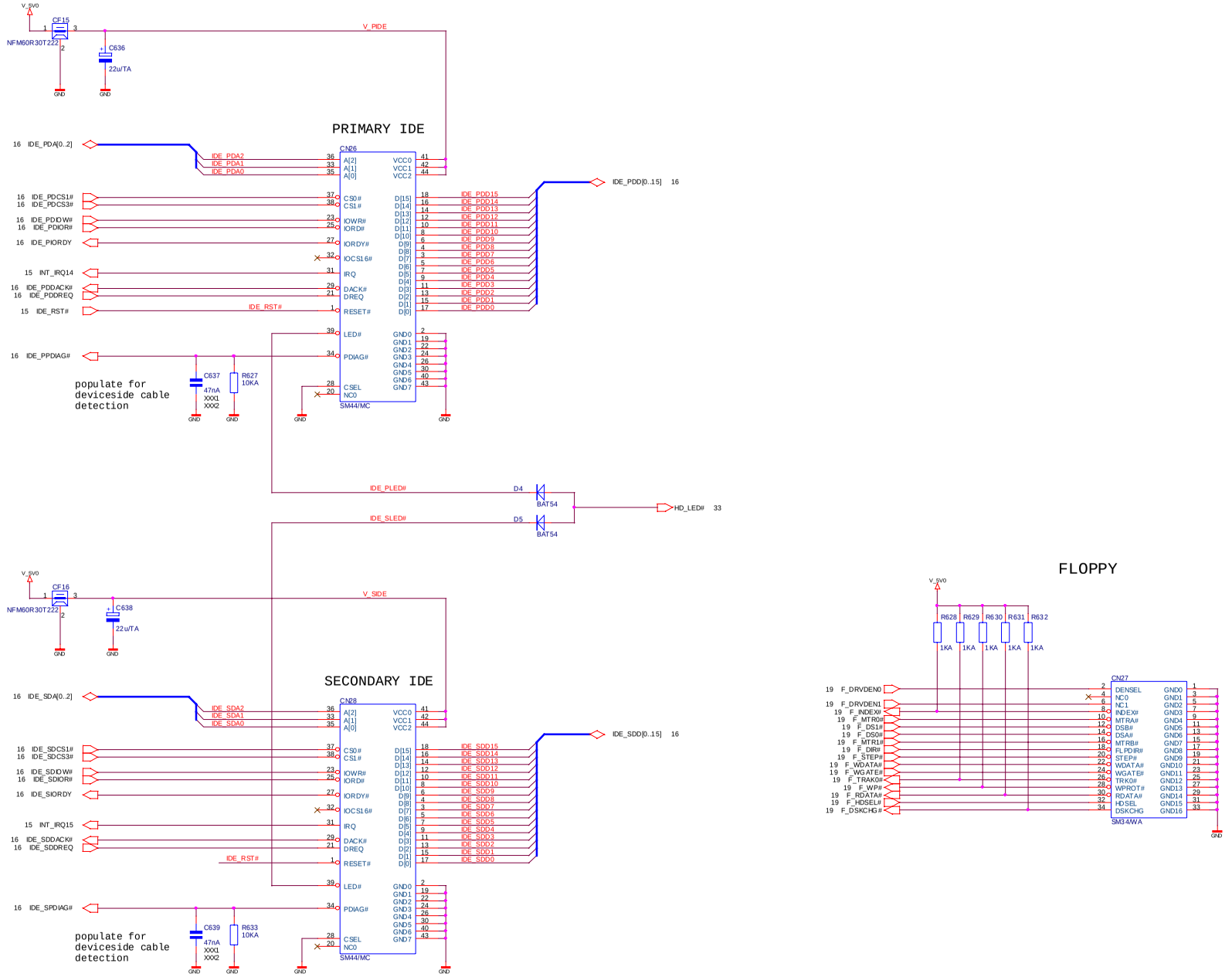
PRIMARY IDE
SECONDARY IDE
FLOPPY
V_5V0
V_PIDE
V_SIDE
CF15
CF16
NFM60R30T222
C636
C638
22u/TA
CN26
CN28
SM44/MC
IDE_PDA[0..2]
IDE_SDA[0..2]
IDE_PDD[0..15]
IDE_SDD[0..15]
IDE_PDCS1#
IDE_PDCS3#
IDE_PDIOW#
IDE_PDIOR#
IDE_PIORDY
INT_IRQ14
IDE_PDDACK#
IDE_PDDREQ
IDE_RST#
IDE_PPDIAG#
IDE_SDCS1#
IDE_SDCS3#
IDE_SDIOW#
IDE_SDIOR#
IDE_SIORDY
INT_IRQ15
IDE_SDDACK#
IDE_SDDREQ
IDE_SPDIAG#
IDE_PLED#
IDE_SLED#
D4
D5
BAT54
HD_LED#
populate for deviceside cable detection
C637
C639
47nA
R627
R633
10KA
R628
R629
R630
R631
R632
1KA
CN27
SM34/WA
F_DRVDEN0
F_DRVDEN1
F_INDEX#
F_MTR0#
F_DS1#
F_DS0#
F_MTR1#
F_DIR#
F_STEP#
F_WDATA#
F_WGATE#
F_TRAK0#
F_WP#
F_RDATA#
F_HDSEL#
F_DSKCHG#
17,19..21,23,25..27,29,31..35 V_5V0
17,19,21,22,31..35 V_5V0SB
4,7,8,10..29,31..35 GND
Intel (R) 845E Interactive Client Reference Design
CONN-01 IDE-FLOPPY
B444B-W
2.00
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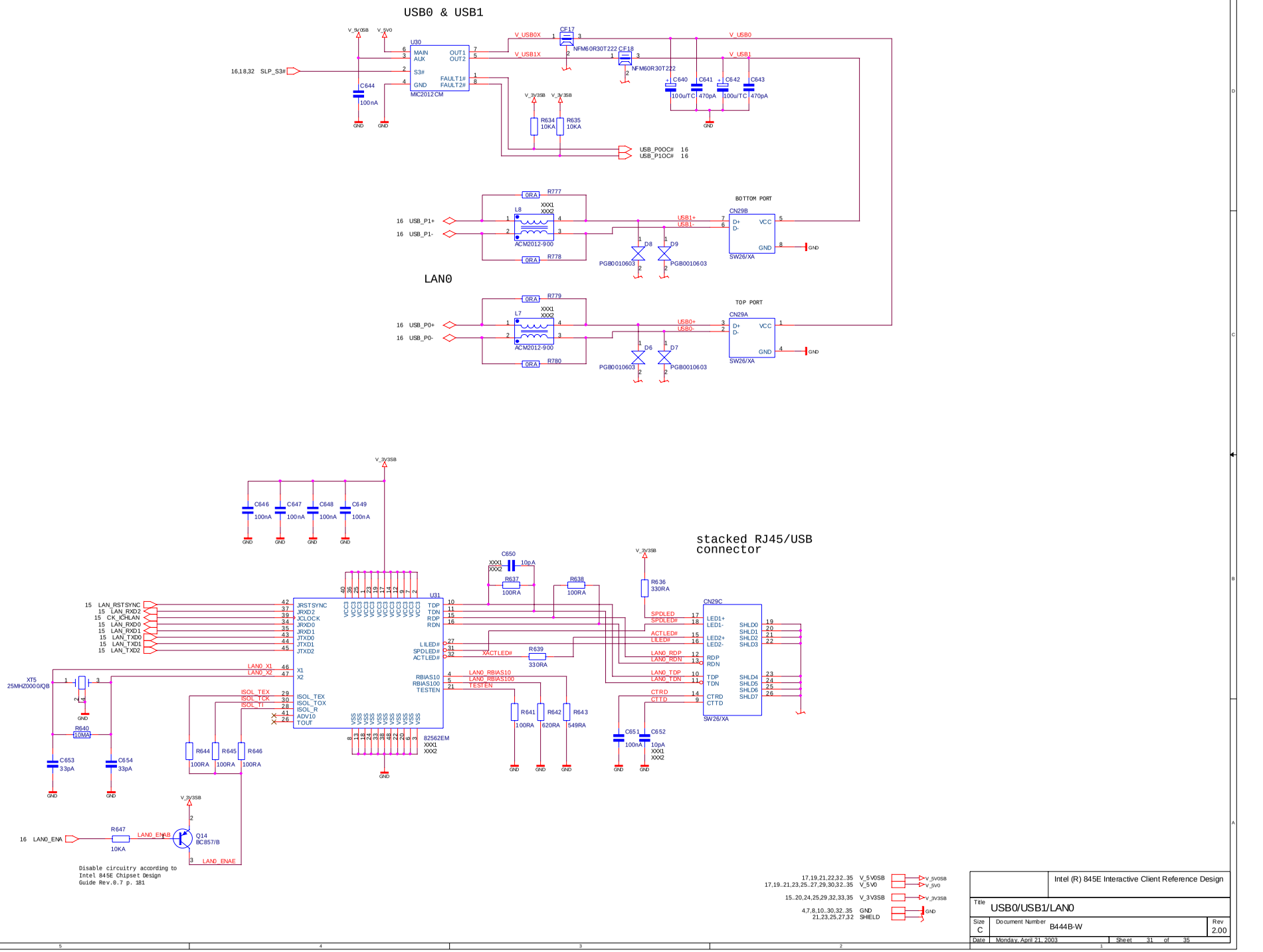
USB0 & USB1
U30
MIC2012CM
MAIN
AUX
S3#
GND
OUT1
OUT2
FAULT1#
FAULT2#
SLP_S3#
V_USB0X
V_USB1X
V_USB0
V_USB1
CF17
CF18
NFM60R30T222
C644
100nA
C640
C641
C642
C643
100u/TC
470pA
R634
10KA
R635
10KA
USB_P0OC#
USB_P1OC#
R777
R778
0RA
L8
XXX1
XXX2
ACM2012-900
USB_P1+
USB_P1-
USB1+
USB1-
D8
D9
PGB0010603
BOTTOM PORT
CN29B
SW26/XA
LAN0
R779
R780
L7
USB_P0+
USB_P0-
USB0+
USB0-
D6
D7
TOP PORT
CN29A
stacked RJ45/USB
connector
C646
C647
C648
C649
C650
10pA
R637
R638
100RA
330RA
R636
CN29C
LAN_RSTSYNC
LAN_RXD2
CK_ICHLAN
LAN_RXD0
LAN_RXD1
LAN_TXD0
LAN_TXD1
LAN_TXD2
JRSTSYNC
JRXD2
JCLOCK
JRXD0
JRXD1
JTXD0
JTXD1
JTXD2
U31
TDP
TDN
RDP
RDN
LILED#
SPDLED#
ACTLED#
XXACTLED#
R639
LAN0_RDP
LAN0_RDN
LAN0_TDP
LAN0_TDN
CTRD
CTTD
LED1+
LED1-
LED2+
LED2-
SHLD0
SHLD1
SHLD2
SHLD3
SHLD4
SHLD5
SHLD6
SHLD7
LAN0_X1
LAN0_X2
X1
X2
XT5
25MHZ0000/QB
R640
10MA
C653
33pA
C654
33pA
ISOL_TEX
ISOL_TCK
ISOL_TI
ISOL_TEX
ISOL_TOX
ISOL_R
ADV10
TOUT
RBIAS10
RBIAS100
TESTEN
LAN0_RBIAS10
LAN0_RBIAS100
R641
R642
R643
100RA
620RA
549RA
82562EM
R644
R645
R646
C651
C652
100nA
R647
10KA
LAN0_ENA
LAN0_ENAB
Q14
BC857/B
Disable circuitry according to
Intel 845E Chipset Design
Guide Rev.0.7 p. 181
17,19,21,22,32..35 V_5VOSB
17,19..21,23,25..27,29,30,32..35 V_5V0
15..20,24,25,29,32,33,35 V_3V3SB
4,7,8,10..30,32..35 GND
21,23,25,27,32 SHIELD
Intel (R) 845E Interactive Client Reference Design
Title
USB0/USB1/LAN0
Size
C
Document Number
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Rev
2.00
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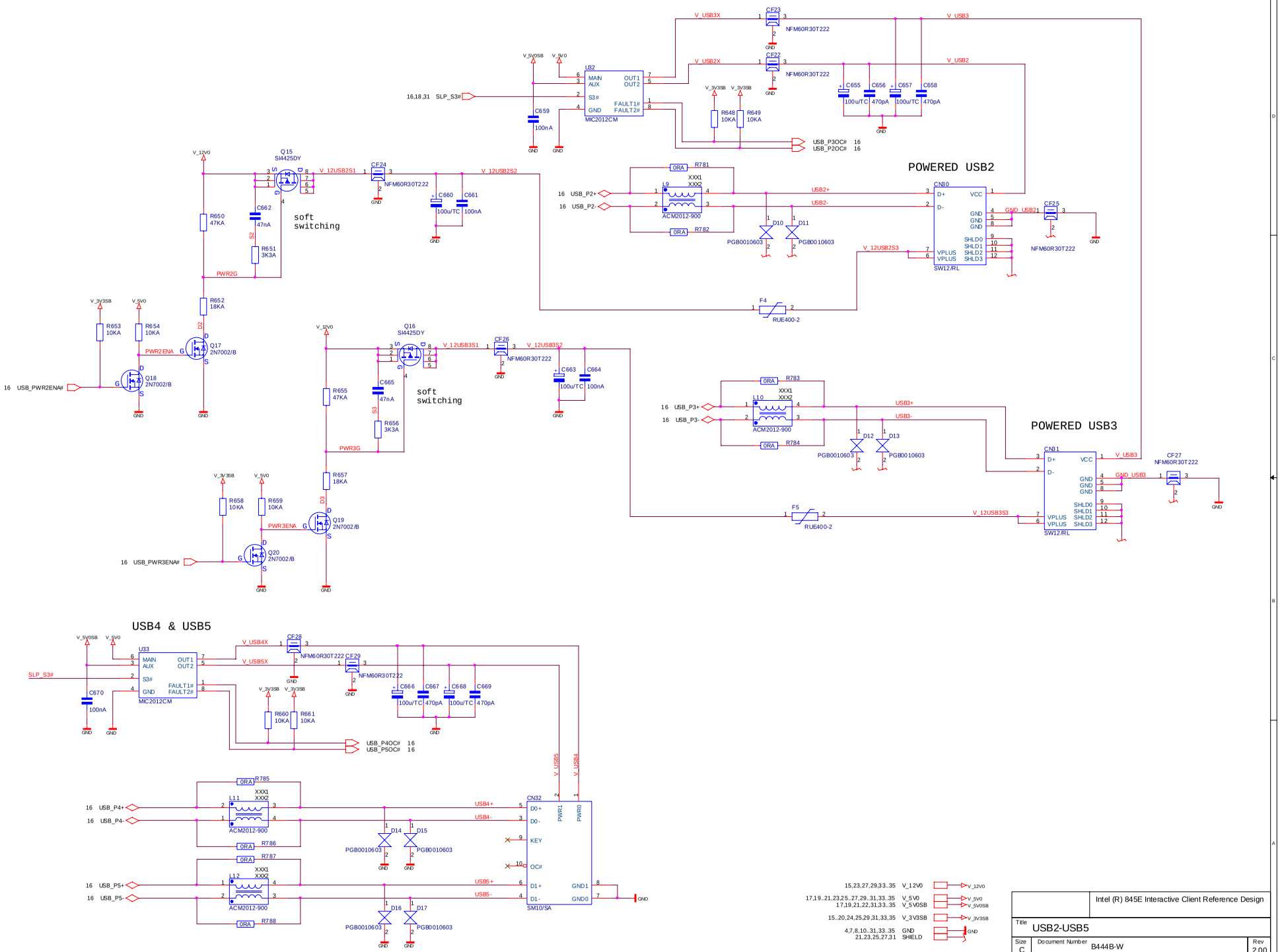
35


POWERED USB2
POWERED USB3
USB4 & USB5
soft switching
soft switching
U2
MIC2012CM
U33
MIC2012CM
Q15 SI4425DY
Q16 SI4425DY
Q17 2N7002/B
Q18 2N7002/B
Q19 2N7002/B
Q20 2N7002/B
CN30
CN31
CN32
SW12/RL
SM10/SA
ACM2012-900
PGB0010603
RUE400-2
NFM60R30T222
V_12V0
V_5V0
V_3V3SB
V_5V0SB
V_USB2
V_USB3
V_USB4
V_USB5
PWR2G
PWR3G
PWR2ENA
PWR3ENA
SLP_S3#
USB_P2OC#
USB_P3OC#
USB_P4OC#
USB_P5OC#
USB_PWR2ENA#
USB_PWR3ENA#
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USB2-USB5
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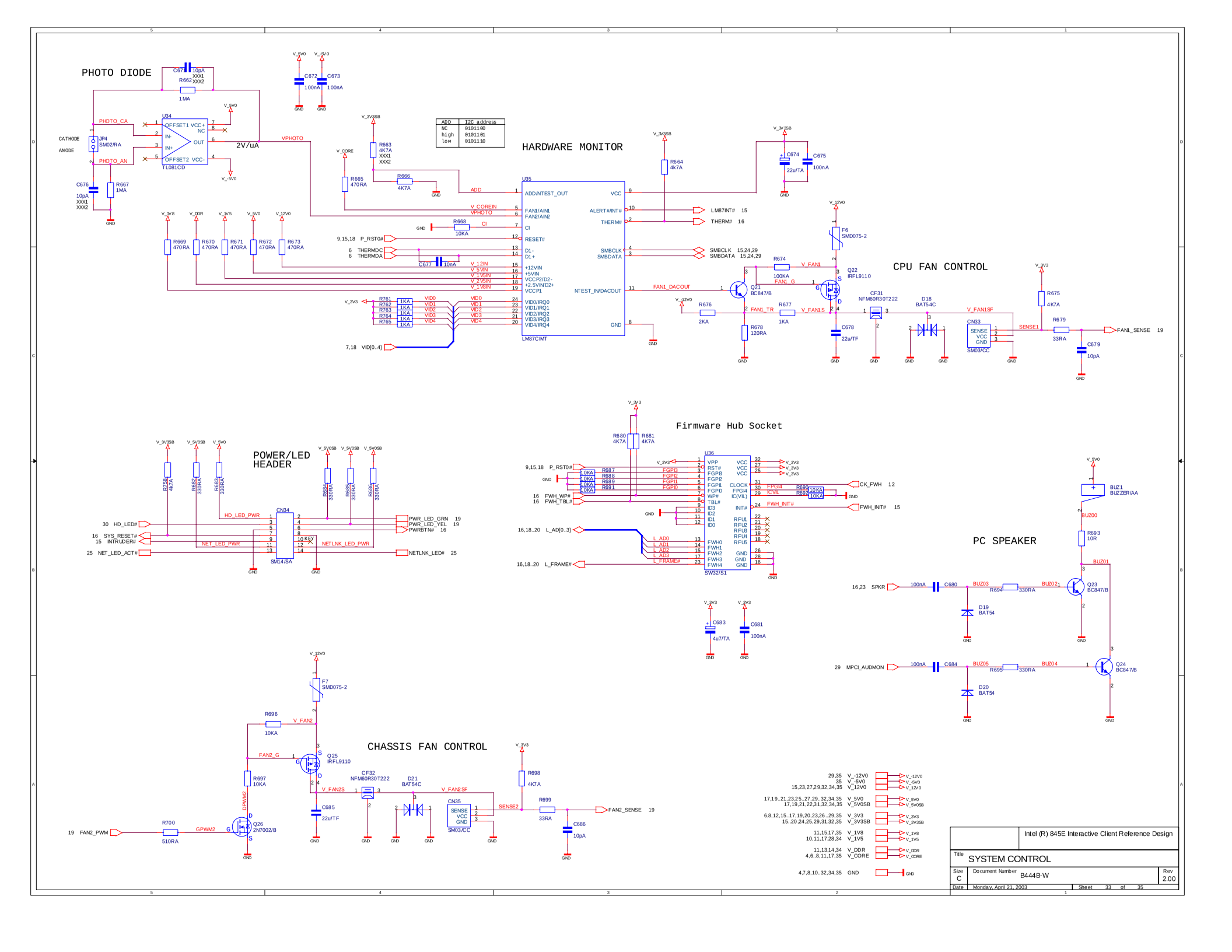
PHOTO DIODE
HARDWARE MONITOR
CPU FAN CONTROL
POWER/LED HEADER
Firmware Hub Socket
PC SPEAKER
CHASSIS FAN CONTROL
Intel (R) 845E Interactive Client Reference Design
SYSTEM CONTROL
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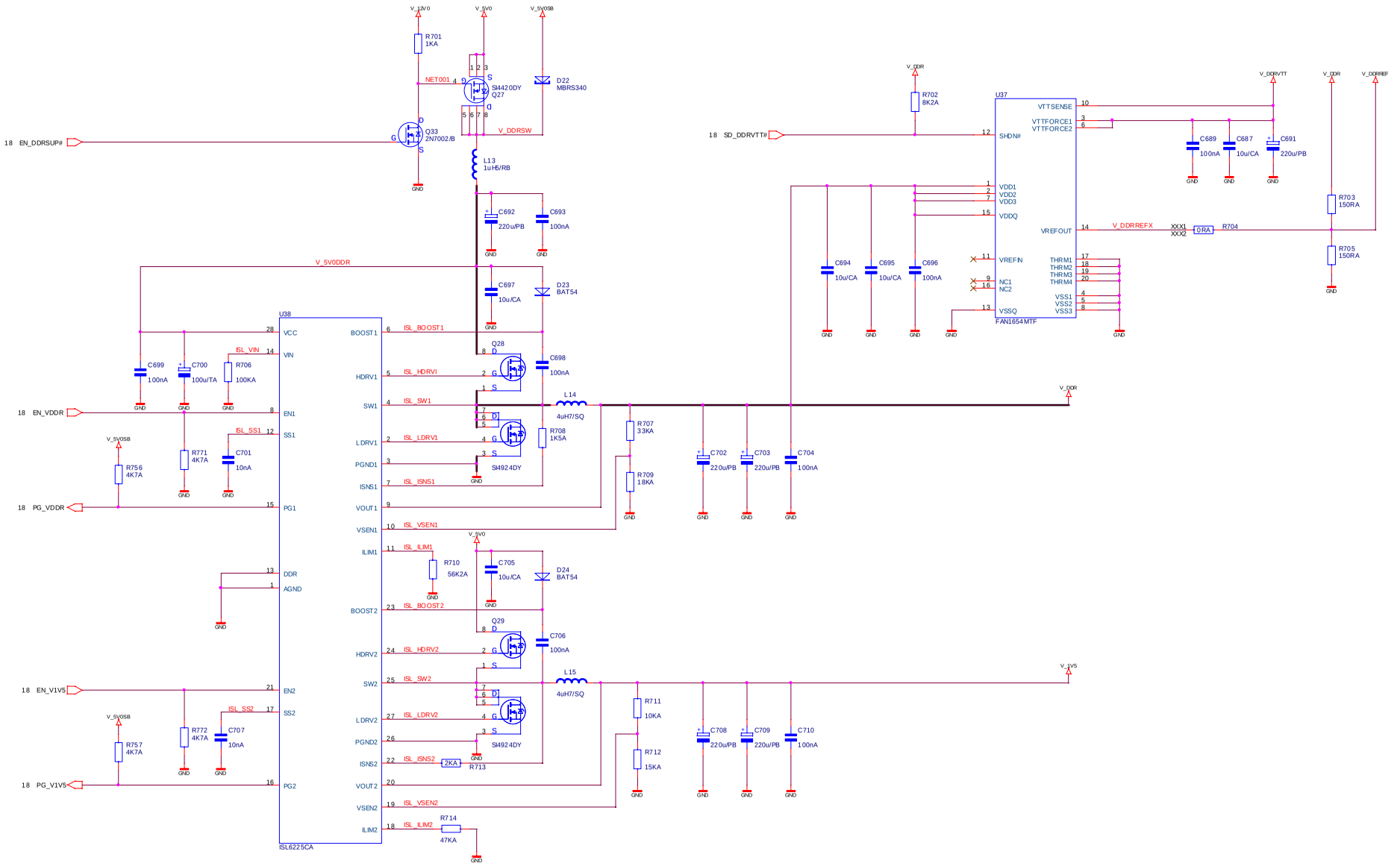

15,23,27,29,32,33,35 V_12V0
17,19..21,23,25..27,29..33,35 V_5V0
17,19,21,22,31..33,35 V_5V0SB
10,11,17,28,33 V_1V5
11,13,14,33 V_DDR
11,14 V_DDRVTT
11,13,14 V_DDRREF
4,7,8,10..33,35 GND

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Title	DDR POWER	
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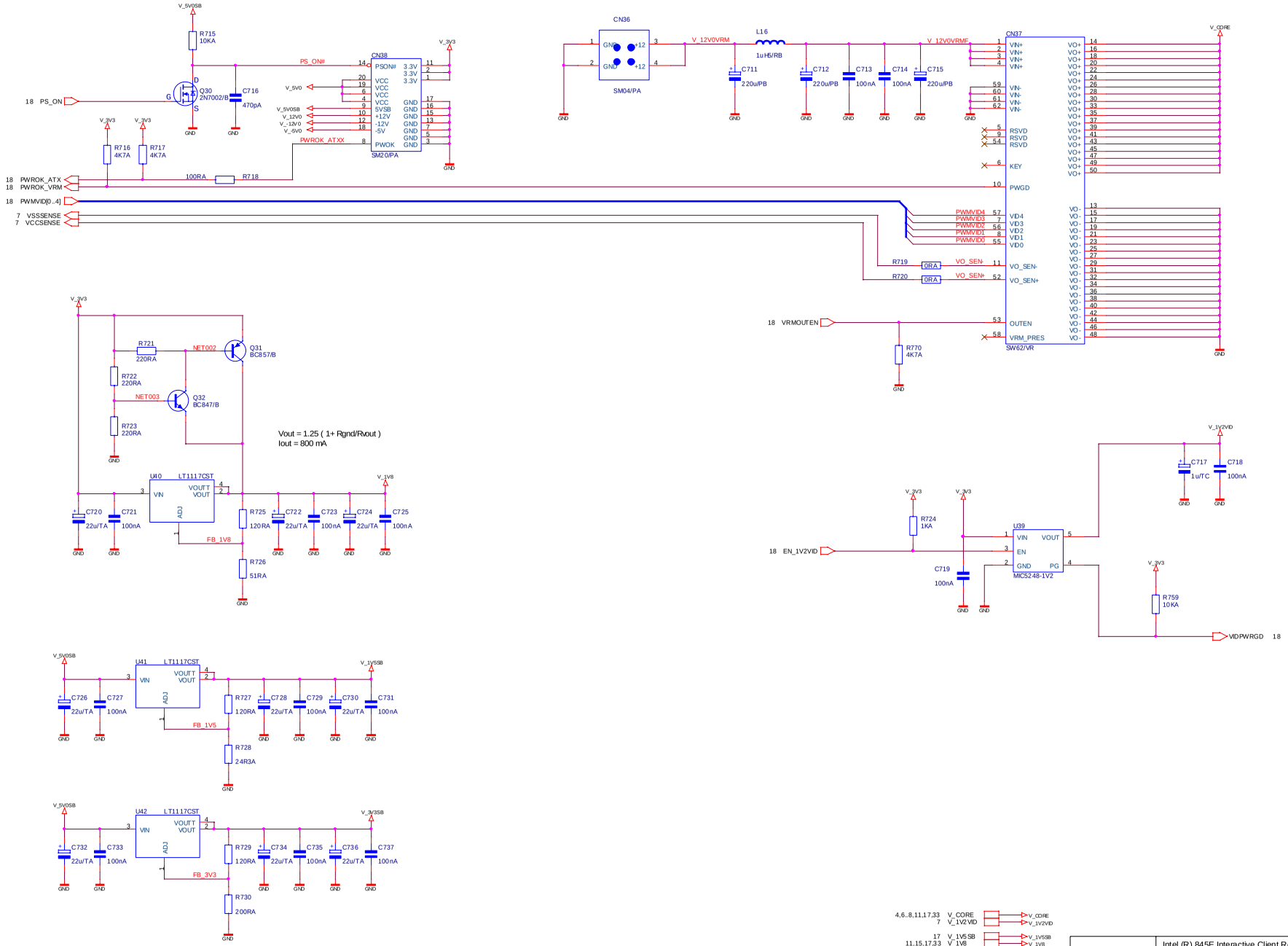
V_5V0SB
R715 10KA
PS_ON#
CN38
PSON#
Q30 2N7002/B
C716 470pA
18 PS_ON
V_3V3
R716 4K7A
R717 4K7A
V_5V0
V_5V0SB
V_12V0
V_-12V0
V_-5V0
PWROK_ATXX
SM20/PA
100RA
R718
18 PWROK_ATX
18 PWROK_VRM
18 PWMVID[0..4]
7 VSSSENSE
7 VCCSENSE
CN36
SM04/PA
V_12V0VRM
L16
1uH5/RB
C711 220u/PB
C712 220u/PB
C713 100nA
C714 100nA
C715 220u/PB
V_12V0VRMF
CN37
SW62/VR
V_CORE
PWMVID4
PWMVID3
PWMVID2
PWMVID1
PWMVID0
R719 0RA
R720 0RA
VO_SEN-
VO_SEN+
18 VRMOUTEN
R770 4K7A
R721 220RA
NET002
Q31 BC857/B
R722 220RA
NET003
Q32 BC847/B
R723 220RA
Vout = 1.25 (1+ Rgnd/Rvout)
Iout = 800 mA
U40 LT1117CST
V_1V8
C720 22u/TA
C721 100nA
R725 120RA
C722 22u/TA
C723 100nA
C724 22u/TA
C725 100nA
FB_1V8
R726 51RA
V_1V2VID
C717 1u/TC
C718 100nA
18 EN_1V2VID
R724 1KA
U39
MIC5248-1V2
C719 100nA
R759 10KA
VIDPWRGD 18
U41 LT1117CST
V_1V5SB
C726 22u/TA
C727 100nA
R727 120RA
C728 22u/TA
C729 100nA
C730 22u/TA
C731 100nA
FB_1V5
R728 24R3A
U42 LT1117CST
V_3V3SB
C732 22u/TA
C733 100nA
R729 120RA
C734 22u/TA
C735 100nA
C736 22u/TA
C737 100nA
FB_3V3
R730 200RA
4,6..8,11,17,33 V_CORE
7 V_1V2VID
17 V_1V5SB
11,15,17,33 V_1V8
6,8,12,15..17,19,20,23,26..29,33 V_3V3
15..20,24,25,29,31..33 V_3V3SB
17,19..21,23,25..27,29..34 V_5V0
17,19,21,22,31..34 V_5V0SB
15,23,27,29,32..34 V_12V0
29,33 V_-12V0
4,7,8,10..34 GND
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