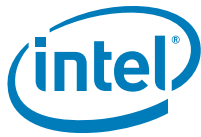


Intel[®] Core[™]2 Duo Processor SL9380 with 800 MHz Front Side Bus on 45 nm Process

Datasheet Addendum

For Platforms based on Intel[®] 3100 Chipset for Embedded Use

September 2008



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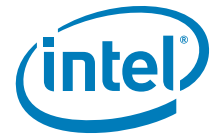
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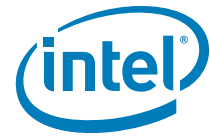
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Revision History

Revision Number	Description	Date
001	Initial Release	September 2008

§



1 Overview

This document is the datasheet addendum for the **Intel® Core™2 Duo Processor SL9380 Low-Voltage (LV) Small Form-Factor (SFF)** for **platforms featuring the Intel® 3100 Chipset**.

Aside from the specific differences (highlighted in **bold** typeface) mentioned in this addendum, the general processor specifications are identical to a mobile Intel® Core™2 Duo processor LV SFF (i.e., SL9400).

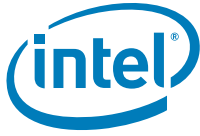
Note:

In this document, the Intel Core 2 Duo mobile processors are referred to as the processor and Intel® 3100 chipset is referred as the IMCH (Integrated Memory and I/O Controller Hub). The following list provides some of the key features of this processor for embedded use:

- **800 MHz Source Synchronous Front Side Bus (FSB)**
- Dual Core with Symmetric Multiprocessing (SMP) support
- On-die, 6-MB L2 cache with Advanced Transfer Cache Architecture
- Supports Intel® architecture with Intel® Wide Dynamic Execution
- Supports L1 Cache to Cache (C2C) transfer
- On-die, primary 32-KB instruction cache and 32-KB write-back data cache in each core
- Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), Supplemental Streaming SIMD Extensions 3 (SSSE3) and Streaming SIMD Extensions 4 (SSE4)
- Advanced power management features including Enhanced Intel SpeedStep® Technology
- Digital Thermal Sensor (DTS)
- Intel® 64 Technology
- 956 ball Micro-FCBGA packaging technologies
- Small Form Factor (SFF) package size of 22mm x 22mm
- Execute Disable Bit support for enhanced security

Note:

Intel® 64 Technology requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel 64 Technology. The processor will not operate (including 32-bit operation) without an Intel 64 Technology-enabled BIOS. Performance will vary depending on your hardware and software configurations. See <http://developer.intel.com/technology/intel64/index.htm> for more information including details on which processors support Intel 64 Technology or consult with your system vendor for more information.



1.1 Processor Unsupported Features

Intel® Core™2 Duo Processor SL9380 **does NOT** support the following features:

- 1066 MHz Front Side Bus (FSB - 800 MHz supported only).
- Dynamic FSB frequency switching (SLFM).
- Low-power processor core C-states: C3E, C4, C4E, C6
- Low-power processor package C-states: Deeper Sleep, Intel® Enhanced Deeper Sleep, Deep Power Down Technology.

1.2 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as <i>address</i> or <i>data</i>), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level). XXXX means that the specification or value is yet to be determined.
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
TDP	Thermal Design Power
V _{CC}	The processor core power supply
V _{SS}	The processor ground



1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Document	Document Number
<i>Intel® Core™ 2 Duo on 45 nm process Datasheet</i>	http://www.intel.com/design/intarch/core2duo/tech_docs.htm
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual</i>	http://www.intel.com/products/processor/manuals/index.htm
<i>Intel® 64 and IA-32 Architectures Software Developer's Manual Documentation Changes</i>	http://developer.intel.com/design/processor/specupdt/252046.htm
<i>Volume 1: Basic Architecture</i>	253665
<i>Volume 2A: Instruction Set Reference, A-M</i>	253666
<i>Volume 2B: Instruction Set Reference, N-Z</i>	253667
<i>Volume 3A: System Programming Guide</i>	253668
<i>Volume 3B: System Programming Guide</i>	253669
<i>Intel® 64 and IA-32 Architectures Optimization Reference Manual</i>	248966

