

Introduction to Via-In-Pad Board Design

Application Note

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Revision 001



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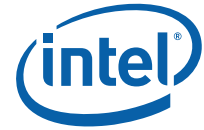
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Revision History

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320970	001	Initial release.	November 2008

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1 Introduction

1.1 Introduction

From Internet. http://www.ami.ac.uk/courses/topics/0262_hdi/index.html#1

"In the 50+ years since printed circuits have become commonplace, the complexity and density of interconnect offered has increased markedly. For example, tracks that were 1mm wide successively became 0.25mm and 150 μ m, and 100 μ m is nowadays achievable in volume, although prudence suggests that such densities are not used for large areas. And holes, which used to be 0.9–1.2mm diameter for through-hole connectors, are now typically 0.35mm or less for vias. In other words, conventional printed circuit technology is still capable of meeting many of today's requirements. Yet there is a grouping of products referred to as "High Density Interconnect" (HDI for short) that are used to create still denser interconnect..."

The above quote refers to a new technology that is becoming more common for board design considerations. An alternative approach to HDI is VIP (Via-In-Pad). This paper will focus on what VIP is and its trade-offs versus other design techniques.

1.2 Terminology

Term	Description
HDI	High Density Interconnect
PTH	Plated Through-hole
VIP	Via-In-Pad

1.3 Reference Documents

Document	Document No./Location
http://www.ami.ac.uk/courses/topics/0262_hdi/index.html#1	

1.4 HDI / VIP overview and definitions:

High-Density Interconnect (HDI) board designs contain blind and/or buried vias often containing very small diameters. Doing this can lead to problems in manufacturability and debug. Some of these issues are described later.

A via is a drilled hole through a PCB board. The via usually connects an item on one layer to an item on another layer. Some typical vias types used in HDI designs are shown in [Figure 1](#):

- Micro via – Via may not go all the way through the board (blind via) or may be buried within the stack-up (buried via)
- Staggered micro via – Via blind or buried within the board in an offset pattern
- Stacked micro via – Vias may exist in either a blind or buried scenario overtop of each other.
- Plated Through-hole vias (PTH) – The vias extend from the bottom to the top of board.

Figure 1. HDI/Micro via types

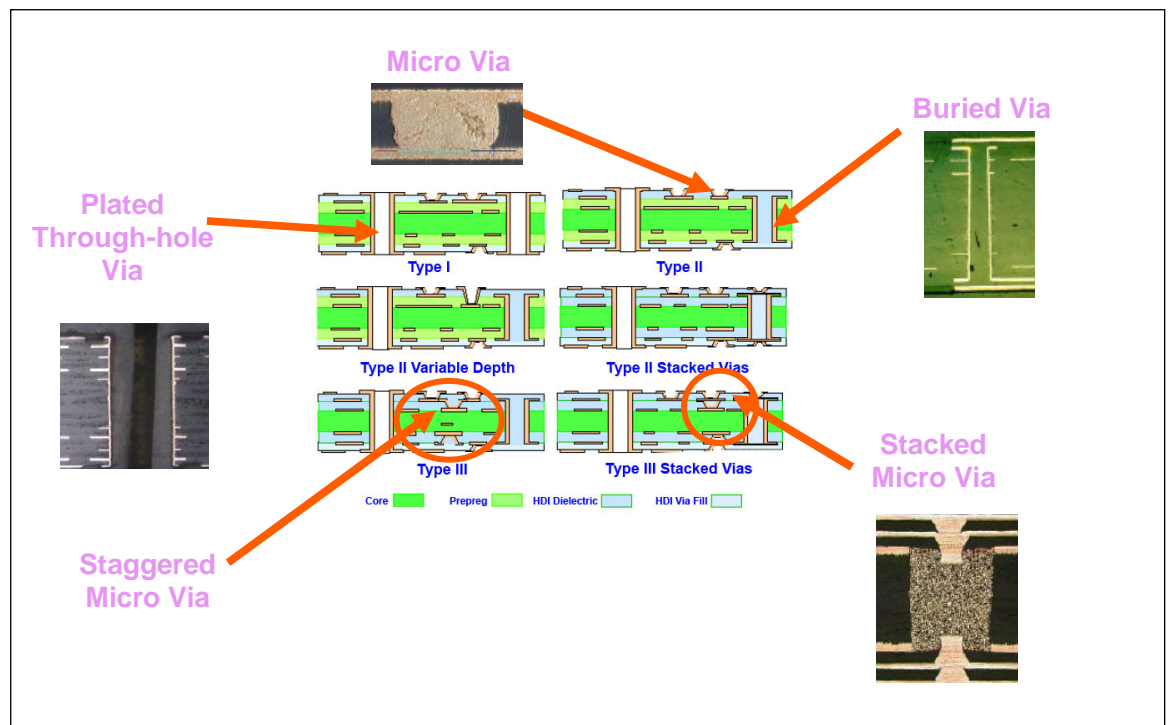




Figure 2 further illustrates the meaning of HDI and by blind/buried vias. Figure 2 shows three possible stack-ups.

The 1-x-1 stack-up configuration contains one build-up layer and one laser drilled layer. This stack-up uses micro vias to connect L1 to L2 and L8 to L7. It also uses a buried via to run between L2 and L7.

The 1-x-1+ stack-up configuration contains one build-up layer and two laser drilled layers. The stack-up uses micro vias to connect L1 to L2, L2 to L3, L7 to L6, and L8 to L7. It uses a buried via to run between L2 and L7.

The 2-x-2 stack-up configuration contains two build-up layers and two laser drilled layers. This stack-up uses micro vias to connect L1 to L2, L2 to L3, L7 to L6, and L8 to L7. It uses a buried via to run between L3 and L6.

Figure 2. Example of HDI stack-up

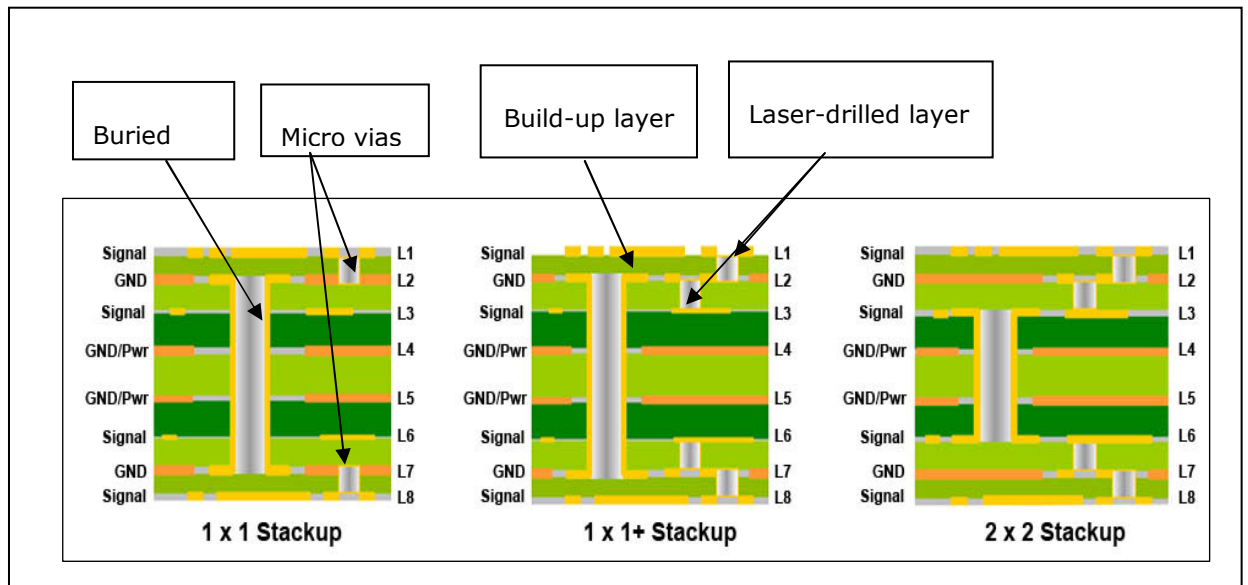
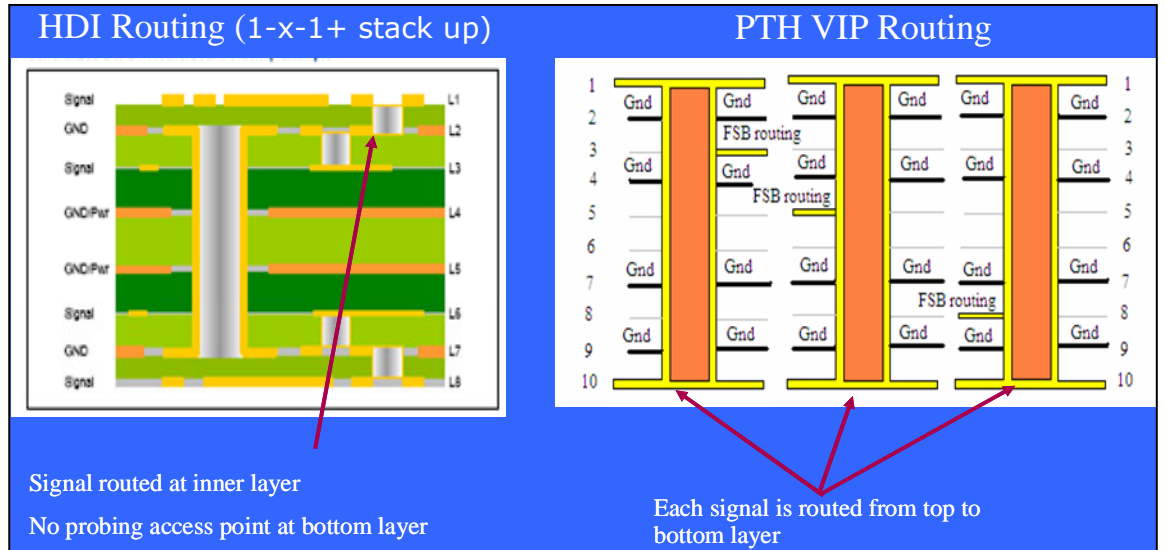


Figure 3 is used to highlight the differences between HDI and VIP. The vias in HDI routing do not extend to the bottom or top later. However in the Plated Through-hole (PTH) VIP routing diagram, the vias extend from the bottom to the top of board. The pad, which is a conductive pattern on printed circuits designated for mounting of attachment of components, is directly over the via, hence the name via-in-pad. Several advantages and disadvantages to this approach are described in later sections.

Figure 3. HDI and VIP board stack-up side-by-side comparison



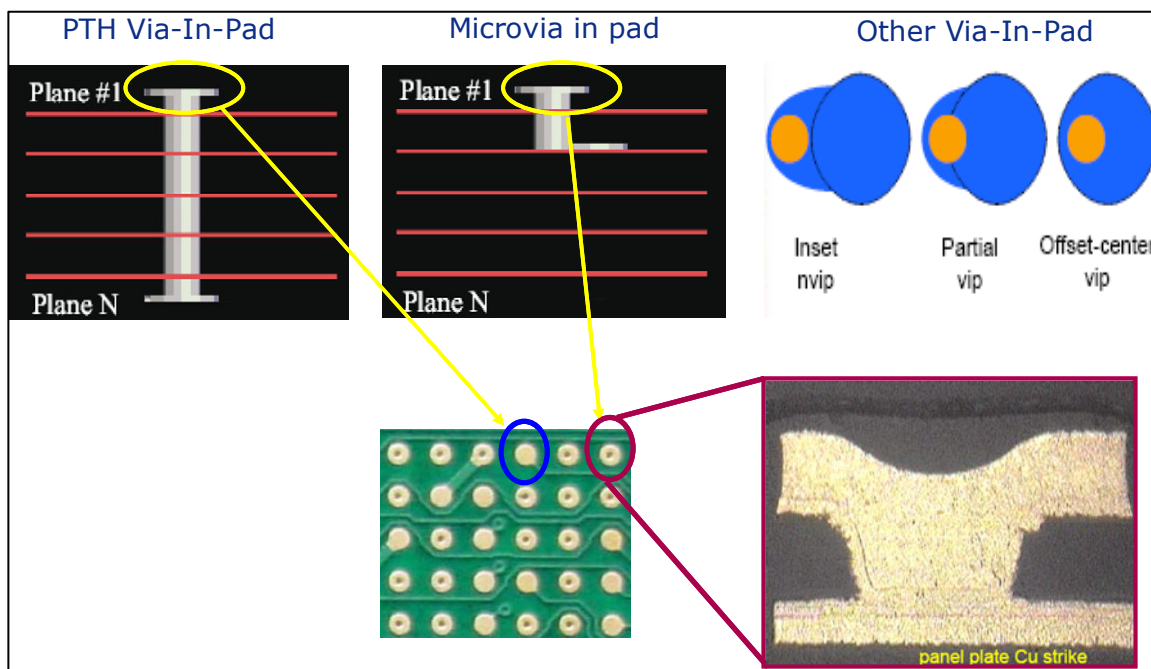
2 Via-In-Pad Type

There are three major groupings of via-in-pads shown in [Figure 4](#):

- 1) PTH
- 2) Micro via-in-pad
- 3) Various other VIP types

The focus on this paper is on Plated Through-hole. Some of the key advantages of PTH are low cost, simple PCB process; commonality to many Fabrication houses (FAB Houses); and relatively high Fabrication (FAB) yield.

Figure 4. Types of Via-In-Pads

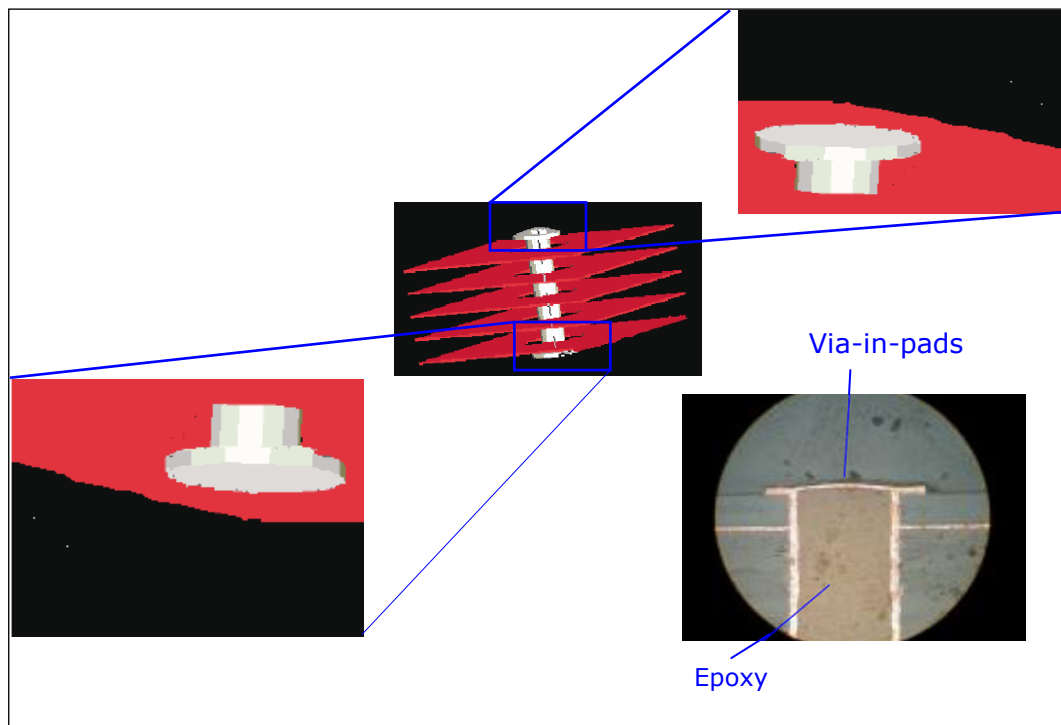


3 Via-In-Pad (VIP) Structure

By definition, the structure of a PTH VIP is a copper clad substrate that is drilled and plated with copper from top to bottom of the board (see [Figure 5](#)). To construct a PTH VIP, a hole is drilled through the pad and then filled with epoxy. Once the epoxy is cured, excess epoxy is removed, and the via is plated with copper on both the top and the bottom.

The lower right corner of [Figure 5](#) shows a magnified X-Ray image of a PTH VIP.

Figure 5. Structure of Plated Through-hole Via-In-Pad

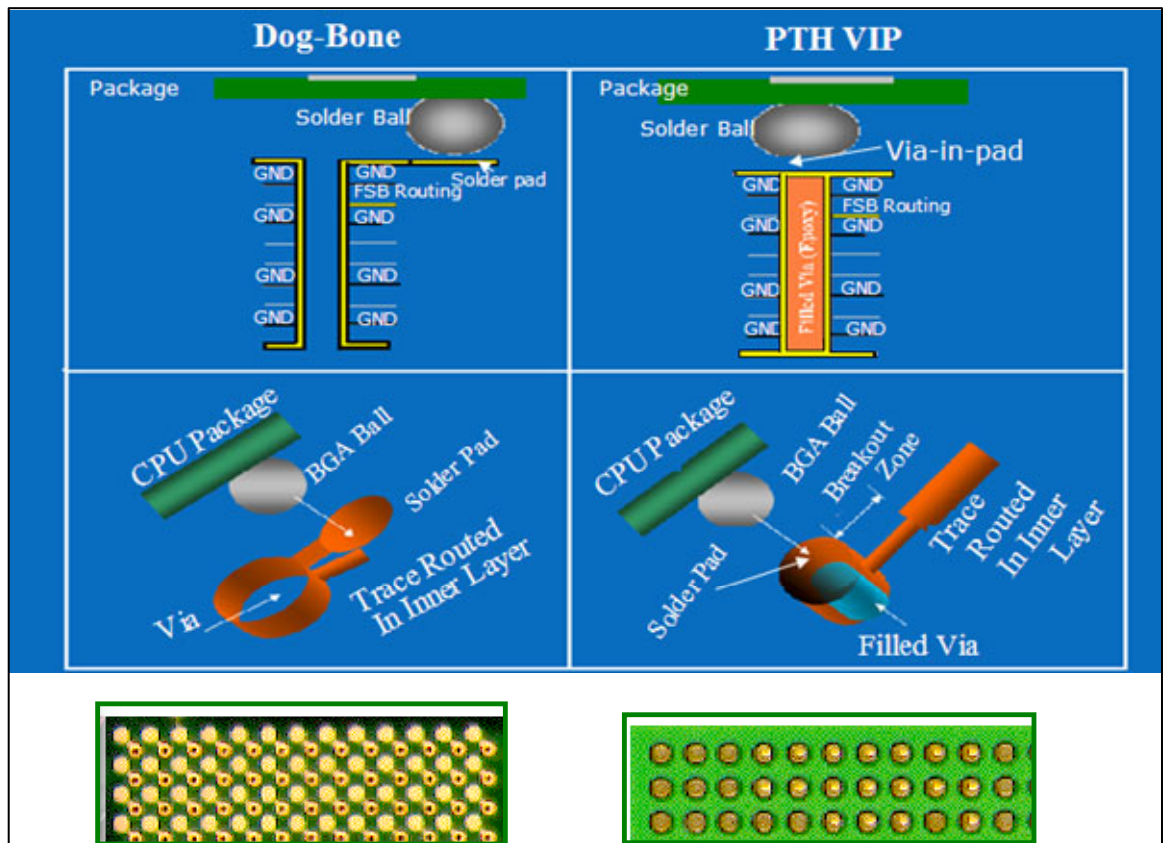




4 Dog-bone vs. VIP Routing

Figure 6 illustrates the difference between a standard board design (dog-bone technique) and VIP. In the dog-bone diagram on left, the pad is separate from the via through a routed trace. In a PTH VIP design as seen on diagram on right, the solder pad is directly over the via. The pad being separate from the vias in the dog-bone scenario allows flexibility in component and routing placement on the inner layers but routing area is compromised on the pad mounting layer.

Figure 6. Dog-bone versus VIP routing



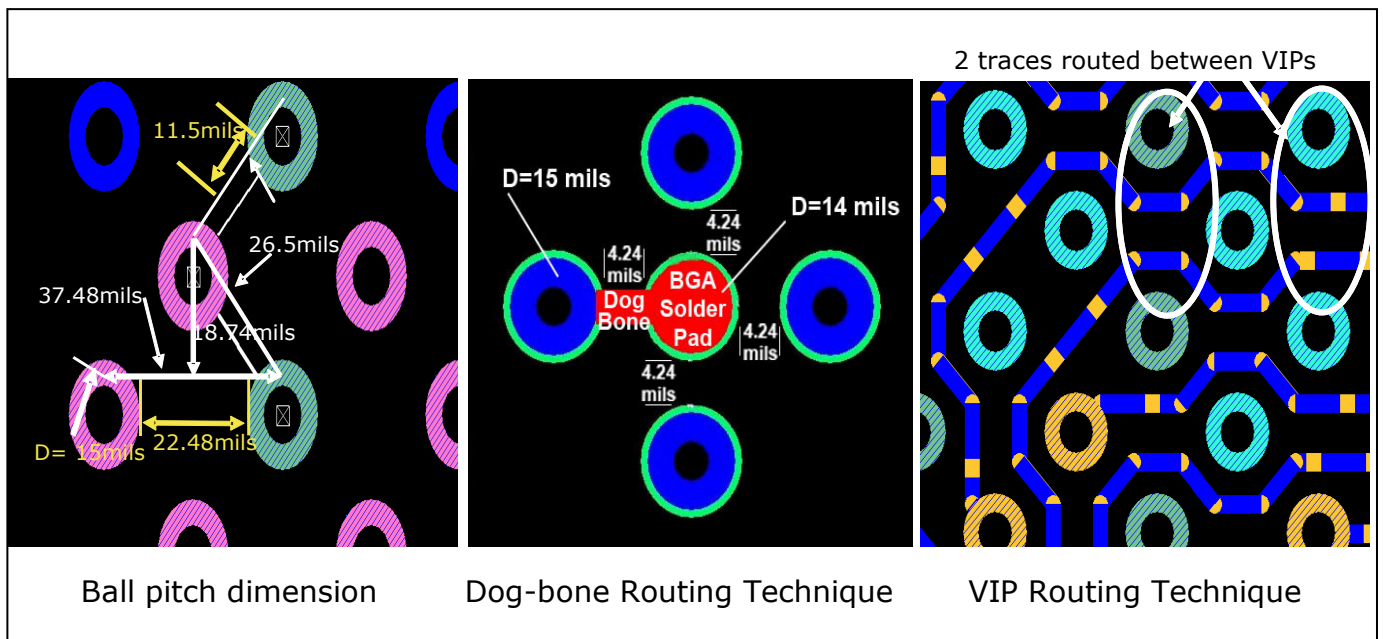
5 Advantages Using Via-In-Pad

5.1 High Pin Count Devices

As can be seen in [Figure 7](#), VIP techniques allows board designer to utilize the extra space given by the combination of the PAD and the via for top layer escapes. VIP gives no less escape real-estate on the internal layers.

The same scenario holds true versus HDI on the top layers but HDI provides considerably more routing space on the internal layers at a minimum cost of visibility for debug.

Figure 7. VIP provides more routing space for high pin count devices





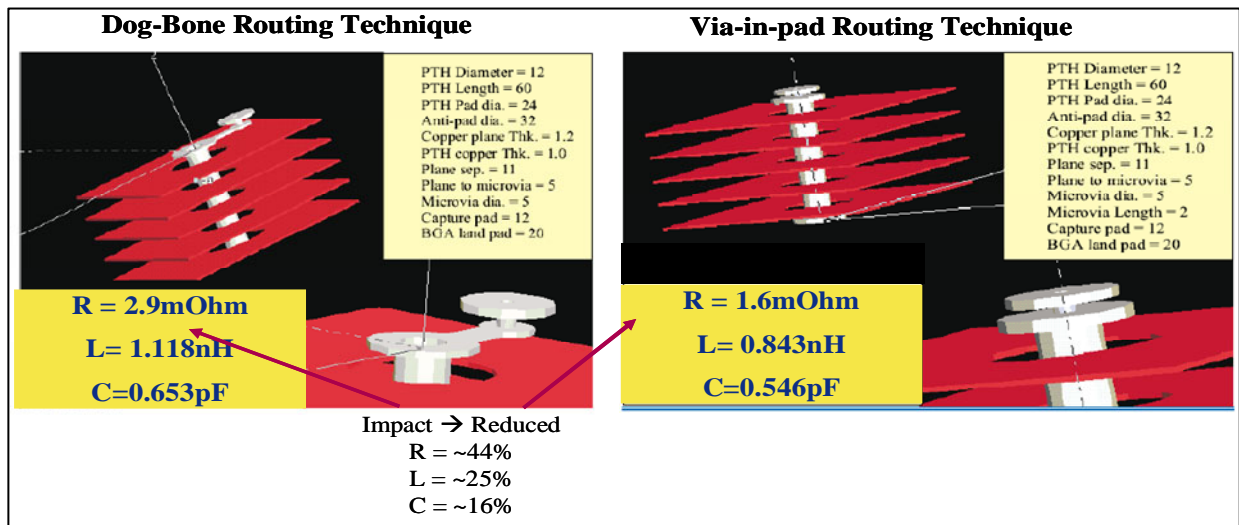
5.2 Reduce Pad Resistance, Inductance, and Capacitance

Figure 8 is an illustration of the same stack-up utilizing the Dog-Bone and the VIP technique. As a percentage, the RLC characteristics of the VIP are significantly better:

- Resistance 44% improved
- Inductance 25% improved
- Capacitance 16% improved.

These improvements may aid in the overall performance of the circuit by reducing external factors induced through board material variance.

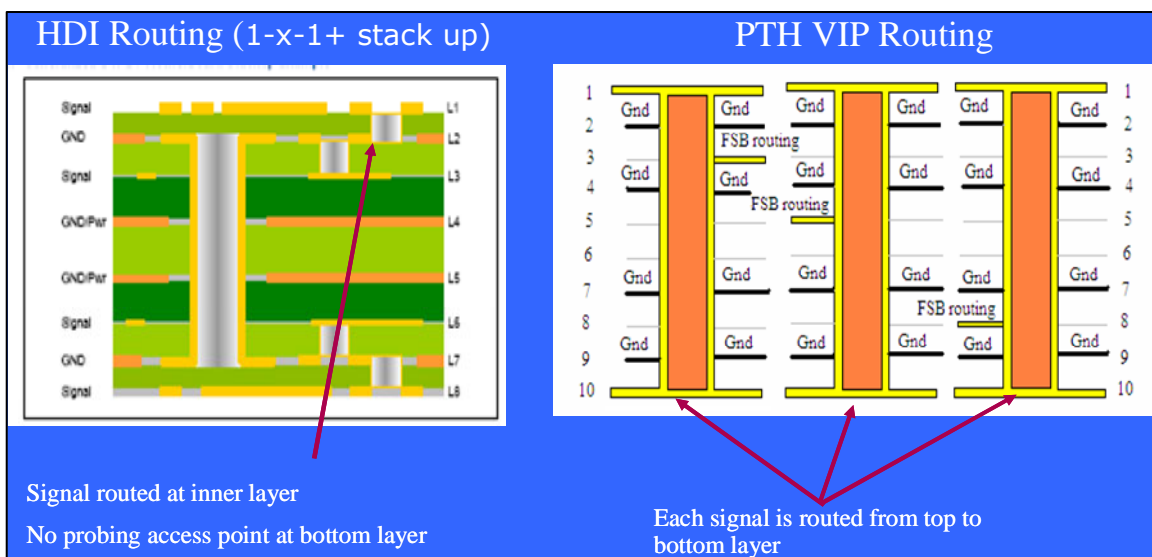
Figure 8. Eliminating Dog-Bone trace results in reduced RLC characteristics



5.3 Accessibility for Validation Probing

Figure 9 illustrates a HDI stack-up example on the left and a PTH VIP stack-up on the right. The lack of probe accessibility on the HDI is easily seen on the HDI diagram on the left. This key disadvantage can make board debug difficult. Manufacturing defects are not easily identified in the HDI stack-up. Implementing a work-around for engineering units becomes limited in the HDI stack-up. This is a key advantage of VIP over HDI.

Figure 9. PTH Via allow Non-Mount layer probing for each signal



5.4 More Fab Houses of Choice

At the time of this paper’s initial release, HDI is less prevalent technology within FAB Houses and VIP is commonly used. This fact does not guarantee that VIP will remain as the more dominate technique. HDI may and will likely become at least as common as the technology proliferates.

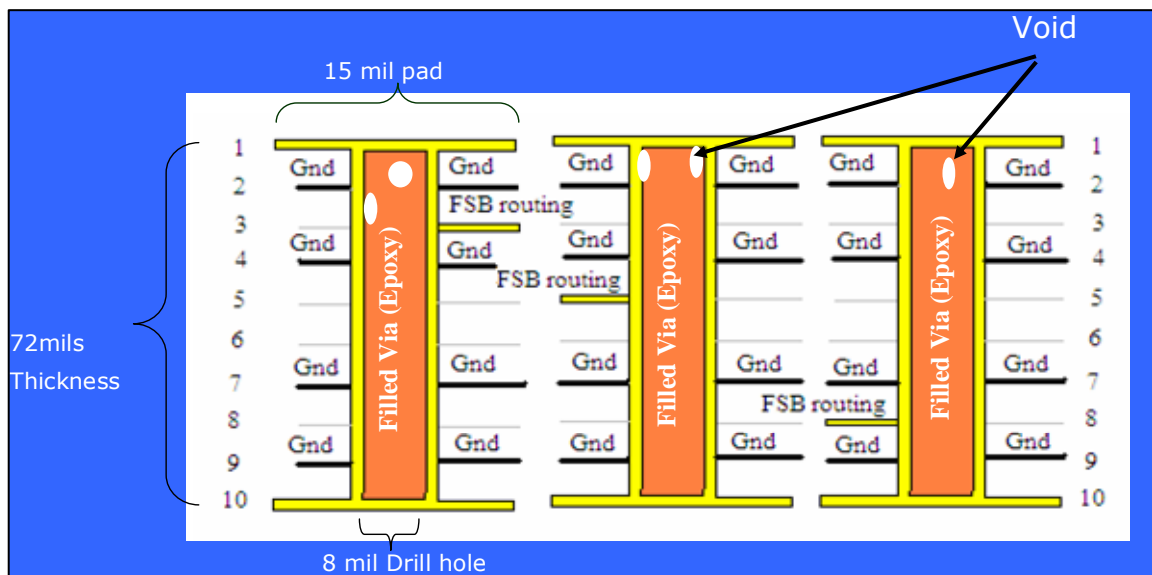


6 Challenges with Via-In-Pad

6.1 Void Concern

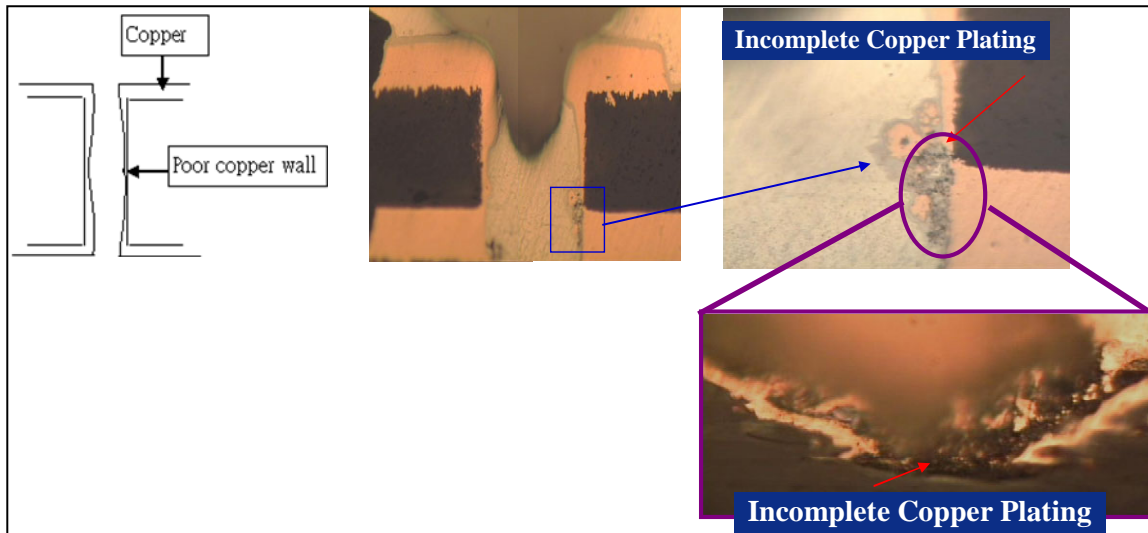
Void concerns in the epoxy are one of the key challenges using VIP. Larger board thickness increases risk of voids in the epoxy (see [Figure 10](#)). Voids can create expansion and/or contraction with temperature variation. The expansion/contraction creates stressing on the via walls which can cause connection issues.

Figure 10. Epoxy-filled Vias with voids



The void concerns also force a concern with wall thickness due to plating copper in the via. The chemical becomes more difficult to flow with board thickness increase and via diameter decrease. This forces thinning of the copper in the PTH, see, [Figure 11](#). The thinning copper wall along with the expansion/contraction due to void concerns creates potential blow out of the via wall. The general rule of thumb is that higher than 6:1 aspect ratio, board thickness to via diameter creates a potential issue. Please consult the particular FAB house chosen on this concern.

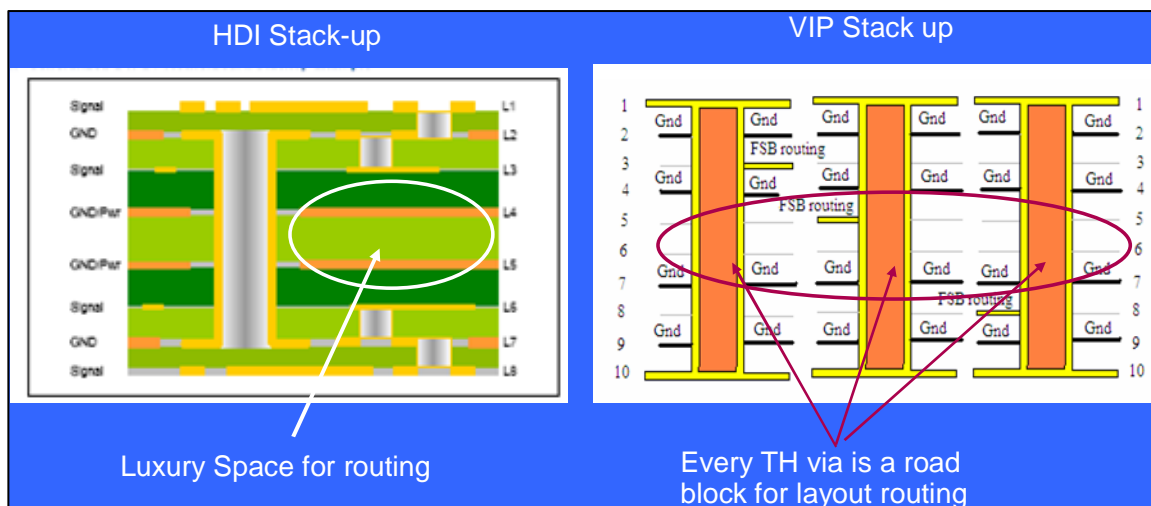
Figure 11. Aspect ratio concerns



6.2 Limited Routing Space for Inner Layer

Figure 12 illustrates how HDI makes more efficient use of the inner layers versus VIP. The blind and buried vias keep clear routing lanes on the inner layers opening them up physically for routing. There may be other concerns such as signal integrity, cross talk, etc. which may prevent this from being usable space. The inner layer routing of VIP routing is generally equivalent when comparing to the dog-bone technique.

Figure 12. VIP limited internal routing versus HDI

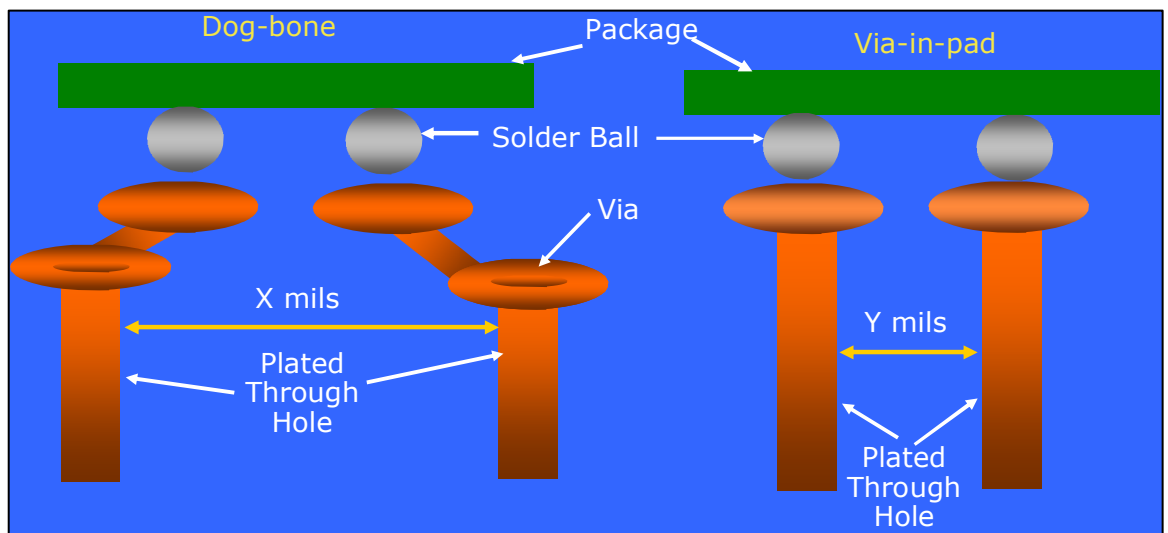




6.3 Fixed Gap between Vias

Figure 13 displays a disadvantage when using VIP versus dog-bone technique. The diagram on the left illustrates how the small trace enables movement of the via versus the ball pitch on the package. The diagram on the right shows how VIP must follow the pitch of the part. This restriction increases the risk of the inability to place bottom side capacitance or cause shorting when bottom side capacitance is placed.

Figure 13. Dog-Bone versus VIP route spacing



6.4 Fine ball pitch versus Trace width considerations

Be careful on board layout with fine pitch. Designing your board to meet maximum specified values of pitch, diameter, and trace thickness, could leave you with minimal trace width and spacing. This trace width and spacing limitation could force violation of proper design rules. Ensure that proper design rules/techniques may be met when using VIP.



7 ***Summary***

Plated Through-hole Via-In-Pad board design is a proven technique that drives for-cost competitive board development, improved signal quality, robust yield, and equivalent PCB/Packaging reliability. It is an alternative technique to consider when starting a new board design. Please consult the chosen FAB House for more explicit details on the differences between the multiple techniques.