



The Intel® IOP321 I/O Processor

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Intel® XScale™ core processor and tightly integrated I/O peripherals in a single chip

Overview

The continued growth of complex networking and storage applications demands a combination of I/O processing performance, high data throughput, programmability, tight integration and cost effectiveness. The Intel® IOP321 I/O processor was created to fill these needs as a highly integrated system on a chip with the performance and I/O bandwidth required to serve a wide range of these applications. The IOP321 was specifically designed with features to support networking, storage, and embedded applications, including networking control plane devices, Voice over IP blades, network security appliances, Host Bus Adapters, print imaging devices, industrial control systems, RAID storage applications, networked storage devices, and network gateways.

The architecture of the Intel IOP321 I/O Processor (IOP321) is designed for a combination of high-performance I/O application processing and extremely high data throughput. It is the first Intel I/O Processor to combine both the Intel® XScale™ technology as well as the high-performance PCI-X parallel bus interface. The device employs a high-throughput 200 MHz internal bus architecture to connect its high-performance memory controller unit, integrated hardware-based Application Accelerator Unit and other peripherals to the processor core. With these high I/O throughput features, the IOP321 delivers a maximum I/O rate that is over 100% greater than previous Intel I/O processor chipsets.

Highlights of the IOP321 include:

- **Performance** - as a single-chip I/O processing solution, the IOP321 implements tight integration of the Intel XScale core at up to 600 MHz with peripherals designed to maximize data throughput. The chip also features a 200 MHz internal bus and a 200 MHz DDR SDRAM interface with support for up to 1 GByte of memory.
- **PCI-X** - the IOP321 is the first Intel I/O processor with a single high-bandwidth 64-bit, 133 MHz PCI-X bus, providing connections to the fastest parallel PCI-X bus architecture systems.
- **Flexibility** - the peripheral bus provides an interface to external components that do not interface directly to the PCI bus, including flash memory and optional ASICs, DSPs or legacy devices to meet application needs.
- **Cost-effectiveness/flexibility** - the IOP321 is an affordable solution for price-sensitive embedded, storage, and networking applications.
- **Compact package size** - 544L PBGA has small dimensions (35mm x 35mm) to conserve board real-estate.
- **Code-compatibility** - The IOP321 is code compatible with the Intel® IOP310 I/O processor chipset, Intel® StrongARM* SA-110 and is supported by extensive Intel XScale technology tools support.



- **Low power consumption** - the combination of the low-power Intel XScale core and the implementation of a power optimized, highly integrated peripheral set delivers low power consumption and avoids the need for a heat sink.
- **Compatibility** - As with all Intel I/O processors, the IOP321 is a fully validated I/O solution designed to work with Intel® Architecture processors, chipsets, and server products.
- **Manufacturing technology** – The IOP321 is designed and manufactured using Intel's state of the art 0.18-micron process technology.

When compared to Intel's previous single-chip Intel® IOP303 I/O processor, the IOP321 delivers about three times greater performance, twice the I/O throughput via PCI-X, a 40 percent reduction in package size, and a 40 percent reduction in power consumption.

The ability of the IOP321 to handle processor-intensive data-handling tasks involved in RAID and other I/O processing enables the chip to optimize system-level performance in a variety of networked storage applications.

Applications

The IOP321 was specifically designed with features to support networking, storage, and embedded applications. These applications include networking control plane devices, Voice over IP blades, network security appliances, Host Bus Adapters, print imaging devices, industrial control systems, RAID storage applications, networked storage devices, and network gateways.

The commonality between these applications is their need for high I/O throughput, memory performance and processing power. Features on the IOP321 also support connection to a wide variety of communications interfaces, which are important in the design of these types of applications. In addition, the ability of the IOP321 to offload processor-intensive data-handling tasks, involved in RAID and other I/O processing functions, enables the chip to optimize overall system-level performance when used as a co-processing solution in networking and storage applications.

High-performance Processor with Integrated Peripherals

The Intel IOP321 I/O processor is based on the Intel XScale core processor and is available in both 400 and 600 MHz versions. The Intel XScale microarchitecture features Intel® Super-Pipelined RISC Technology, a 7-stage integer, 8-stage memory super-pipelined core that achieves high speed with ultra-low power consumption. Capabilities include up to 720 Dhrystone 2.1 MIPS and core power consumption of less than 800 mW at 600 MHz, and typical power consumption including I/O of about 3.5W at 600 MHz.

The Intel XScale core features 32 Kbyte data and instruction caches, and a 2 Kbyte mini-data cache. The combination of speed and larger caches allows users to use complex applications involving processor-intensive calculations. The 2 Kbyte mini data cache enhances data streaming by avoiding impacts to the data cache caused by frequently changing data streams. For enhanced



data throughput in core-intensive applications, the processor implements a 200 MHz, 64-bit internal bus capable of moving data at 1.6 Gbyte/s. Performance additions include write-back caching, an integrated write buffer, cache locking, and the ability to continue an instruction while the data cache is retrieving data.

Other integrated features include:

- Branch Target Buffer capable of storing 128 entries of next-instruction predictions
- Multiply-Accumulate unit (MAC) for performing multiply/accumulate operations caching, enables policy for data-write allocation and manages the write buffer to coalesce stores to external memory
- Memory Management Unit (MMU) identifies code as cacheable or non-cacheable, selects the mini data cache, manages write-back or write-through data caching, enables policy for data-write allocation and manages the write buffer to coalesce stores to external memory

For ease of development, the Intel IOP321 I/O processor preserves code-compatibility with the Intel StrongARM SA-110 processor and the Intel IOP310 I/O processor chipset. It is also compliant with ARM* v.5TE instruction set architecture, including ARM V5 instructions without floating point instructions, ARM Thumb* instructions V5T, and ARM* V5E DSP extensions. The instruction set executes either a 32-bit ARM instruction set or the 16-bit Thumb instruction that can be used to maximize code density. As the Intel IOP321 is Intel XScale microarchitecture compatible, it will be code compatible with future I/O processors, thereby preserving investment in code development.

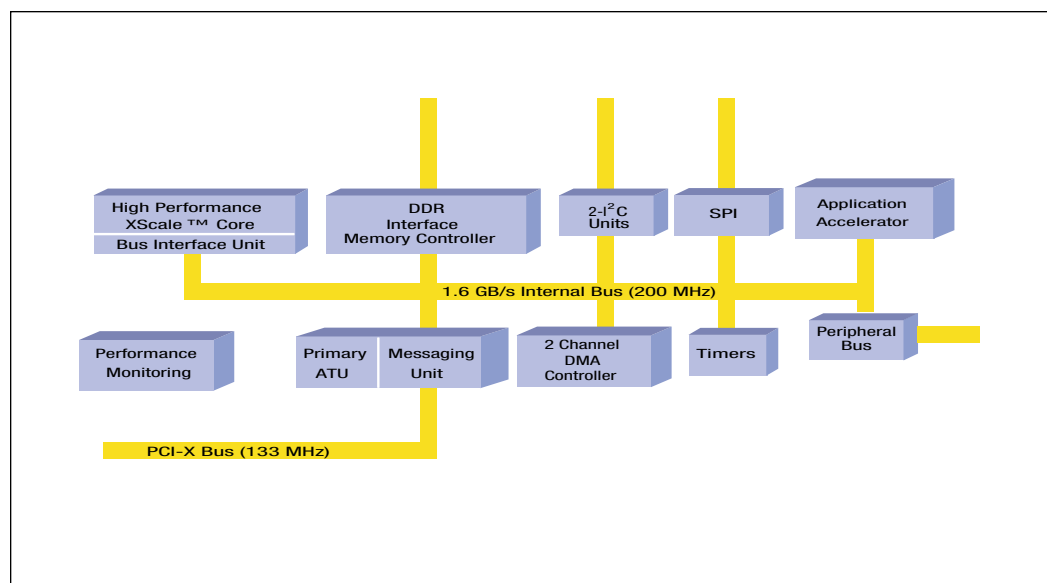
In addition to its high-speed core, the IOP321 implements a broad array of features designed to significantly enhance performance and throughput. To provide maximum implementation flexibility, the processor implements a single PCI-X (PCI-X 1.0A) interface which can operate at 133, 100 and 66 MHz, or PCI 2.2 interface at 66 or 33 MHz (3.3v). For optimum performance the processor also includes support for PC200 Double Data Rate (DDR) SDRAM with Error Correction (ECC) and is capable of supporting 1 Gigabyte of 64-bit memory. It also supports 32-bit mode memory.

DMA Channels

Two independent Direct Memory Access (DMA) channels provide support for automatic data chaining and high-throughput data transfers from PCI-to-memory or memory-to-memory. Each DMA features two 1 Kbyte queues, 4 Gbyte addressing on the internal bus and support 1 Gbyte/s burst support for PCI-X transfers and 1.6 Gbyte/s burst support for transfers to the internal bus.

Memory Controller Unit

The Memory Controller provides an interface between the I/O processor and local memory. The IOP321 supports 64-bit memory capacity of PC200 DDR SDRAM from 64 Mbytes to 1 Gbyte organized in two DIMM banks or 32 Mbytes to 512 Mbytes of 32-bit DDR PC200 SDRAM down on board for reduced cost. The memory controller supports selectable ECC for single-bit and multi-bit error detection. It also features a 1024-byte posted memory write queue supporting 40 and 72 bit-wide memory.



Intel® IOP321 I/O Processor Block Diagram

Application Accelerator Unit

Especially useful for RAID parity processing in storage applications, the Application Accelerator Unit (AAU) transfers read and write data to the memory controller in addition to performing data parity computation across local memory blocks, performing block fills and optional XOR computations on reads. Features include a programmable 512 byte to 1 Kbyte store queue, hardware support for unaligned data transfers to the internal bus and automatic data chaining.

Address Translation Unit

The Address Translation Unit (ATU) enables PCI masters on the PCI bus to initiate transactions on the I/O processor's internal bus, and also enables the Intel XScale core to initiate transactions on the PCI bus. The ATU provides 64-bit address windowing for outbound translation and 64-bit address windowing for inbound translation with four sets of base, limit and translation registers.

Peripheral Bus

The peripheral bus provides an interface to external components that do not interface to the PCI bus, including flash memory and optional ASICs, DSPs or legacy devices. The peripheral bus is programmable to 8, 16 or 32 bits and features six chip-enables to support speeds of 33 MHz, 66 MHz and 100 MHz. The peripheral bus provides a glueless interface for 8 and 16-bit flash memory.



Interrupt Controller

The Interrupt Controller handles interrupts from internal sources including: DMA channels, the ATU, the Performance Monitoring Unit, timers, the I2C bus, Application Accelerator Unit, Messaging Unit, Memory Controller Unit, serial port, and software exceptions. The controller also handles external interrupts from five external pins, including one high-priority interrupt and four maskable inputs.

Performance Monitor Unit

The Performance Monitor Unit measures and monitors system parameters that determine overall I/O processor performance. Peripheral performance monitoring includes: one 32-bit dedicated Global Time Stamp counter, three control/status registers and 14 programmable event counters. The Performance Monitor Unit can be used to increase the performance of an application running on the Intel IOP321.

Additional integrated features implemented in the Intel IOP321 to reduce chip count and simplify design include eight GPIO pins and six SDRAM output clocks.

Software Support and Development Tools

The Intel® IQ80321 development kit is a complete board solution for rapid intelligent I/O software development. The kit features Macraigor Systems Raven* JTAG support, Accelerated Technology, Inc. CodeLab* Development Tools and includes evaluation copies of the Wind River VxWorks* RTOS and Tornado* development environment, Accelerated Technology, Inc. Nucleus* RTOS, Red Hat eCos* RTOS evaluation copy and Lynuxworks BlueCat* Linux RTOS.

In addition, the kit provides Intel XScale core-tools including Red Hat GNUPro* Tools, ARM Developer Suite* and Wind River Tornado* Tools in addition to debug-monitor images including Red Hat Red Boot* and ARM Angel*. The kit is complete with comprehensive documentation.

Summary

The IOP321 is Intel's fifth generation I/O processor. It combines the high performance of the Intel XScale core processor with a compelling set of integrated peripherals. It delivers a decisive combination of performance, flexibility, PCI-X data throughput, small package size, reduced power dissipation and cost effectiveness. With an integrated data flow architecture that includes a 200 MHz internal data bus, support for up to a gigabyte of DDR SDRAM, integrated hardware acceleration and tightly integrated peripherals on a single chip, the IOP321 is an advanced system-on-a-chip for building powerful high I/O applications. The Intel IOP321 I/O Processor is a superior choice for powering networking, storage and embedded applications that require the highest I/O and processing performance.

For more information, visit the Intel Web site at: developer.intel.com

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