



Intel[®] 80321 I/O Processor PCI-X Clock Speed Initialization

White Paper

February 2002



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Revision History

Date	Revision	Description
February 2002	001	Initial Release.



1.0 White Paper Purpose and Description

The Intel® 80321 I/O processor (80321), based on Intel® XScale™ microarchitecture (ARM* architecture compliant), provides enhanced data transfer performance through the use of the PCI-X bus. The *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a* specifies a new power-up initialization pattern to indicate PCI-X versus PCI mode and the speed of the PCI-X bus:

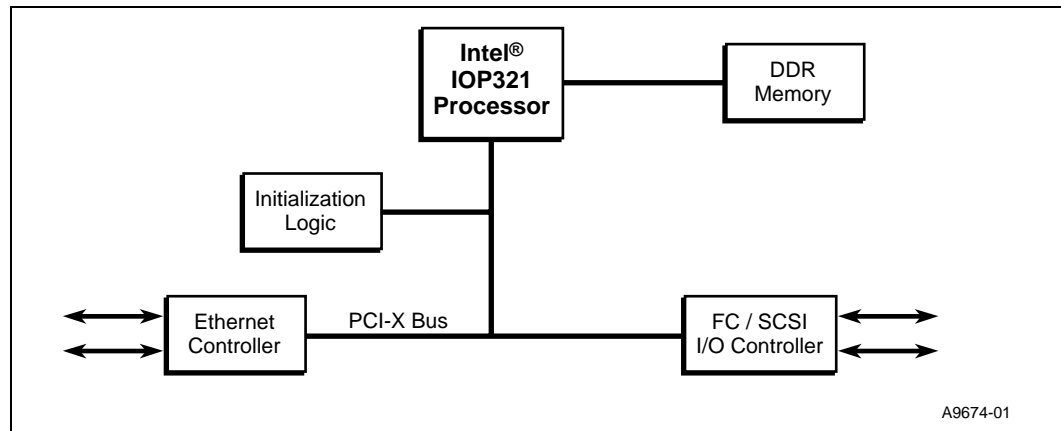
- 66MHz.
- 100MHz
- 133MHz

This pattern is explained in the *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a*, section 6.2. The pattern is defined by the combination of FRAME#, IRDY#, DEVSEL#, STOP# and TRDY# signals at the rising edge of RST#.

Typically this pattern is initiated by the source bridge. This document is targeted at the customers using the 80321 without a PCI-X bridge in a standalone embedded design (non-add-in card). An example of this is a Network Attached Storage (NAS) application as shown in [Figure 1](#). In order to properly initialize the PCI-X bus, the extra initialization logic must be added as shown in [Figure 1](#), as the Initialization Logic block.

Note: The example design described in the paper has not yet been validated with actual hardware.

Figure 1. NAS Application Using the Initialization Logic Block



1.1 Document Highlights

This paper is organized as follows:

- [Chapter 1.0, “White Paper Purpose and Description”](#), consists of a introduction and listing of related documents and web links.
- [Chapter 2.0, “PCI-X Initialization Pattern”](#), provides an explanation of the PCI-X initialization.
- [Chapter 3.0, “PCI-X Initialization Design Example”](#), provides an example of a simple circuit implementation.
- [Chapter 5.0, “References”](#), additional background references.

1.2 Related Documents

- *Intel® 80321 I/O Processor Developer’s Manual (273520)*
- *Intel® 80321 I/O Processor Datasheet (275318)*
- *IDT Quickswitch IDTQ3126 Datasheet: http://www.idt.com/docs/CBTLV3126_DS_85424.pdf*
- *Lattice GAL16V8 Datasheet: http://www.latticesemi.com/lit/docs/datasheets/pal_gal/16lv8.pdf*
- *PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a: www.pcisig.com*

2.0 PCI-X Initialization Pattern

2.1 Initialization Requirements

The information in this section is available through the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. Each PCI-X device decodes the initialization pattern consisting of the signals FRAME#, IRDY#, DEVSEL#, STOP# and TRDY#, on the rising edge of reset, to determine whether to enter PCI-X mode or default to conventional PCI mode. This pattern is initiated by the source bridge. In the absence of the source bridge external circuitry is required to create the expected PCI-X initialization pattern to force the 80321 into PCI-X mode.

2.1.1 PCI/PCI-X Clocking Modes

The 80321 clocking modes for PCI-X and PCI bus are shown in Table 1. At the PCI bus reset, the 880321 samples the P_FRAME#, P_IRDY#, P_TRDY#, P_STOP#, and P_DEVSEL#, to determine the operating frequency for PCI-X mode. When P_FRAME# is deasserted and P_IRDY# is deasserted (i.e., the bus is idle) and one or more of P_DEVSEL#, P_STOP#, and P_TRDY# are asserted at the rising edge of P_RST#, the device enters PCI-X mode (see Table 1). Otherwise the device enters conventional PCI mode. With conventional PCI mode, a low on P_M66EN determines that the PCI bus is at 66MHz. The Table 1 lists the expected signals which need to be asserted in order to indicate to the device which PCI-X mode is desired.

Table 1. PCI-X Clocking Modes and Initialization

Mode	PCIXCAP	P_M66EN	P_DEVSEL#	P_STOP#	P_TRDY#
PCI 33 MHz	GND	Deasserted	Deasserted	Deasserted	Deasserted
PCI 66 MHz	GND	Asserted	Deasserted	Deasserted	Deasserted
PCI-X 66 MHz	10KΩ 0.01 μF cap to GND	N/A	Deasserted	Deasserted	Asserted
PCI-X 100 MHz	0.01 μF cap to GND	N/A	Deasserted	Asserted	Deasserted
PCI-X 133 MHz	0.01 μF cap to GND	N/A	Deasserted	Asserted	Asserted

Note: PCI-X cap is used to indicate to the host bridge that an add-in card is PCI-X capable and its frequency. Due to the fact that this White Paper addresses a non-add-in card application PCI-X cap details are not discussed.

Table 2 details the range of frequencies allowed in each of the PCI-X modes:

- PCI-X designs with a nominal clock frequency of 66 MHz have a range of 50-66 MHz.
- PCI-X designs with a nominal clock frequency of 100 MHz have a range of 66 MHz to 100 MHz.
- PCI-X designs with a nominal clock frequency of 133 MHz have a range of 100 MHz to 133 MHz.

Table 2. PCI-X Clocking Frequency

Mode	Minimum Frequency (MHz)	Maximum Frequency (MHz)
PCI 33MHz	0	33
PCI 66MHz	33	66
PCI-X 66MHz	50	66
PCI-X 100MHz	66	100
PCI-X 133MHz	100	133

2.2 PCI-X Reset Mode

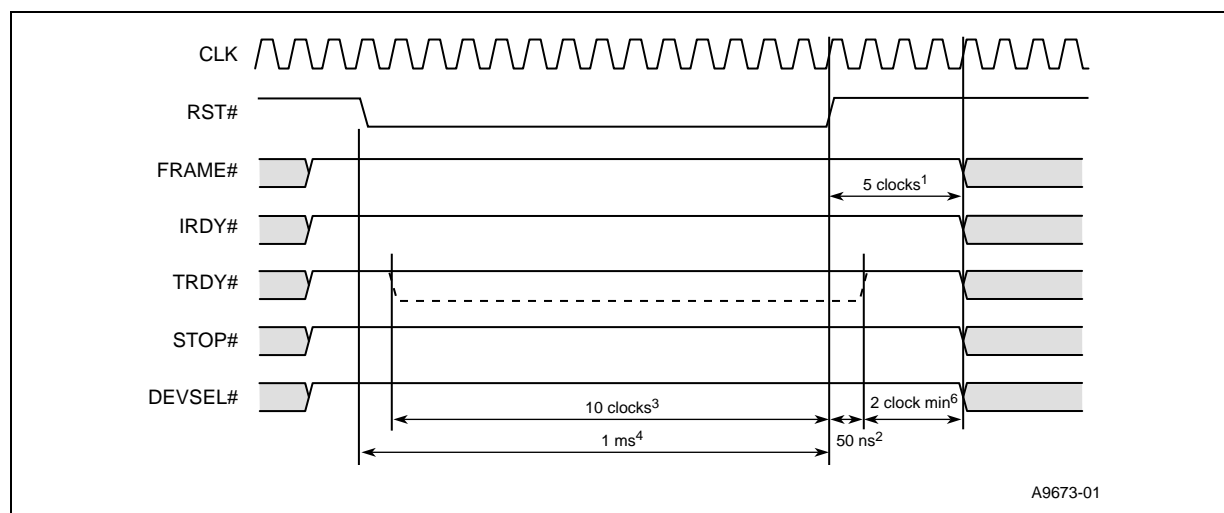
With RST# asserted the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a, allows a change in frequencies. This means that state machines and PLLs are reset.

Note: PCI clock is not required to be stable during the RST# low period.

2.3 Reset Timing

The RST# timing is different in PCI-X to allow for the PCI-X initialization pattern. These values are shown in Figure 2. The P_CLK is shown continuous during the RST#.

Figure 2. RST# Timing for PCI-X



Timing Requirement Notes:

1. Five clock minimum delay from RST# high to the first FRAME# assertion.
2. 50 ns PCI-X initialization pattern maximum hold time after RST# high.
3. Ten clock minimum PCI-X initialization pattern setup time before RST# high.
4. 1 ms minimum RST# active time.
5. 100 μ s minimum RST# active time after CLK is stable.
6. Two clock minimum between the PCI-X initialization being deasserted and the first FRAME# active.

3.0 PCI-X Initialization Design Example

The external circuit design shown in [Figure 3](#) provides the control necessary to allow the selection of the PCI-X clock speeds through two user selectable external switches. Instead of external switches, these signals can easily be dynamically selected using logic control, following the values specified in [Table 3](#).

3.1 PCI-X Speed Selection

To change the speed while the application board is running requires asserting reset:

- Speed selection:
 - 66 MHz PCI-X mode, S1 is open and S2 is open.
 - 100 MHz PCI-X mode, S1 is closed and S2 is open.
 - 133 MHz PCI-X mode, S1 is open and S2 is closed.

The selection must be set by using the below sequence:

1. Assert reset P_RST#
2. Assert SEL0 and SEL1 signals to control the frequency as shown in [Table 3](#).

Table 3. PCI-X Frequency Selection

Frequency (MHz)	PCIX_SEL1	PCIX_SEL0
66	0	0
100	0	1
133	1	0
undefined	1	1

3.2 PCI-X Initialization Timing Requirements

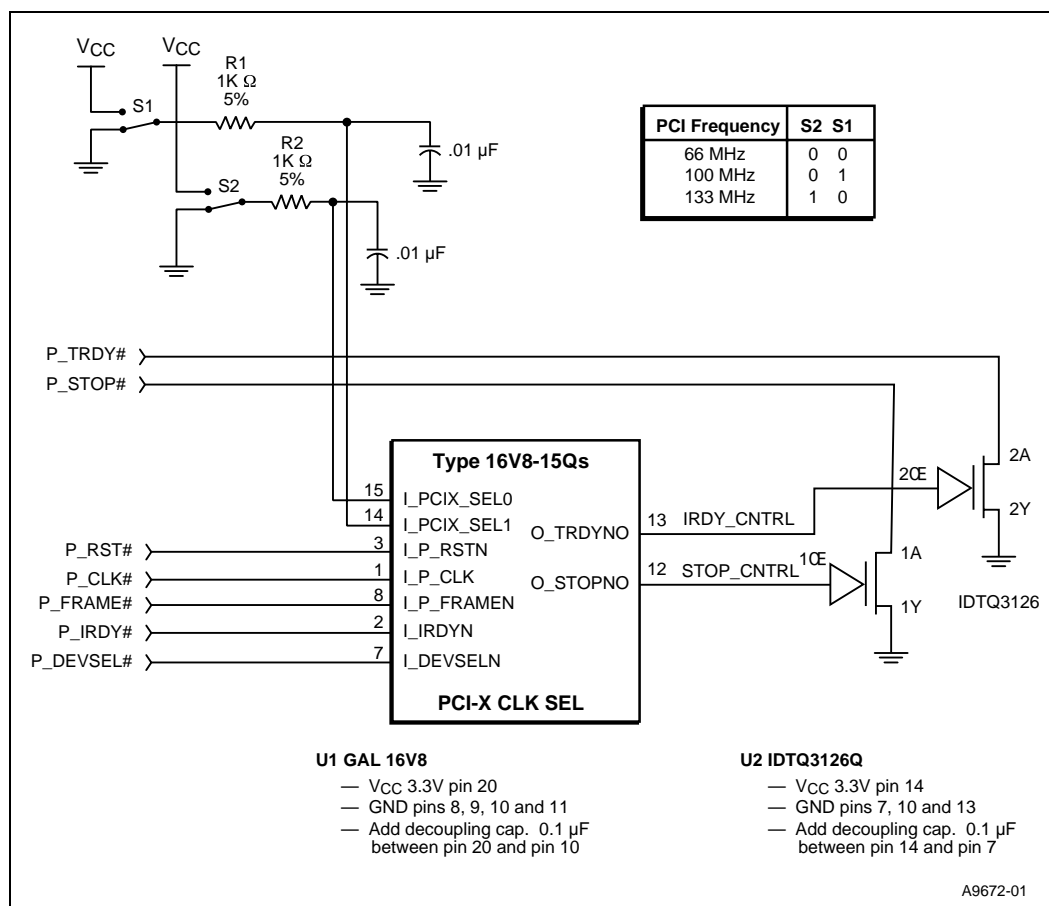
- The specification states that PCI clock is not stable and continuous during reset. However, it is required to be stable for 100 μ s prior to FRAME# being reasserted. This active clock requirement allows more than enough continuous clocks to control the logic described in this paper. Thus, all the logic described is synchronous to P_CLK.
- Referring to the timing specification in the last chapter, reset must be deasserted a minimum of five clocks before the first FRAME# is deasserted and the PCI-X initialization hold time must be less than 50 ns.
- PCI-X initialization pattern must be deasserted no later than two clocks before the first active FRAME# and floated no later than one clock before FRAME# is asserted.
- The PCI-X initialization hold time through the logic, using the Lattice* GAL 16V8-15 ns grade part, is sufficient to meet the maximum 50 ns requirement. There is approximately one clock delay from P_RST# high to the PCI-X initialization pattern being released. At the slowest PCI-X speed of 66 MHz, the clock period is 15 ns. With a one clock hold time, plus the 16V8 clock to out delay of 2.5 ns and the Quickswitch turn-off delay of 5.5 ns, there is a margin of approximately 27 ns from the 50 ns maximum hold requirement. This margin also meets the pattern to be deasserted two clocks prior to the first FRAME# being asserted.

3.3 P_TRDY# and P_STOP# Control

As shown in Table 1, the only two signals that need to be controlled during P_RST#, are P_TRDY# and P_STOP#. The signal P_DEVSEL# is always deasserted during P_RST# active for each of the PCI-X speeds. In the Figure 2, the signals TRDY_CNTRL and STOP_CNTRL are high active and provide control of U2 pins 1OE and 2OE. The component U2 is a IDT® Quickswitch. It was chosen for the low On resistance. A high on TRDY_CNTRL and STOP_CNTRL, activates the switch and pull to ground, P_TRDY# through pin 1A and P_STOP# through pin 2A.

Note: The signals P_TRDY# and P_STOP# already have pull-ups to V_{CC} with the recommended value of 4.7 K.

Figure 3. PCI-X Clock Select Example Design



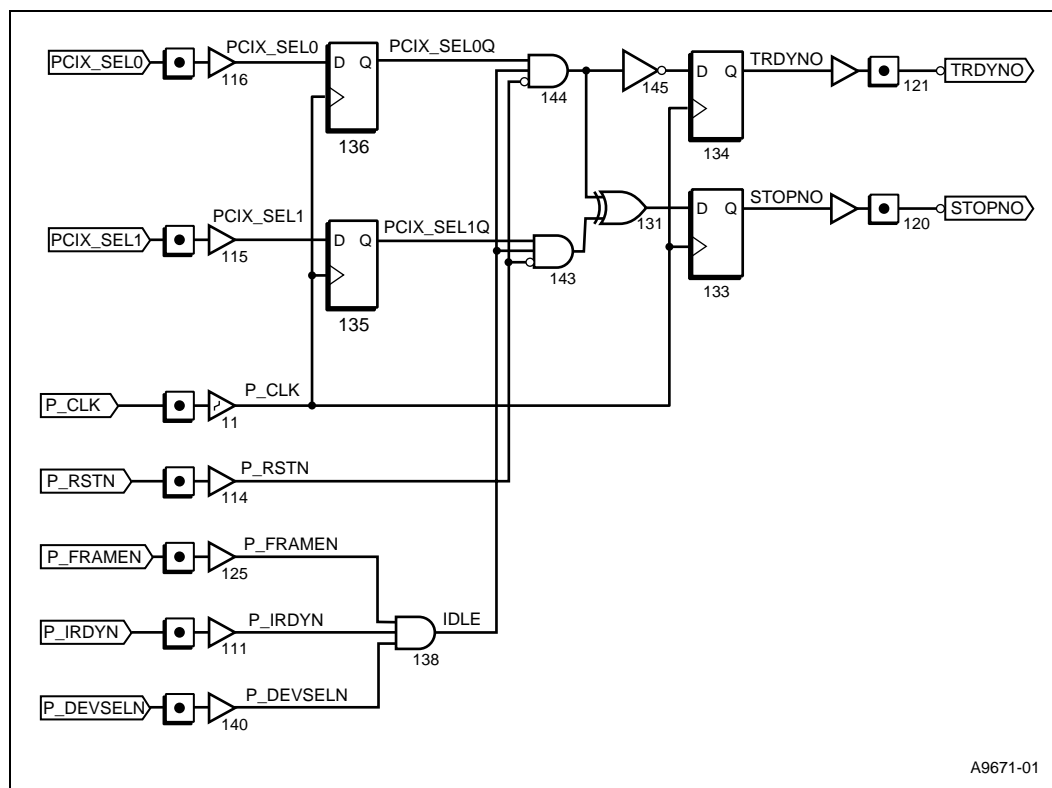
3.4 Programmable Logic Design for GAL

The logic design of the U1 was implemented using the schematic entry method, allowing it to be easily understood. The internal logic schematic was designed using Lattice* ispDesignEXPERT and compiled using Lattice ispEXPERT Compiler. The schematic is shown in Figure 4.

Note: PCIX_SEL0 and PCIX_SEL1, are synchronized using the internal D flip flops to help prevent metastability. P_IRDYN, P_FRAMEN, P_DEVSELN, are ANDed together to make sure that the bus is in the state of IDLE# during RESET#.

In most systems this is almost always the case. The designer may choose not to add this additional logic. It was added as a safeguard with the extra logic space in the GAL. TRDYNO and STOPNO signals are active approximately one clock after P_RST# gets deasserted.

Figure 4. U1 GAL Internal Schematic



3.5 Logic Equations

Below are the equations compiled from the schematic in Figure 4.

Note: “&” represents logic AND, “#” represents logic OR, and “!” is logic NOT.

Equations:

```
O_TRDYNO.D = (N_1);
O_TRDYNO.C = (P_CLK);
O_STOPNO.D = (N_2);
O_STOPNO.C = (P_CLK);
P_CLK = (I_P_CLK);
P_RSTN = (I_P_RSTN);
P_DEVSELN = (I_DEVSELN);
P_IRDYN = (I_IRDYN);
P_FRAMEN = (I_P_FRAMEN);
IDLE = (P_FRAMEN & P_IRDYN & P_DEVSELN);
PCIX_SEL0 = (I_PCIX_SEL0);
PCIX_SEL1 = (I_PCIX_SEL1);
PCIX_SEL0Q.D = (PCIX_SEL0);
PCIX_SEL0Q.C = (P_CLK);
PCIX_SEL1Q.D = (PCIX_SEL1);
PCIX_SEL1Q.C = (P_CLK);
N_1 = (!N_3);
N_2 = (N_3 & !N_4 # !N_3 & N_4);
N_3 = (!P_RSTN & PCIX_SEL0Q & IDLE);
N_4 = (!P_RSTN & PCIX_SEL1Q & IDLE);
```

3.6 Timing Example

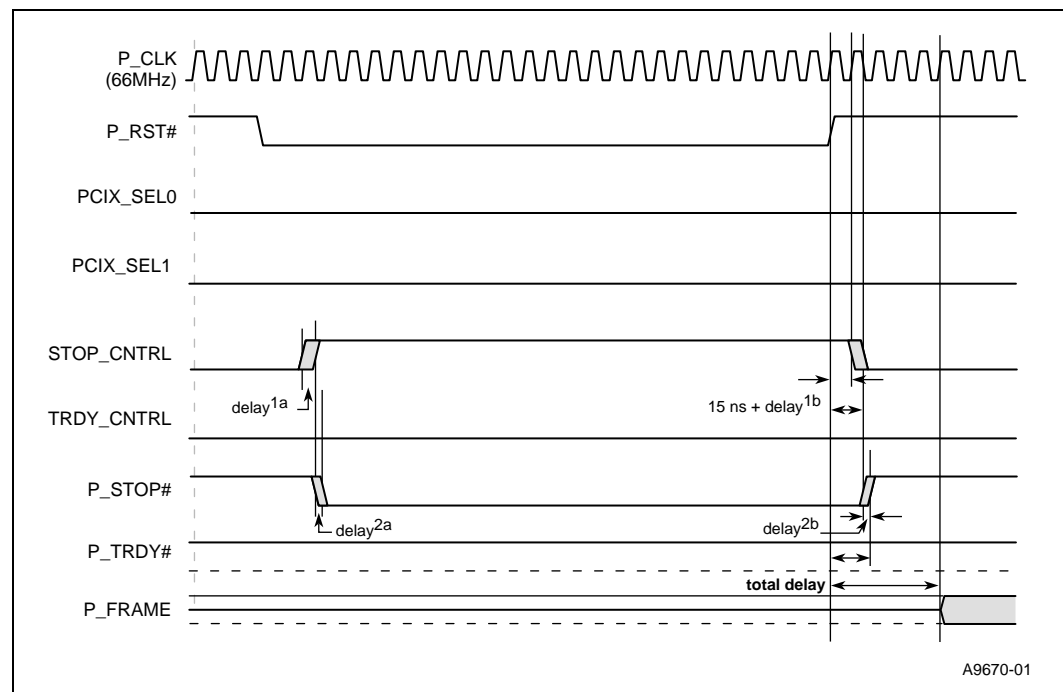
Figure 5 shows the timing for 66 MHz PCI-X selection. This diagram assumes that TRDY#, DEVSEL# and RST# are all deasserted and the bus is in IDLE mode during reset. The selection control lines PCIX_SEL0 = 0 and PCIX_SEL1 = 0 force the 80321 into 66 MHz mode. The delay^{1b} of the STOP_CNTRL going low, includes maximum clock to output delay of the 16LV8-3 of 2.5 ns. The delay^{2b} of plus, the Quickswitch maximum turn-off delay of 5.5 ns. The maximum **total delay** from P_RST# to the initialization pattern release is approximately 23 ns (within the 50 ns maximum specification). The five clock minimum time from RST# being asserted and the first FRAME# being deasserted, provides a minimum total time period of 75 ns at 66 Mhz. Table 4 details the total delay through logic for the different frequencies, to guarantee the design meets the 50 ns maximum hold and two clocks before FRAME# active rules.

Table 4. Total Delays vs. Frequency

Frequency (MHz)	1. RST# to Frame 5 clock (ns)	2. Total Delay (ns) (< 50 ns)	Pattern Release to Frame w/i 2 clocks Margin (ns) = col1 - col2
66	75	23	52
100	50	18	32
133	37.5	15.5	22

Note: Assumes the maximum 8 ns delay through logic (2.5 ns GAL plus 5.5 ns through QuickSwitch).

Figure 5. 66 MHz Timing Example



A9670-01



4.0 Summary

This White Paper provided an explanation of the requirements needed to initialize a PCI-X system frequency when the embedded 80321 application does not use a source bridge. The document discussed the timing requirements for initializing PCI-X frequencies. This document also provided a reference design as a guide. This extra logic can easily be incorporated into any embedded 80321 application.

Note: This example design has not yet been validated in actual hardware.

5.0 References

Table 5. Intel References

Document Title	Document #
<i>Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Developer's Manual</i>	273411
<i>Intel® 80200 Processor based on Intel® XScale™ Microarchitecture Datasheet</i>	273414
<i>Intel® 80321 I/O Processor Datasheet</i>	275318
<i>Intel® 80321 I/O Processor Developer's Manual</i>	273517
<i>Intel® 80321 I/O Processor Product Brief</i>	273525
<i>Intel® IQ80310 Evaluation Platform Board Manual</i>	273521
<i>Intel® 80321 I/O Processor Design Guide</i>	273520

Table 6. Other Useful References

Application References
<i>PCI-X Addendum to the PCI Local Bus Specification, Revision 1.0a</i>
<i>PCI Local Bus Specification, Revision 2.3; PCI Special Interest Group 1-800-433-5177</i>
<i>"PCI-X System Architecture" by Tom Shanley</i>





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