

Migrating Intel[®] 8033x I/O Processors to Intel[®] 81348 I/O Processor

Application Note

September 2006



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Revision History

Date	Revision	Description
September 2006	001	Initial Release.

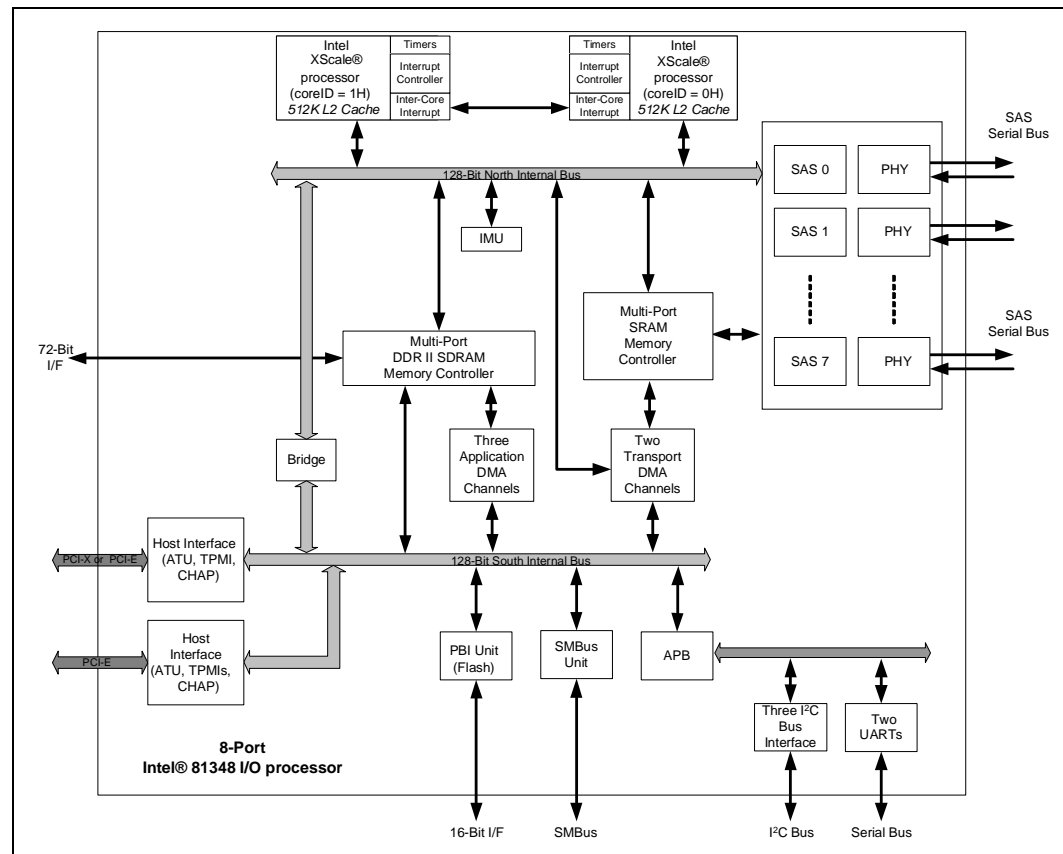


1.0 Introduction

Intel® 81348 I/O Processor (81348) has dual-core Intel XScale® technology¹ and dual-interface architecture. One of the cores is dedicated to running the SAS transport firmware (FW) and is called the "Transport Core." The other core is named the "Application Core" and is where customer BSPs and OSes execute. Intel provides a 2 MB binary that resides at 0x0 in Flash and provides for both initial boot code (for both cores, called "common boot"), as well as the transport core FW that provides the programming interface into the transport core. The common boot code model assures synchronized start-up of the cores, while maintaining maximum flexibility for the application core developer. Source code for the common boot code is not provided. However, full particulars on the state of the application core upon first customer instruction fetch, is to be fully detailed in the final documentation and covered later in this document.

The dual-interface denotes that there is no transparent bridge inside the 81348 microarchitecture. Instead, two Address Translation Units (ATUs) are implemented. One is the ATUe (which connects to a PCI Express Bus), the other is the ATU-X (which connects to a PCI-X bus). For the Host Bus Adapter Customer Reference Board Manual for Intel® 8134x I/O Processors (8134x HBA CRB), also referred to as the CRB, the host-connection is on the PCIe/ATUe unit and the ATU-X is the Central Resource for the PCI-X bus.

Figure 1. Intel® 81348 I/O Processor Functional Block Diagram



1. ARM* architecture compliant.



1.1 Related Documentation

The *Intel® 81348 I/O Processor Developer's Manual* covers the same kind of information as previous generations of I/O processors (IOPs); operation of the part and its various units, register interfaces, etc.

Please contact local Intel Field Service representative for additional SAS, SATA and SCDL questions.

Note: Consult the *Intel® 81348 I/O Processor Specification Update* frequently (or contact local Field Service Representative), since this migration document is intended to provide focus on functional areas that have changed from previous products and although it may touch on an occasional errata, it does not fully document or discuss *all* errata; **errata information are found in the specification update.**

1.2 Terms and Definitions

Table 1. Terms and Definitions (Sheet 1 of 2)

Term	Definition
AAU	Application Accelerator Unit
ADMA	Application DMA
API	Application Programming Interface
ARM	Refers to both the microprocessor architecture and the company that licenses it.
ATU	Address Translation Unit
ATUe	Address Translation Unit for PCI Express Bus
ATU-X	Address Translation Unit for PCI-X Bus
BSP	Board Support Package
CHAP	Chipset Hardware Architecture Performance
CP	Coprocessor
CRB	Customer Reference Board
DDR	Double Data Rate
DIMM	Dual Inline Memory Module
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
FW	Firmware
GB	Gigabit
I ² C	Inter-Integrated Circuit
IB	Internal Bus
IBL	Intel Business Link
ICU	Interrupt Controller Unit
IMU	Inter-processor Messaging Unit
I/O	In/Out
IOP	I/O processor
MB	Mega Bytes
MHz	Mega Hertz
MMU	Memory Management Unit
MU	Messaging Unit

**Table 1. Terms and Definitions (Sheet 2 of 2)**

Term	Definition
OS	Operating System
PBI	Peripheral Bus Interface
PCI	Peripheral Component Interface
PCIe	PCI Express bus
PCI-X	PCI-X bus
PHY	Physical Layer
SAS	Serial Attached 'Small Computer Systems Interface (SCSI)'
SATA	Serial Advanced Technology Attachment
SCDL	SAS Common Driver Library
SDRAM	Synchronous Dynamic Random Access Memory
SLI	Server Level Interface
SPD	Serial Presence Detect
SRAM	Synchronous Random Access Memory
TPMI	Third Party Messaging Interface
TSR	Test and Set Register
UART	Universal Asynchronous Receiver-Transmitter
XOR	Exclusive OR



2.0 ATUs (ATUe and ATU-X)

2.1 Register Offsets

The register offset for each ATU varies depending on how the Intel® 81348 I/O Processor device is strapped to operate. There is a strapping register in the PBI unit which can be read to determine how the device is strapped. The code below is the example of how to determine where each ATU base is located.

Note: The current relevant documentation does not document this register, refer to the example code below.

Table 2. Register Offsets

```
#define ATUX_BASE      (( *PBIU_ESSTSRO & CONTROLLER_ONLY) == 0) ? 0xffdcc000 : \
                      (( *PBIU_ESSTSRO & INTERFACE_SEL_PCIX) == 0) ? 0xffdc8000 \
                                                                0xffdcd000
#define ATUe_BASE     (( *PBIU_ESSTSRO & CONTROLLER_ONLY) && \
                      ( *PBIU_ESSTSRO & INTERFACE_SEL_PCIX)) ? 0xffdc8000 : \
                                                                0xffdcd000
```



2.2 Outbound Windows

There are four outbound windows for each ATU and they are located above the 4 GB memory region. Each of the four outbound windows is 4 GB in size. In order to access the outbound window for either ATU, the Intel XScale® technology must create SuperSection Page Table Descriptors for the MMU, which are new in the Manzano. These SuperSection descriptors map a 32-bit virtual address into a 36-bit physical address. Each SuperSection descriptor describes a memory range of 16 MB and the same SuperSection descriptor must be repeated in 16 consecutive memory locations in the MMU Table (as each entry in the table is to define 1 MB – so a 16 MB descriptor must be repeated 16x).

The Outbound Memory Windows only have a translate value register for the Upper 32-bits of a 64-bit address. The lower 32-bits of the Outbound Memory transaction pass through untranslated (in other words, there is no longer an outbound translation value register for the lower 32). The key point is that the SuperSection page table entries must be modified each time the Outbound Memory lower 32-bit window needs to slide.

The Outbound Enable bits in each ATU Configuration Register (offset 0x70) must be set to '1' before any outbound transactions occur. Be careful when setting the ATUe ATUCR register to just "OR", the register with a '2', so bit 6 is not cleared (which prevents hosts from booting).

2.2.1 Conflicts

The Outbound Memory Windows (OUMBARs) for the ATUe and ATU-X are enabled and overlap by default when the 81348 is powered on. This causes internal bus conflicts when writing to an Outbound Window, since each ATU tries to claim that address. The simplest fix is to only enable OUMBAR0 for ATU-X and OUMBAR1 for ATUe. The enable bit must be cleared in the other OUMBARs (Bit31) to disable them.

2.2.2 36-Bit Addresses

The SuperSection descriptors are new to the 81348 microarchitecture and allow 32-bit virtual addresses to be translated into 36-bit physical addresses. The *Intel XScale® Processor Developer's Manual* has details on how to program the 36-bit PT entries. Each PT entry references 16 MB of memory and the PT entry must be repeated in 16 consecutive locations in the MMU table.

2.3 Reset PCI-X Bus Operating as Central Resource

The 8134x HBA CRB CRB operates as a Central Resource on the PCI-X bus. This means that the Intel® 81348 I/O Processor has to release the Reset on the PCI-X bus, before scanning and configuring any devices. To deassert Reset on the PCI-X bus, clear bit 21 in the PCSR of the ATU-X. Once bit 21 is cleared, the Firmware must wait 2^{25} PCI Clocks before doing any cycles on the bus.

Note: 2^{25} PCI clocks is approximately 1.02 seconds at 33 MHz.



3.0 Messaging Unit

The circular queues must be initialized starting with the HEAD first and then the tail, or the queue is considered full and a write is continuously retried, causing a hang condition.

Figure 2. Required Initialization Order for Intel® 81348 I/O Processor Circular Queues

```
IN_FREE_HEAD_REG = IN_FREE_BOTTOM
IN_FREE_TAIL_REG = IN_FREE_BOTTOM
IN_POST_HEAD_REG = IN_POST_BOTTOM
IN_POST_TAIL_REG = IN_POST_BOTTOM
OUT_FREE_HEAD_REG = OUT_FREE_BOTTOM
OUT_FREE_TAIL_REG = OUT_FREE_BOTTOM
OUT_POST_HEAD_REG = OUT_POST_BOTTOM
OUT_POST_TAIL_REG = OUT_POST_BOTTOM
```

The MU is now a device on the Internal Bus (IB) and it can claim any transaction on the South IB, which hits its MUBAR/MUUBAR. This includes for example, using the ADMA for initial DDR memory scrub. Note that core access to memory does not conflict with the MU since the core comes in from the North IB and is isolated via the internal bridge. In situations where South IB access conflicts with the MU region, use the core to access that region of DDR.

Because the MU is now movable on the IB, the inbound translation value register, for the appropriate inbound BAR, is programmed to match the MU base, to assure inbound traffic translates as expected.

4.0 ADMA

The ADMA unit is different from previous IOPs (a careful review of the ADMA chapter in the relevant Developer’s Manual is recommended).

- The XOR engine is now included in the ADMA and is not a separate AAU unit.
- The descriptor format and register layout have changed from previous IOPs.
- The functionality of the ADMA is enhanced and can transfer to/from any internal bus unit into local SDRAM memory.

The key point to remember is that at least one of the legs of an ADMA transfer (source and/or destination) has to be SDRAM.



5.0 MCU

The following features are part of the MCU:

- Only CAS latency of four is supported.
- Only DDR-II DIMMs are supported, either 400 MHz or 533 MHz.
- DLLRCVER (offset 0x2030) values are not listed in the relevant Component Specification yet they need to be set to:

Table 3. DLLRCVER[10:8, 4:0]

Size	400 MHz 60 Ohms	400 MHz 50 Ohms	533 MHz 60 Ohms	533 MHz 50 Ohms
2"	000,00000	000,00000	000,00000	000,00000
4"	000,00000	000,00011	000,00100	000,00100
6"	000,01000	000,01101	000,10000	000,10001
8"	000,10001	000,10110	000,11101	000,11110

- The SDRAM Control, Base, and initialization registers (SDIR) have changed significantly.
For simplicity, when bringing up the BSP, avoid implementing the SPD scan, Refer to your DIMM datasheet for values to use.
You can use the JEDEC init sequence from the RedBoot* code (iq8134x_setup_mcu.c) to initialize the DIMM.
- 8134x HBA CRB specifics:
 - The SPD device is on I²C Bus#2.
 - MEM_FREQ speed determined by switch 5. Switch 5 "On (Up)" = 533 MHz.

5.1 SDIR

Register has been completely redefined. Refer to relevant Developer’s Manual for details.



5.2 SDCR0

The following features are part of the SDCR0:

- RAS Field is: SDCR0[31:28] for Intel® 80332 I/O processor (80332), SDCR0[31:27] for 81348 (equation is same).
- RP Field is: SDCR0[26:24] for 80332 and 81348 (No Change).
- RCD Field is: SDCR0[22:20] for 80332 and 81348 (No Change).
- tEDP Field is: SDCR0[17:16] for 80332, SDCR0[18:16] for 81348.
 - tEDP for 80332 is 10b.
 - tEDP for 81348 is:
 - 0x4 for Trace Length up to 8".
 - 0x5 for Trace Length up to 10".
- WDL Field is: SDCR0[13:12] on 80332 and 81348, but:
 - WDL for 81348 is based on an equation:
 $WDL = tCAS - 2$ (where tCAS is the CAS latency of the DIMM which must be ≥ 4).
(in other words, when a DIMM supports CAS latency of 3 and 4, 4 must be used)
- CAS Field is SDCR0[09:08] on 80332, and SDCR0[10:8] on 81348
 - CAS for 81348 is based on an equation:
 $CAS = tCAS - 1$ (where tCAS is the CAS latency of the DIMM, which must be ≥ 4).
(in other words, when a DIMM supports CAS latency of 3 or 4, 4 must be used)
- Reset Read FIFO is a new field on 81348 at SDCR0[07]. It must be set to 0x1.
- Internal Bus Address map Control is SDCR0[06] and is a new field in 81348. It can be set to change the row/address scheme for a DIMM. Refer to the relevant Component Specification for more details.
- SDCR0[05:04] is ODT on both 81348/80332. It is being set to 01b (75 Ohm) by RedBoot. (No Change).
- SDCR0[02] is DDR type, but is always set to 0 on 81348 to select DDR-II. It can be set to 1 on 80332 to select DDR.
- SDCR0[1] is bus width on both 80332 and 81348. (No Change)
- SDCR0[00] is the "DIMM Type" field, but must always be set to 0x1 on 81348, regardless of DIMM type. The DLLRCVER register is the method of selecting unbuffered/registered DIMM type on 81348.



5.3 SDCR1

The following features are part of the SDCR1:

- DQS# Disable is SDCR1[31] on both 80332 and 81348. (No Change)
- RTCMD is SDCR1[30:28] on 80332 and SDCR1[30:27] on Intel® 81348 I/O Processor. 81348 also uses an equation to calculate RTCMD. It is tRTP, which is from the SPD and must be equal to 0x2 for 400/533 MHz DIMMs.
- WTCMD is SDCR1[27:24] on 80332 and SDCR1[26:23] on 81348. The equation is different for 81348 - it is:

$$\text{WTCMD} = \text{tCAS} - 1 + (\text{BL}/2) + \text{tWR}$$
 - tCAS must be ≥ 4
 - BL = 4
 - tWR is from the SPD (you must convert into MCLKS)
- RTW is SDCR1[22:20] on 80332 and SDCR1[22:19] on 81348.
 - The equation is different for 81348, it is:

$$\text{RTW} = (\text{BL}/2) + 2$$
 Where BL = 4, so the result = 4
- RFC is SDCR1[16:12] on 80332 and SDCR1[17:12] on 81348, but the equation is the same.
- WR is SDCR1[11:09] on 80332 and SDCR1[11:09] on 81348.
 - The equation is different for 81348, it is:

$$\text{WR} = \text{tWR}$$
 where tWR is from the SPD (but must be converted to MCLKS)
- RC is SDCR1[08:04] on 80332 and 81348. (No Change)
- WTRD is SDCR1[3:0] on both 80332 and 81348, but the equation is different. On 81348, the equation is:

$$\text{WTRD} = \text{tCAS} - 1 + (\text{BL}/2) + \text{tWTR}$$
 - Where tCAS must be ≥ 4
 - BL = 4
 - tWTR is from the SPD (and must converted into MCLKS)
- The 81348 implements the SDUBR (SDRAM Upper Base Address Register) to provide the ability to place SDRAM in the 36-bit address range.
- The 81348 does not implement the SBR0/SBR1 (SDRAM Boundary Registers) of 80332, but instead uses:
 SBSR (SDRAM Bank Size Register). See relevant Component Specification for details on how to program this register.
 ECC Log registers have changed the definitions of the Requestor field due to the different requestors on the internal bus for DDR



6.0 SRAM

Although information on SRAM is in the current revision of the relevant Component Specification, SRAM is not available to the application core developer at any time. This chapter can be skipped when reviewing the relevant Component Specification.

7.0 PBI

The PBI on Ax 81348 only supports write accesses per the width of the bus, either 8 or 16. B0 silicon behaves as follows:

- 32-bit writes show up as 4x8-bit writes when in 8-bit mode
- 32-bit writes show up as 2x16-bit writes when in 16-bit mode
- 16-bit writes show up as 2x8-bit writes when in 8-bit mode
- 16-bit writes show up as 1x16-bit writes when in 16-bit mode
- 8-bit writes show up as 8-bit writes in 8-bit mode
- 8-bit writes are not supported in 16-bit mode
- Writes with address/byte counts are never permitted to cross a DWORD boundary

8.0 ICU

Information on TMPI INTs (interrupts from the transport core) is currently missing from the relevant Component Specification. Following are the relevant register information:

- INTPND3: Bit 7 indicates an outbound INT from TPMIO
- INTCTL3: Bit 7: 0=Masked 1=Unmasked for TPMIO outbound INTs
- INTSTR3: Bit 7: 0 directs TPMIO to IRQ, 1 to FIQ
- INTSRC3: 0 = Not Interrupting or Not steered to internal IRQ exception or masked by
- INTCTL3. 1 = Interrupting and steered to internal IRQ exception and unmasked by INTCTL3

Note: That TPMI outbound INTs are cleared in the SCDL.



9.0 I²C

I2C_Bus0 belongs to the transport core, I2C_Bus1 and I2C_Bus2 belong to the application core.

10.0 UARTS

UART0 belong to the transport core, UART1 to the application core.

11.0 MMRs

Because writes are posted, when an MMR value setting needs to be set before the next operation occurs, then a read from the MMR after the write must be issued, to guarantee that the data has made it to the MMR. The MMR base address defaults to 0xFFD8.0000 and each register in the relevant Component Specification is an offset from the MMR base address. Do not change this base address since it controls MMR access for the transport core as well. When register locations need to be remapped from the application core perspective, use the MMU to do this.

Note: In previous parts, many MMRs had dual-access, either memory mapped or coprocessor. In 81348 however, registers are either one or the other. For example, the ICU registers in 81348 are only accessible via CP access, whereas in the Intel® 80331 I/O processor (80331)/80332 they can be accessed via either method.



12.0 Application/Transport Core Interaction

The SSAS has the detailed documentation regarding the interactions, but here is a general overview. The Transport core is Core0 and its Core ID is 0. The Application Core is Core1 and its Core ID is "1". BSPs are ported to the Application Core and the Transport Core FW is provided in the Flash. The Application Core has its code burned into Flash at the 0x20.0000 (2M) offset. A "Common Boot Code", which is Intel Secret (source cannot be released) is stored in the Flash from 0x0 to 0x20.0000.

12.1 Transport Core (Core0) Owns

- UART0
- I2C_Bus0
- SRAM
- TPMI (except for interface to SLI on TPMIO)
- SAS PHYs

Caution: Application Core must not access or unpredictable results occur!

12.2 Application Core (Core1) Owns

Note: Transport Core does not access.

- UART1
- I2C_Bus1 and I2C_Bus2
- SDRAM



12.3 Rules for Both Cores

- PMMR Base is not to be changed.
- Flash not to be accessed without proper adherence to Flash semaphores. See Developer's Manual.

12.4 Flash Semaphores (FAC0 and FAC1)

Please contact local Intel Field Service representative for additional SAS, SATA and SCDL questions.

12.5 Common Boot Code

Please contact local Intel Field Service representative for additional SAS, SATA and SCDL questions.



12.6 New Intel XScale® Technology Considerations

12.6.1 SuperSection Descriptors

Supersection descriptors are a way to translate 32-bit virtual addresses into 36-bit physical addresses. This is important for accessing the Outbound windows of the ATUs because they are physically located above the 4 GB region and cannot be moved down into 32-bit address space.

12.6.2 L2

Each Manzano core has 512 KB of unified (instruction and data) cache on chip. The easiest way to deal with the L2 cache during first BSP bring-up is to not enable it. It is disabled by default and must be enabled in the ARM Control Register before it can be used.

The L2 Cache behaves a little different than L1, a quick summary is:

- Intel XScale® technology talks about Inner and Outer cacheability: Inner = L1 (Data or Instruction) and Outer = L2.
- L2 on the 81348 is 512k and it is unified, so both inst and data are cached.
- L2 must be enabled at the same time the MMU is enabled.
- L2 cannot be disabled directly by a coprocessor write. The only way to “disable” the L2 is to change the Page Table entries to be Non-Outer Cacheable for the region where you want to disable L2.

12.7 Developing a Transport Core Driver

Refer to Appendix A, Quickstart Guide for concise information on how to get a driver up and running quickly. The common driver library handles all internal bus addressing for TPMI control and memory access for you.

