Migrating from Intel® 80310 I/O Processor Chipset to Intel® 80321 I/O Processor

Application Note

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Contents

Figures

Tables

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1.0 Objective

This document describes both hardware and software considerations when migrating from the Intel® 80310 I/O processor chipset with Intel® XScale™ microarchitecture (ARM* architecture compliant) to the Intel® 80321 I/O processor (80321). Table 1 provides a summary of the major features of each product and how they are different. The sections that follow detail the differences between the major functional blocks and also detail the additional features that are offered by the 80321 including additional registers, pins and bit changes/additions in existing registers.

Table 1. Summary of Differences

Function	Intel® 80310 I/O Processor Chipset	Intel® 80321 I/O Processor
Core Voltage (V)	0.95 V - 1.55 V (Intel® 80200 processor) 3.0 V - 3.6 V (Intel® 80312 I/O companion chip)	0.75 V - 1.45 V (core) 2.5 V (DDR SDRAM) 3.3 V (80321 pads)
Processor Speeds	400, 600, 733 MHz	400, 600 MHz
Power	< 1 W @ 733 MHz (Intel® 80200 processor) 6 W (Intel® 80312 I/O companion chip)	Approximately 4.0 W @ 600 MHz (full chip)
Package/Size	80200: 241-Lead PBGA (27 mm x 27 mm) 80312: 540-Lead PBGA (42.5 mm x 42.5 mm)	544-Lead PBGA (35 mm x 35 mm)
Timers	PMU or external timers needed	Two 32-bit timer units Watchdog TImer
PCI-to-PCI Bridge	• 33 MHz or 66 MHz • 3.3 V and 5 V PCI signaling • Six secondary PCI output clocks • 256-byte upstream delayed read completion queue	• No PCI Bridge • 133 MHz Single PCI-X Bus • 3.3 V Signaling
Memory Control Unit	• 100 MHz SDRAM • 64, 128, 256 Mbit SDRAM • No 32-bit SDRAM support • ECC always on • Four SDRAM output clocks • Unbuffered DIMMs only	• 200 MHz DDR SDRAM • Up to 1 GB of 64-bit/512 MB of 32-bit DDR SDRAM. • 32-bit DDR SDRAM support • ECC selectable on/off • Unbuffered and Registered DIMMs • Supports write coalescing • 12 drive strength registers
DMA Queues	1 x 256 B/Channel	2 x 1 KB/Channel
Inbound/Outbound Queues - ATU	256 Bytes/16 Bytes	4 KB/4 KB
Peripheral Bus	Use Flash Bus: 8-Bit	33, 66, 100 MHz/ 8, 16, or 32 bits
Co-Processors	CP0 (DSP), 13 (INT), 14 (Debug), 15 (Cache)	CP0 (DSP), CP6 (INT, Timers), 7 (BIU), 14 (Debug), 15 (Cache)

1.1 Intel® 80310 I/O Processor Chipset and Intel® 80312 I/O Companion Chip

As indicated in Figure 1, the Intel® 80312 I/O companion chip (80312) combines with the Intel® 80200 processor (80200) to create the Intel® 80310 I/O processor chipset (80310).

Figure 2, is a block diagram of the 80312. For detailed functional descriptions, refer to the *Intel® 80312 I/O Companion Chip Developer's Manual* .

The PCI bus is an industry standard, high performance, low latency system bus that operates up to 528 Mbyte/s. The 80310, a multi-function PCI device, is fully compliant with the *PCI Local Bus Specification*, Revision 2.2. Function 0 is the PCI-to-PCI bridge unit; Function 1 is the address translation unit.

The PCI-to-PCI bridge unit is the path between two independent 64-bit PCI buses and provides the ability to overcome PCI electrical load limits. The addition of the 80200 brings intelligence to the bridge.

The internal bus, a 64-bit PCI-like bus, is a high-speed interface to local memory and I/O. Physical and logical memory attributes are programmed via memory-mapped control registers (MMRs).

Figure 1. Intel® 80310 I/O Processor Chipset System Block Diagram

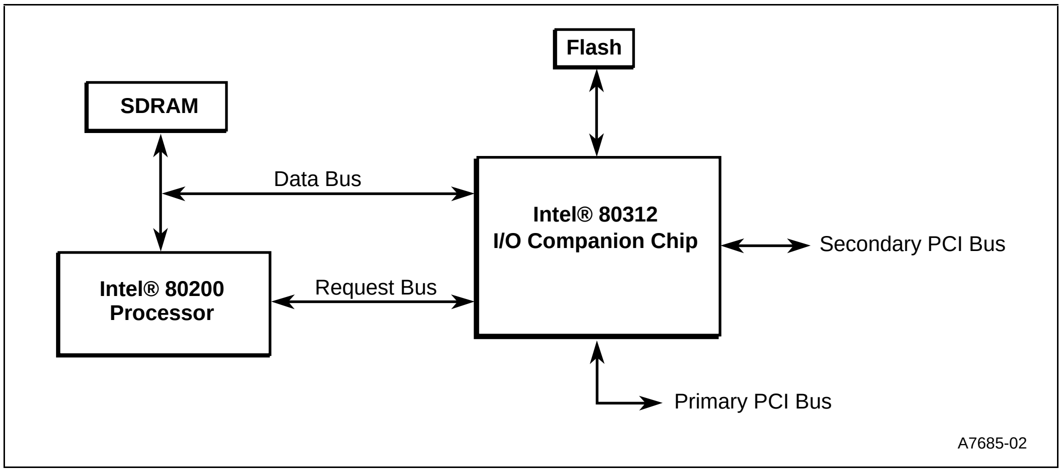
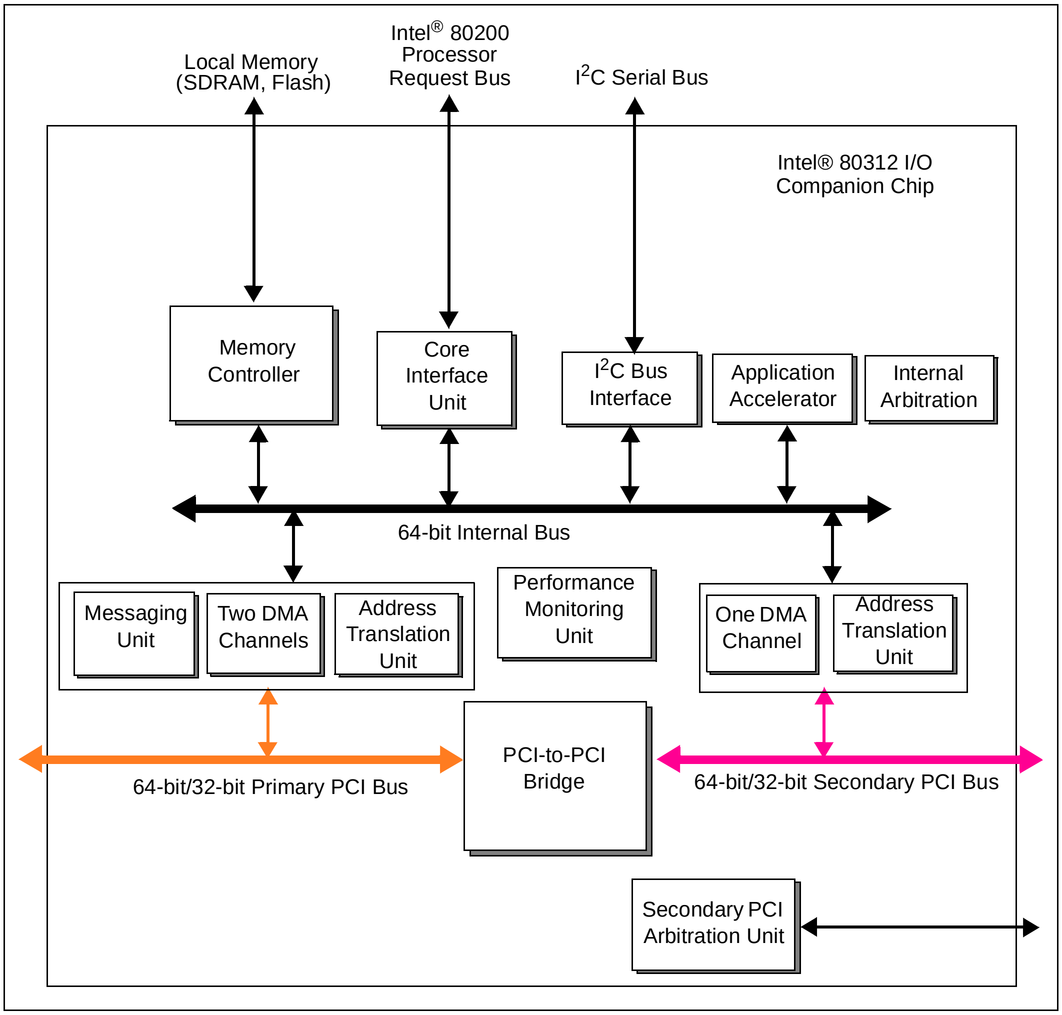


Figure 2. Intel® 80312 I/O Companion Chip Block Diagram



1.2 Intel® 80200 Processor Features

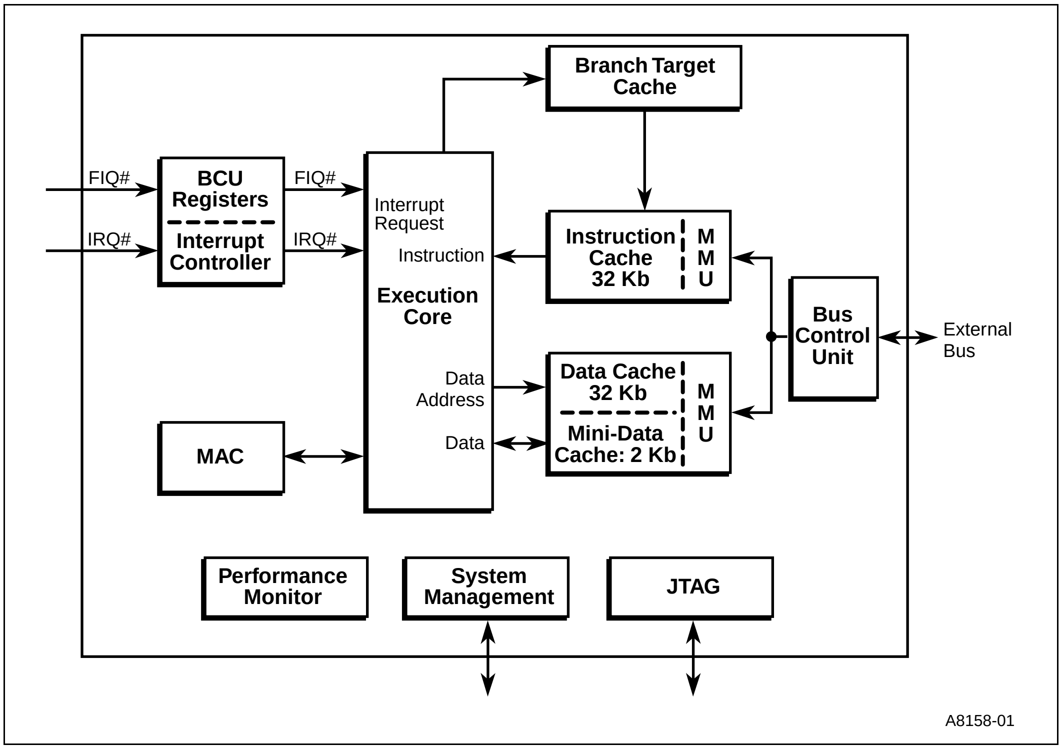
The 80312 was designed to directly interface to the 80200, using a 100 MHz bus (Figure 3). The 80200 was designed for high performance and low-power, leading the industry in mW/MIPS.

The 80200 incorporates several architecture features that allows it to achieve high performance.

Factors that contribute to the 80200 performance include:

- up to 733 MHz core frequency
- 7-stage superpipeline architecture
- 32 K, 32-way, lockable by line instruction cache
- 32 K, 32-way, write-back or write-through data cache
- 2 K, 2-way mini-data cache
- 4-entry Fill Buffer
- 8-entry Write Buffer
- 128-entry Branch Target Buffer
- ARM* v5TE instruction set architecture

Figure 3. Intel® 80200 Processor Block Diagram



1.3 About the Intel® 80321 I/O Processor

The 80321 is a single-function device that integrates the Intel® XScale™ core with intelligent peripherals including a PCI bus application bridge. The 80321 consolidates, into a single system:

- Intel® XScale™ core
- PCI - Local Memory Bus Address Translation Unit
- I_2O* Messaging Unit
- Direct Memory Access (DMA) Controller
- Peripheral Bus Interface Unit
- Integrated Memory Controller
- Performance Monitor
- Application Accelerator
- Two I^2C Bus Interface Units
- Synchronous Serial Port Unit
- Eight General Purpose Input Output (GPIO) ports

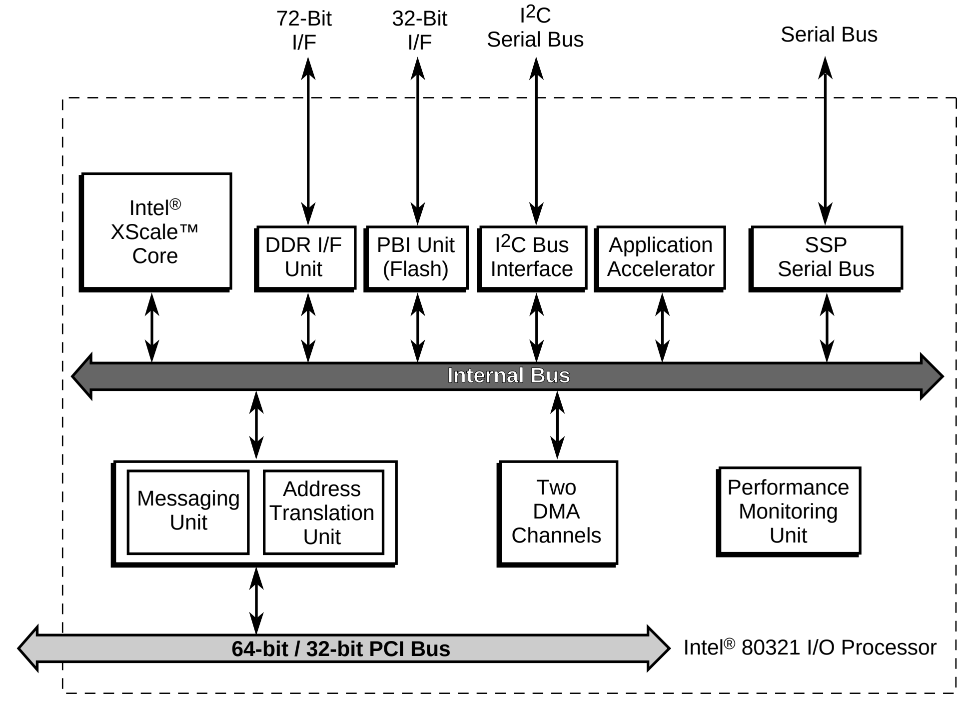
It is an integrated processor that addresses the needs of intelligent I/O applications and helps reduce intelligent I/O system costs.

The PCI Bus is an industry standard, high performance, low latency system bus. The 80321 PCI Bus is capable of 133 MHz operation in PCI-X mode as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. Also, the processor supports a 66 MHz conventional PCI mode as defined by the *PCI Local Bus Specification*, Revision 2.2. The addition of the Intel® XScale™ core brings intelligence to the PCI bus application bridge.

The 80321 is a single-function PCI device. This function represents the address translation unit. The address translation unit is an ‘application bridge’ as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a. The 80321 contains PCI configuration space accessible through the PCI bus.

Figure 4 is a block diagram of the Intel® 80321 I/O processor.

Figure 4. Intel® 80321 I/O Processor Functional Block Diagram



Notes:
Intel XScale Microarchitecture is ARM* Architecture compliant.
* Other brands and names are the property of their respective owners.

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2.0 Address Translation Unit (ATU)

PCI-X Mode:	Delayed read transactions are replaced by split read transactions
Four Base Address Registers (BAR):	Additional ATU Inbound Translation Windows have been added, BAR1, BAR2 and BAR3. BAR3 is a private BAR that resides outside of the standard PCI configuration header space of (00H – 3FH)

2.1 Queue Sizes

Table 2. ATU Queue Sizes

Queue	Intel® 80312 I/O Companion Chip	Intel® 80321 I/O Processor
Outbound Read Queue	16 B	2 KB or 4 KB
Outbound Write Queue	16 B	4 KB
Inbound Read Queue	256 B	4 KB
Inbound Read Queue	256 B	4 KB

2.2 PCI Function Power Management State

D1 Power Management State is supported on the 80321. D1 state is a light sleep state. Some functions may be processing background tasks such as monitoring the network which actually requires most of the function to be active. In this state, the only PCI operation the PCI function is allowed to initiate is a PME. The function is only allowed to respond to PCI configuration accesses (e.g., memory and I/O spaces are disabled). Configuration Space must be accessible by system software while the function is in D1.

When a function supports this state when operating on a 33 MHz PCI bus, it also supports it when operating on a 66 MHz PCI bus (when 66 MHz operation is supported).

See *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.

Table 3. New or Changed ATU Registers in the Intel® 80321 I/O Processor (Sheet 1 of 2)

Register Name	Internal Bus Address	Default Value	Register Description
ATUBISTR	FFFF E10FH	0000 0000H	ATU BIST Register – The ATU BIST Register controls the functions the Intel® XScale™ core performs when BIST is initiated.
IABAR0-3	FFFF E110H, FFFF E118H, FFFF E120H, FFFF E190H	0000 000CH, 0000 0000H, 0000 0000H, 0000 0000H	Inbound ATU Base Address Registers 0-3 – The IABAR0-3 together with the IAUBAR0-3 defines the block of memory address where the inbound translation window 0-3 begins.
IAUBAR0-3	FFFF E114H, FFFF E11CH, FFFF E124H, FFFF E194H	0000 0000H	Inbound ATU Upper Base Address Register 0-3 – These registers contain the upper base address when decoding PCI addresses beyond 4 Gbytes.
IALR0-3	FFFF E140H, FFFF E150H, FFFF E154H, FFFF E198H	0000 0000H, FF00 0000H, 0000 0000H, 0000 0000H	Inbound ATU Limit Register 0-3 – Inbound address translation for memory window 0-3 occur for data transfers occurring from the PCI bus (originated from the PCI bus) to the 80321 internal bus. The address translation block converts PCI addresses to internal bus addresses.

Table 3. New or Changed ATU Registers in the Intel® 80321 I/O Processor (Sheet 2 of 2)

Register Name	Internal Bus Address	Default Value	Register Description
IATVR0, 2, 3	FFFF E144H, FFFF E158H, FFFF E19CH	FF00 0000H, 0000 0000H, 0000 0000H	Inbound ATU Translate Value Register 0, 2, 3 – The IATVR0, 2, 3 contains the internal bus address used to convert PCI bus addresses.
OIOWTVR	FFFF E15CH	0000 0000H	Outbound I/O Window Translate Value Register – The OIOWTVR contains the PCI I/O address used to convert the internal bus to a PCI address.
OMWTVR0, 1	FFFF E160H, FFFF E168H	0000 0000H	Outbound Memory Window Translate Value Register 0,1 – The OMWTVR0,1 contains the PCI address used to convert 80321 internal bus addresses for outbound transactions.
OUMWTVR0, 1	FFFF E164H, FFFF E16CH	0000 0000H	Outbound Upper 32-bit Memory Window Translate Value Register 0,1 – The OUMWTVR0,1 defines the upper 32-bits of address used during a dual address cycle.
OUDWTVR	FFFF E178H	0000 0000H	Outbound Upper 32-bit Direct Window Translate Value Register – The OUDWTVR defines the upper 32-bits of address used during a dual address cycle for the transactions via Direct Address
PCSR	FFFF 184H	Varies with ext. state of P_DEVSEL#, PSTOP#, P_TRDY#, P_M66EN, and PREQ64#	PCI Configuration and Status Register – The PCSR has additional bits for controlling and monitoring various features of the PCI bus interface.
ATUIMR	FFFF E18C	0000 0900H	ATU Interrupt Mask Register – The ATUIMR contains the control bit to enable and disable interrupts generated by the ATU.
PM_Cap_ID	FFFF E1CO	01H	PM Capability Identifier Register – For the 80321, this is the PCI Bus Power Management extended capability with an ID of 01H as defined by the *PCI Bus Power Management Interface Specification,* Revision 1.1.
PM_Next_Item_Ptr	FFFF E1C1	D0H	PM Next Item Pointer Register – This register describes the location of the next item in the function’s capability list. For the 80321, the next capability (MSI capability list) is located at offset D0H.
PCI-X_Cap_ID	FFFF E1E0H	07H	PCI-X Capability Identifier Register – For the 80321, this is the PCI-X extended capability with an ID of 07H as defined by the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a.
PCI-X_Next_Item_Ptr	FFFF E1E1H	00H	PCI-X Next Item Pointer Register – For the 80321, this is the final capability list, and hence, this register is set to 00H.
PCIXCMD	FFFF E1E2H	0030H	PCI-X Command Register – This register controls various modes and features of ATU and Message Unit when operating in the PCI-X mode.
PCIXSR	FFFF E1E4H	05Bx FFF8	PCI-X Status Register – This register identifies the capabilities and current operating mode of ATU, DMAs and Messaging Unit when operating in PCI-X mode.

Table 4. New or Changed ATU Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
ATUSR.10:9	FFFF E106H	01	DEVSEL# Timing
ATUHTR.7	FFFF E10EH	0	Single Function/Multi-Function Device
ATU_Cap_PTR.6	FFFF E134H	1	Capability List Pointer
ATUCR.21,20,17,12,7,2	FFFF E180H	00,0,0,0,0,0	Reserved
ATUCR.3	FFFF E180H	0	ATU BIST Interrupt Enable
ATUISR.8	FFFF E188H	0	ATU BIST Interrupt
ATUISR.12	FFFF E188H	0	Received Split Completion Error Message
ATUISR.13	FFFF E188H	0	Initiated Split Completion Error Message
ATUISR.14	FFFF E188H	0	ATU Inbound Memory Window 1 Base Updated
ATUIMR.8	FFFF E18CH	1	Power State Transition Interrupt Mask
ATUIMR.9	FFFF E18CH	0	Received Split Completion Error Message Interrupt Mask
ATUIMR.10	FFFF E18CH	0	Initiated Split Completion Error Message Interrupt Mask
ATUIMR.11	FFFF E18CH	1	ATU Inbound Memory Window 1 Base Updated Mask

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 3.

3.0 Messaging Unit (MU)

The Messaging Unit for the 80321 is the same as the Messaging Unit on the 80312 with the exception of the Message-Signaled Interrupt described in the Address Translation Unit section.

3.1 Message-Signaled Interrupts (MSI)

The Messaging Unit is responsible for the generation of all of the Outbound Interrupts from the 80321. These interrupts can be delivered to the Host Processor via the **P_INTA#** output pin or the Message-Signaled Interrupt (MSI) mechanism.

When a host processor enables MSI on the 80321, an outbound interrupt is signaled to the host via a PCI write instead of the assertion of the **P_INTA#** output pin.

Support of message-signaled interrupts is optional for systems and system software.

PCI-X devices that generate interrupts are required to support message-signaled interrupts and must support a 64-bit message address. Implementation of these features is specified in *PCI Local Bus Specification*, Revision 2.2. Devices that require interrupts in systems that do not support message-signaled interrupts must also implement interrupt pins.

System software must not assume that a message-capable device has an interrupt pin. Devices that rely on polling for device service in systems that do not support message-signaled interrupts are permitted to implement messages to increase performance in systems that do support it.

Table 5. New or Changed MU Registers in the Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
Cap_ID	FFFF E2D0	05H	MSI Capability Identifier Register – The value of 05H in this field identifies the function as message signaled interrupt capable.
MSI_Next_Ptr	FFFF E2D1H	E0H	MSI Next Item Pointer Register – This register describes the location of the next item in the function capability list
Message_Control	FFFF E2D2H	0082H	Message Control Register – This register provides system software control over MSI.
Message_Address	FFFF E2D4H	0000 0000H	Message Address Register – This register specifies he DWORD aligned address for the MSI memory write transaction. The value is set by system software during initialization.
Message_Upper_Address	FFFF E2D8H	0000 0000H	Message Upper Address Register – This register is set during system initialization when system software wishes to place MSI address location above 4G address boundary.
Message_Data	FFFF E2DCH	0000H	Message Data Register – The value in this register contains the data used during and MSI write transaction.

Table 6. New or Changed MU Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
ODR.31-29	FFFF E32CH	000	Reserved
OISR.7-5	FFFF E330H	000	Reserved
OIMR.7-5	FFFF E334H	000	Reserved

See *Intel® 80321 I/O Processor Developer’s Manual*, Chapter 4.

4.0 DMA Controller Unit

The 80321 DMA Controller Unit optimizes block transfers of data between the PCI bus and the local processor memory and local memory to local memory transfers. The DMA Controller Unit resides on the Internal Bus and *does not have an independent PCI interface*. The 80321 has two DMA units accessible through the internal bus versus three for the 80310 that are all accessible through the internal bus as well as through the PCI bus.

4.1 Queue Sizes

Table 7. DMA Controller Unit Queue Sizes

Queue	Intel® 80312 I/O Companion Chip	Intel® 80321 I/O Processor
Data; Ch-0 and Ch-1	1 - 256 B	2 - 1 KB per channel
Burst Support	528 MB/sec (PCI) 800 MB/sec (IB)	1064 MB/sec (PCI-X) 1600 MB/sec (IB)

4.2 The Descriptor Control Register (DCR)

One extra bit added, Bit 6 which is detailed in Table 8.

Table 8. New or Changed DMA Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
CSR.1	FFFF E404/44H	0	Unknown PCI-X Split Transaction Error.
DCR.5	FFFF E424/64H	0	Has no effect.
DCR.6	FFFF E424/64H	0	Memory-to-Memory Xfer Enable – When set, the ATU no longer automatically forwards DMA transactions in the PCI address range defined by the 80321 external PCI bus.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 5.

5.0 Application Accelerator Unit (AAU)

The 80321 allows for a XOR-transfer with up to 32 source blocks of data versus only eight for the 80312. This has resulted in the addition of Source Address Registers (SAR) 9 – 32.

5.1 Extended Descriptor Control Registers (EDCR)

Three new registers have been added; EDCR0, EDCR1, EDCR2, see Table 9 for details. These registers are loaded when a chain descriptor that requires a minimum of 16 Source Addresses is read from memory. The values in the EDCRx define the command/control values as follow:

EDCR0: SAR16 – SAR9
EDCR1: SAR24 – SAR17
EDCR2: SAR32 – SAR25

Table 9. New or Changed AAU Registers in the Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
SAR9-32	FFFF E840 – FFFF E8A4H	0000 0000H	Source Address Register9-32 – Each of these registers is loaded with blocks of data to be operated upon by the AAU
EDCR0	FFFF E83CH	0000 0000H	Extended Descriptor Control Register 0 – The values in EDCR0 define the command/control value for SAR16 – SAR9.
EDCR1	FFFF E860H	0000 0000H	Extended Descriptor Control Register 1 – The values in EDCR1 define the command/control value for SAR24 – SAR17.
EDCR2	FFFF E884	0000 0000H	Extended Descriptor Control Register 2 – The values in EDCR2 define the command/control value for SAR32 – SAR25.

5.2 The Accelerator Descriptor Control Register (ADCR)

Three additional bits added, bits 28, 29 and 30 which is detailed in Table 10.

Table 10. New or Changed AAU Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
ADCR.26,25	FFFF E828H	00	Supplemental Block Control Interpreter – This bit field specifies the number of data blocks on which the operation is executed.
ADCR.28	FFFF E828H	0	Transfer Complete – This bit is set when the AA completes the processing of the descriptor.
ADCR.29	FFFF E828H	0	Parity Error – This bit is set when the bit wise parity computed across the data blocks specified by the SARx registers results in the detection of bad parity.
ADCR.30	FFFF E828H	0	Parity Enable – When this bit is set the AA computes the parity across the data blocks specified by the SARx registers.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 6.

6.0 Memory Controller (MCU)

See Table 1 for a summary of the key features of the 80321 Memory Controller.

Table 11. New or Changed MCU Registers in the Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
DBUDSR	FFFF E554H	0000 0000H	Data Bus Pull-up Drive Strength – The DBUDSR is used to control the strength of the p-drivers for DQ[63:0], DM[8:0], CB[7:0] and DQS[8:0] signals.
DBDDSR	FFFF E558H	0000 0000H	Data Bus Pull-Down Drive Strength – The DBDDSR is used to control the strength of the n-drivers for the DQ[63:0], DM[8:0], CB[7:0] and DQS[8:0] signals.
CUDSR	FFFF E55CH	0000 0000H	Clock Pull-Up Drive Strength – The CUDSR is used to control the strength of the p-drivers for the M_CK[2:0] and M_CK[2:0]# clock signals.
CDDSR	FFFF E560H	0000 0000H	Clock Pull-Down Drive Strength – The CDDSR is used to control the strength of the n-drivers for the M_CK[2:0] and the M_CK[2:0]# clock signals.
CEUDSR	FFFF E564H	0000 0000H	Clock Enable Pull-Up Drive Strength – The CEUDSR is used to control the strength of the p-drivers for the CKE[1:0] signals.
CEDDSR	FFFF E568H	0000 0000H	Clock Enable Pull-Down Drive Strength – The CEDDSR is used to control the strength of the n-drivers for the CKE[1:0] signals.
CSUDSR	FFFF E56CH	0000 0000H	Chip Select Pull-Up Drive Strength – The CSUDSR is used to control the strength of the p-drivers for the CS[1:0]# signals.
CSDDSR	FFFF E570H	0000 0000H	Chip Select Pull-Down Drive Strength – The CSDDSR is used to control the strength of the n-drivers for the CS[1:0]# signals.
REUDSR	FFFF E574H	0000 0000H	Receive Enable Pull-Up Drive Strength – The REUDSR is used to control the strength of the p-drivers for the RCVENO# output signals.
REDDSR	FFFF E578H	0000 0000H	Receive Enable Pull-Down Drive Strength – The REDDSR is used to control the strength of the n-drivers for the RCVENO# output signal.
ABUDSR	FFFF E57CH	0000 0000H	Address Bus Pull-Up Drive Strength – The ABUDSR is used to control the strength of the p-drivers for the MA[12:0], BA[1:0], RAS#, CAS# and WE# signals.
ABDDSR	FFFF E580H	0000 0000H	Address Bus Pull-Down Drive Strength – The ABDDSR is used to control the n-drivers for the MA[12:0], BA[1:0], RAS#, CAS# and WE# signals.

There are several new bit functions that have been added to the Memory Controller of the 80321 which are listed in Table 12.

Table 12. New or Changed MCU Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
SDIR.3	FFFF E500H	1	Special DDR SDRAM Command – These bits [3:0] are used for DDR SDRAM initialization.
SDCR.1	FFFF E504H	0	DIMM Type – Selects unbuffered or registered DIMM operating modes for the MCU.
SDCR.2	FFFF E504H	0	Data Bus Width – Indicates width of data bus; 32/64 bits
SDCR.12:3	FFFF E504H	000H	**Bits are now Reserved**. Separate registers added for drive strength. See Table 19, “Memory Controller Signal” on page 31
SBR0.5:0	FFFF E50CH	0H	SDRAM Boundary – Defines upper limit of SDRAM bank 0.
SBR0.31	FFFF E50CH	0	SDRAM Technology – Defines memory subsystem technology.
SBR1.5:0	FFFF E510H	0H	SDRAM Boundary – Defines upper limit of SDRAM bank 1.
SBR1.31	FFFF E510H	0	SDRAM Technology – Defines memory subsystem technology.
ECCR.3	FFFF E534H	0	ECC Enable – Enables ECC
ELOG0/1.23:16	FFFF E538/3C	00H	ECC Error Requester – Indicates requester of logged error.
RFR.12,11	FFFF E550H	00	Refresh Interval.

The following sections describe several registers that have been **DELETED**.

6.1 Flash Base Registers 0-1 (FEBR0-1)

The bits in these registers were used to define the upper 16 bits of the Flash base address for each Flash bank. This function is now incorporated in the PBI Base Address Registers; PBBAR0-5.

6.2 Flash Bank Size Registers 0-1 (FBSR0-1)

The bits in these registers were used to define the size for each Flash bank. This functions is now incorporated in the PBI Limit Registers; PBLR0-5.

6.3 Flash Wait States Registers 0-1 (FWSR0-1)

The bits in these registers were used to define the number of wait states for various read/write transactions. This functions is now incorporated in the PBI Base Address Registers; PBBAR0-5.

See *Intel® 80321 I/O Processor Developer’s Manual*, Chapter 7.

7.0 Peripheral Bus Interface Unit (PBI)

The Peripheral Bus Interface Unit (PBI) is a data communication path to certain components of an 80321 hardware system that do not have PCI bus interface and/or do not optimally reside on the PCI Bus. Examples of such components include Flash Memory and the DSP host interface port. The PBI allows the processor to manipulate data and interact with these components in the I/O environment. To perform these tasks at high bandwidth, the bus features a burst transfer capability which allows successive 32-bit data transfers.

The PBI also provides the following features:

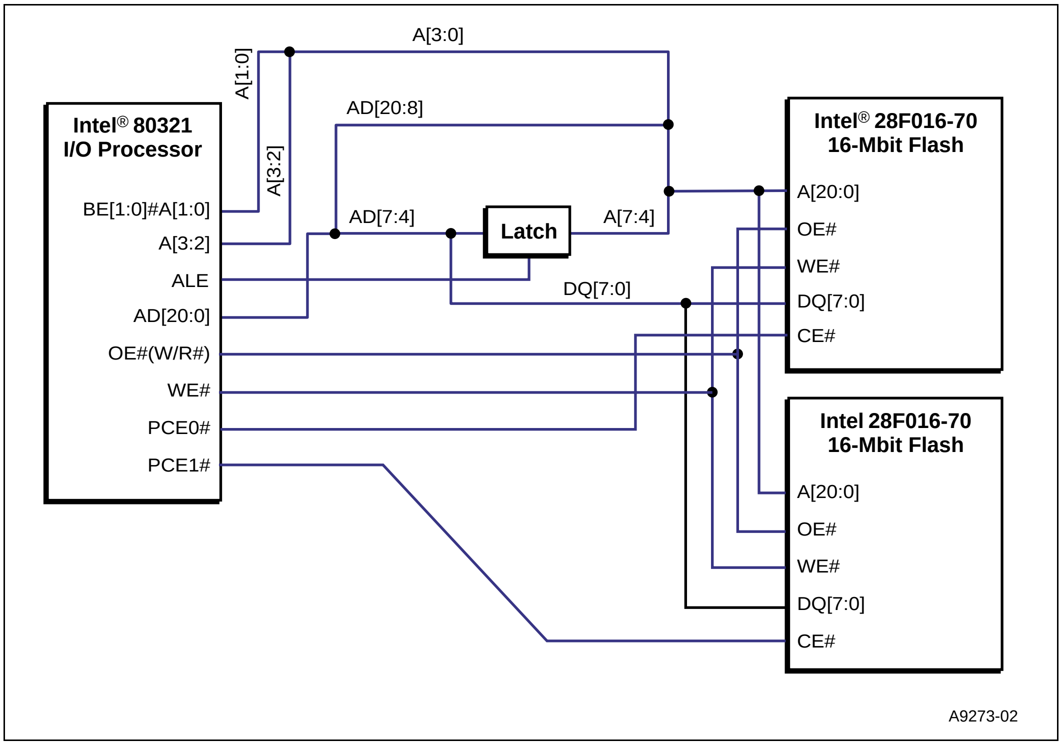
- Similar to the Intel® i960® RP/RD I/O processor local bus.
- 33 MHz, 66 MHz, and 100 MHz operating modes.
- Address/data path is multiplexed for economy.
- Bus width is programmable to 8-, 16-, and 32-bit widths.
- All bus transactions are synchronized with the processor clock output (**PB_CLK**); therefore, the memory system control logic can be implemented as state machines.
- The peripheral bus reset output pin **PB_RST#** mirrors the **P_RST#** includes six chip enables used to activate the appropriate peripheral device.

7.1 Flash Memory Support

The PBI peripheral bus interface supports 8-, 16-, or 32-bit Flash devices. Since the Flash wait state profiles for Recovery and Address-to-Data wait states are deterministic, the PBI provides programmable wait states functionality for windows configured for Flash. This saves the system designer from having to provide logic to assert RDYRCV# externally for Flash devices.

Figure 5 illustrates how two 8-bit Flash devices interface with the 80321 through the PBI interface.

Figure 5. Four Mbyte Flash Memory System



Note: 16-bit wide Flash devices require two latches and 32-bit wide Flash devices require three latches.

Several additional registers have been added to support this new feature. In addition, several functions that were present in the 80310 register set have been incorporated in the PBI Unit register set. Please see the Peripheral Bus Interface Unit chapter of the *Intel® 80321 I/O Processor Developer's Manual* for more details on these registers.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 8.

8.0 I²C Bus Interface Units

The 80321 has two I²C Bus Interface Units versus only one on the 80312. The two units on the 80321 are the same as the one unit on the 80312 with the following exceptions:

Registers added for the additional I²C Bus Interface Unit

The following section describes one register that has been **DELETED**.

8.1 I²C Clock Count Register (ICCR)

Nine bits in this register were used to generate an I²C clock from the 80312. This function is now incorporated in the I²C Control Registers; ICR0-1, Bit 15.

Table 13. I²C Bus Interface Unit Register Bit Changes

Bit Position	Internal Bus Address	Default Value	Bit Function
ICR0,1.15	FFFF F680/A0H	0	Fast Mode – 0 = 100 Kbit/sec operation 1 = 400 Kbit/sec operation

Another item worth mentioning is that the I²C control pins (SDA1, SCL1, SDA0, SCL0) on the 80321, are multiplexed with several of the GPIO pins (GPIO[4], GPIO[5], GPIO[6], GPIO[7]) respectively. Refer to the *Intel® 80321 I/O Processor Datasheet* for more details.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 9.

9.0 SSP Serial Port

The SSP Serial Port is a new feature that has been added to the 80321. The SSP Serial Port is a full-duplex synchronous serial interface. It can connect to a variety of external analog-to-digital (A/D) converters, audio and telecom codecs, and many other devices which use serial protocols for transferring data. It supports National Microwire*, Texas Instruments* synchronous serial protocol (SSP), and Motorola serial peripheral interface (SPI) protocol.

The SSP operates in master mode (the attached peripheral functions as a slave), and supports serial bit rates from 7.2 KHz to 1.84 MHz. Serial data formats may range from 4 to 16 bits in length. Two on-chip register blocks function as independent FIFOs for data, one for each direction. The buffers are 16 entries deep x 16 bits wide.

Buffers may be burst-loaded or emptied by the system processor using SRAM-like burst transfers, from 1 to 8 words per transfer. Each 32-bit word from the system fills one entry in a FIFO using the lower half 16 bits of a 32-bit word.

Several additional registers have been added to support this new feature. Please see the SSP Serial Port chapter of the *Intel® 80321 I/O Processor Developer's Manual* for more details on these registers.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 10.

10.0 Arbitration Unit

Figure 6. Intel® 80312 I/O Companion Chip Arbitration Block Diagram

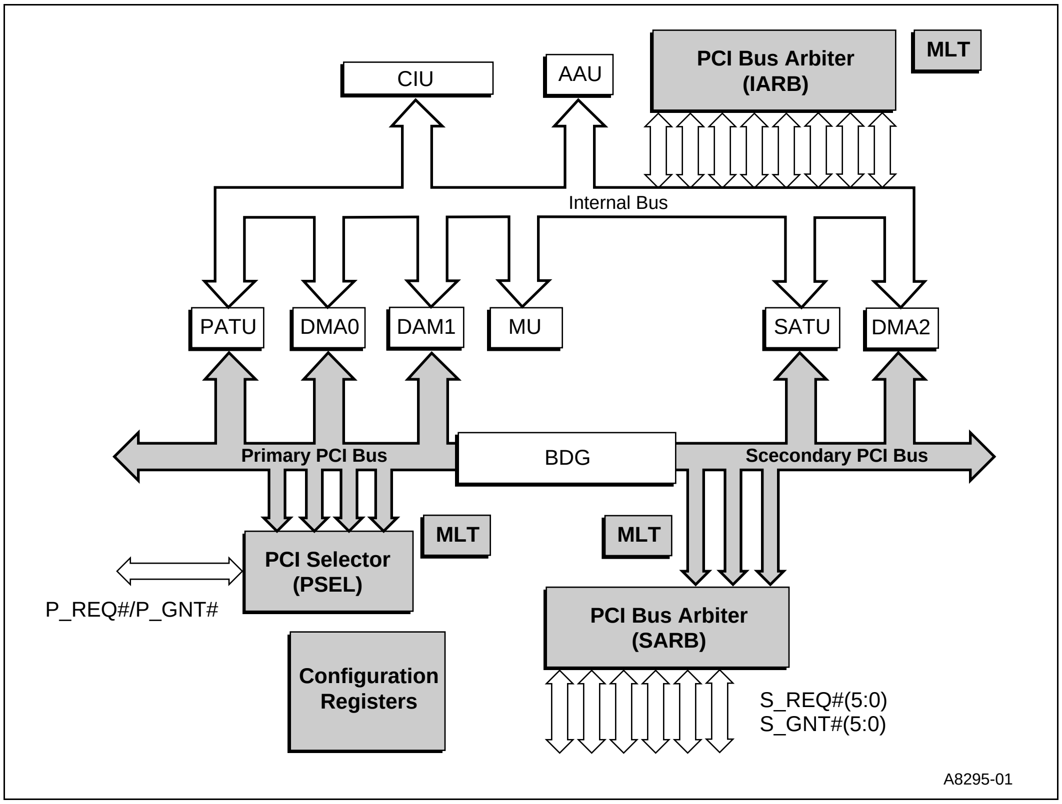
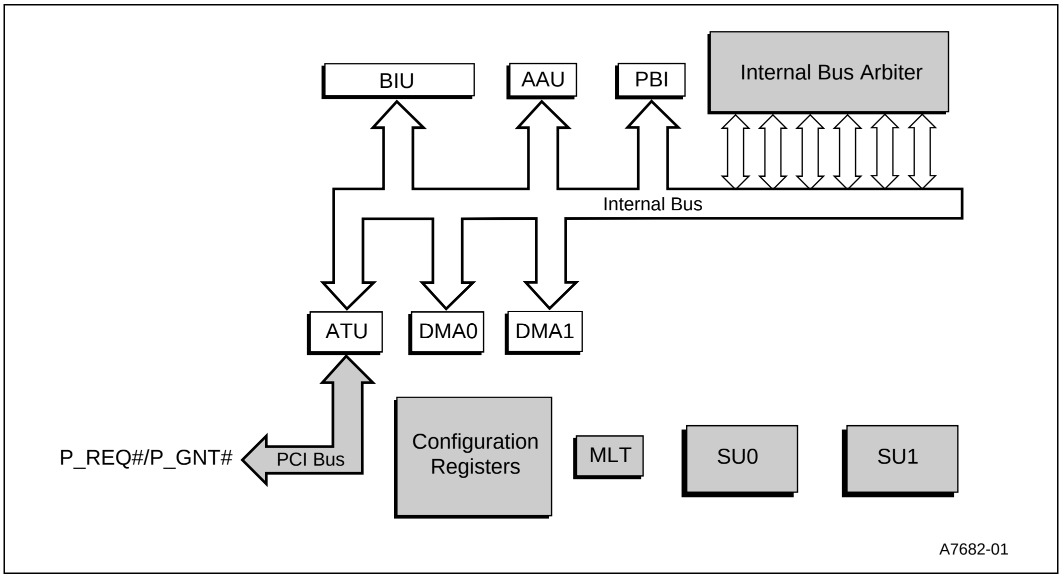


Figure 7. Intel® 80321 I/O Processor Arbitration Block Diagram



10.1 Intel® 80321 I/O Processor Arbitration Unit

10.1.1 Internal Bus Arbitrator

The 80321 has one PCI arbiter, the Internal Bus Arbiter (IABR).

- IARB: arbitrates between the six potential internal bus initiators (ATU, two DMA Channels, Application Accelerator, the PBI, and the Bus Interface Unit for the core).

The 80312 has a PCI Arbiter. The PCI Arbiter arbitrates between multiple PCI masters. The 80312 contains two PCI arbiters: Secondary PCI Arbiter (SARB) and Internal Bus Arbiter (IARB).

- The SARB arbitrates between six potential off-chip secondary PCI bus masters and the three 80312 secondary bus masters (Bridge, Secondary ATU, and DMA Channel 2).
- The IARB arbitrates between the eight potential internal bus masters (Primary and Secondary ATUs, three DMA channels, Messaging Unit, Application Accelerator and the Core Interface Unit for the 80200).

10.1.2 Master Latency Timer

PCI protocol requires each PCI initiator to use a master latency timer (MLT). The MLT counts PCI cycles an initiator uses in a single transaction. The timer defines the minimum time a PCI master may own the PCI bus. When the arbiter deasserts GNT# to the current initiator and the MLT expires, the initiator must relinquish the PCI bus.

The 80321 implements one MLT for the PCI bus.

The 80312 implements three MLTs:

- one each for the Primary PCI bus
- the Secondary PCI bus
- the Internal Bus

The following sections describe two registers that have been **DELETED**.

10.1.2.1 Secondary Arbitration Control Register - (SACR)

The bits in these registers were used to set the arbitration device that uses the secondary PCI bus. The 80321 does not have a bridge, therefore it does not have a secondary bus.

10.1.2.2 Master Latency Timer Register (MLTR)

Defines preload value for the Internal Bus Master Latency Timer. The preload is a 12-bit value. This register is part of the local arbitration configuration register space and is accessible from the 80200. This defines the time allowed for one transaction.

The 80312 contains one Multi-Transaction Timer Register, MTTR1. The 80321 contains two, MTTR1 and MTTR2 one for the Intel® XScale™ core and one for the internal bus agents other than the Intel® XScale™ core.

Table 14. New or Changed Arbitration Unit Registers in the Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
MTTR1	FFFF E784	98H	Multi-Transaction Timer 1 – Indicates the minimum number of clocks the Intel® XScale™ core is allowed to retain ownership of the Internal Bus across back-to-back transactions.
MTTR2	FFFF E788H	38H	Multi-Transaction Timer 2 – Indicates the minimum number of clocks internal bus agents other than the Intel® XScale™ core are allowed to retain ownership of the Internal Bus across back-to-back transactions.

Table 15. New or Changed Arbitration Unit Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
IACR.3:2	FFFF E780H	00	PBI Priority
IACR.9:8	FFFF E780H	00	Reserved
IACR.11:10	FFFF E780H	00	Intel® XScale™ core Priority

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 11.

11.0 Core Comparison

The primary difference between the Intel® XScale™ core of the 80321 and the 80200 is that the 80321 integrates the Intel® XScale™ core therefore, the 80321 Core Interface Unit (CIU) is internal.

Note: The CCLKCFG Register is now a Reserved register. The 80321 runs at either 400 MHz or 600 MHz and the CCLKCFG Register can no longer be used to change the operating frequency of the Intel® XScale™ core.

Coprocessor 6 (CP6) was added to handle the interrupt and timer functions.

The interface between the Intel® XScale™ core and the 80321, 64-bit internal bus, is the Bus Interface Unit (BIU). The BIU initiates bus cycles issued by the Intel® XScale™ core and sends them over the 80312, 64-bit internal bus, the PXBus. The BIU has one transaction queue with four entries. The BIU acts as a Master for all the read and write requests issued by the Intel® XScale™ core and acts as a Slave for split completion requests. All the BIU registers reside in Coprocessor 7 (CP7).

The BIU is reset:

- when P_RST# is asserted
- when the Intel® XScale™ core is reset

When reset, all four transaction buffers are marked as invalid.

Table 16. New or Changed Core Registers in the Core of the Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
BEAR	CP7, Register 0	0000 0000H	BIU Error Address Register – The BEAR is responsible for logging the addresses where errors were detected on the Internal Bus. One error can be detected and logged.
BIUSR	CP7, Register 4	0000 0000H	BIU Status Register – The BIUCR allows software to determine the cause of any BIU interrupts.

12.0 Timers

The 80321 contains two dual-programmable 32-bit timers and a Watch Dog Timer. Each timer is programmed by the timer registers. These registers are mapped into the Intel® XScale™ microarchitecture Coprocessor 6, registers 0 to 5. They may be accessed/manipulated with the MCR, MRC, STC, and LDC instructions. The *CRn* field of the instruction denotes the register number to be accessed. The *opcode_1* and *opcode_2* fields of the instruction are zero. The *CRm* field of the instruction are one. Most systems restricts access to CP6 to privileged processes. To control access to CP6, use the Coprocessor Access Register.

When enabled, a timer decrements the user-defined count value with each Timer Clock (TCLOCK) cycle. The countdown rate is also user-configurable to be equal to the core clock frequency, or the core clock rate divided by 4, 8 or 16. The timers can be programmed to either stop when the count value reaches zero (single-shot mode) or run continuously (auto-reload mode). When a timer count reaches zero, the timer interrupt unit signals the processor interrupt controller.

Table 17. Timer Input Clock (TCLOCK) Frequency Selection

Bit 5 TMRx.csell	Bit 4 TMRx.cse10	Timer Clock (TCLOCK)
0	0	Timer Clock = core clock
0	1	Timer Clock = core clock/4
1	0	Timer Clock = core clock/8
1	1	Timer Clock = core clock/16

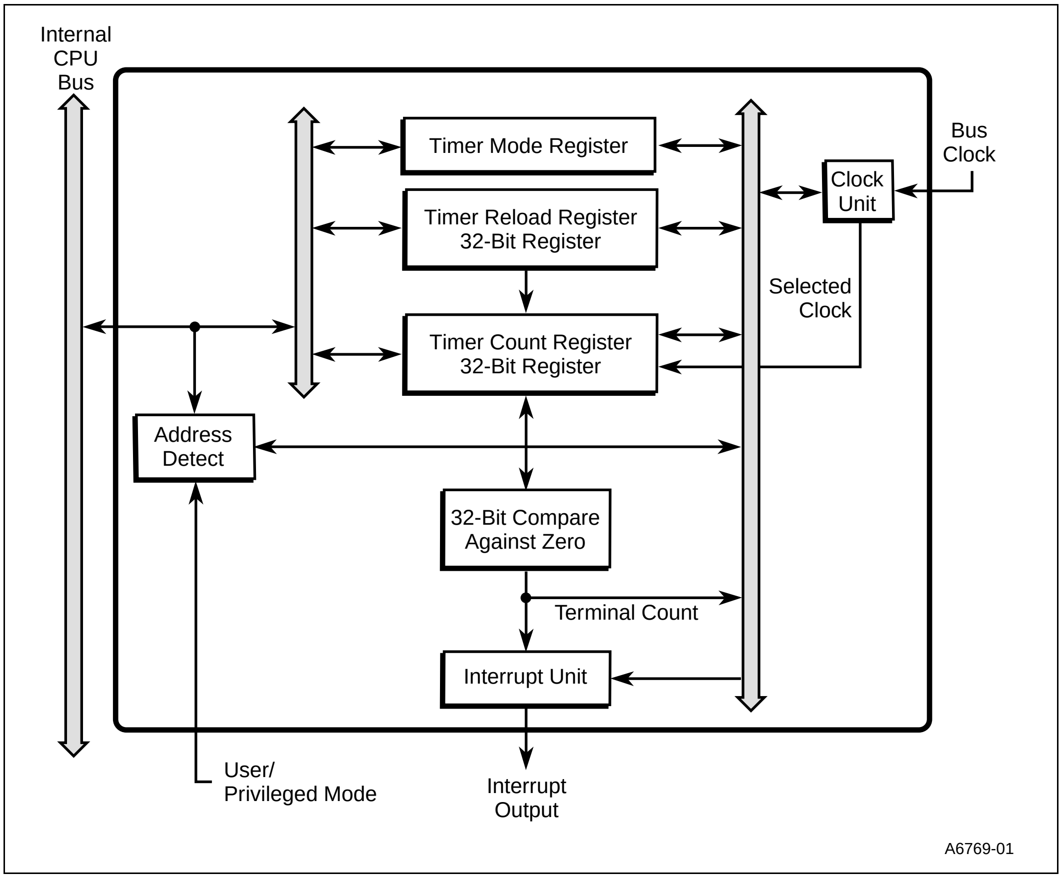
The processor clears these bits upon hardware or software reset (TCLOCK = Core Clock)

Table 18. Timer Performance Ranges

Core Frequency (MHz)	Maximum Resolution (ns)	Maximum Range (mins)
600	1.66	1.90

Figure 8 shows a diagram of the timer functions.

Figure 8. Programmable Timer Functional Diagram



See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 14.

13.0 Package and Ball Out

The 80321 uses a 544-lead PBGA package versus a 540-lead HL-PBGA package for the 80312. For a complete list of all pins, ball out and package dimensions, see the *Intel® 80321 I/O Processor Datasheet*. The 80321 has many of the same pin functions as the 80312 but several new pins have been added that are used to support product enhancements and several have been deleted as well. Table 19 through Table 23 show the new signals and the deleted signals.

Table 19. Memory Controller Signal

Pin	Description
RCVENI#	**RECEIVE ENABLE IN** provides delay information for enabling the input receivers and must be connected to RCVENO# of the 80321.
RCVENO#	RECEIVE ENABLE OUT must be connected to RCVENI# of the 80321 and be trace length matched to CLOCK TRACE + AVG. of the DQ[63:0] TRACES.
M_CK[2:0]	**MEMORY CLOCKS** are used to provide the positive differential clocks to the external SDRAM memory subsystem.
M_CK[2:0]#	**MEMORY CLOCKS** are used to provide the negative differential clocks to the SDRAM memory subsystem.
M_RST#	**MEMORY RESET** indicates when the memory subsystem has been reset with the P_RST# or a software reset.
DQS[8:0]	**SDRAM DATA STROBES** carry the strobe signals which are used to capture data on the data bus.
SDQM[8]	**SDRAM DATA MASK** controls which bytes on the data bus are written. When SDQM[8:0] is asserted, the SDRAM devices do not accept valid data from the byte lanes. SDQM[8] is the additional signal.
V_{REF}	**SDRAM VOLTAGE REFERENCE** is used to supply the reference voltage to the differential inputs of the memory controller pins.

Table 20. Peripheral Bus Interface Signals (Sheet 1 of 2)

Pin	Description
AD[31:0]	**ADDRESS/DATA BUS** During an address cycle 31-2 contain the physical word address and bits 1-0 specify the number of data transfers during the bus transaction. 00 = 1 Transfer 01 = 2 Transfers 10 = 3 Transfers 11 = 4 Transfers During a data cycle bits 31-0, 15-0 or 7-0 contain valid data depending on the corresponding 32-, 16- or 8-bit bus width. During 16- and 8-bit bus write operations the unused bus pins are driven to determinate values.
A[3:2]	**ADDRESS[3:2]** carry a demultiplexed version of bits 3 and 2 of the address bus. During an address cycle A[3:2] matches AD[3:2]. During bursted read or write data cycle a[3:2] represents the current DWORD address in the bursted transaction.
BE[3:0]	**BYTE ENABLES** select which of up to four data bytes in the bus participate in the current bus access. The byte enables are asserted during the address cycle. These signals do not toggle during a burst and they remain active through the last data cycle. Byte enable encoding is dependent on the bus width. See the *Intel® 80321 I/O Processor Datasheet* for more details.
ALE	**ADDRESS LATCH ENABLE** indicates the transfer of a physical address. The pin is asserted during the first address cycle and deasserted during the second address cycle. The pin floats whenever the bus us relinquished to an external device.
ADS#	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. The pin is asserted during the second address cycle and deasserted during the first data cycle. The pin floats whenever the bus is relinquished to an external device.
PB_CLK	**PERIPHERAL BUS CLOCK** us the references clock for all signals on the peripheral bus.
W/R#	**WRITE/READ** indicates whether the bus access is a write or a read with respect to the 80321 and is valid during the entire bus access.
WE#	**FLASH WRITE ENABLE** indicates whether the bus access is a write or a read with respect to the 80321 and is valid during the entire bus access. This pin is used for Flash memory accesses and controls the WE# input on the ROM.
DEN#	**DATA ENABLE** indicates data transfer cycles during a bus access. DEN# is asserted at the start of the first data cycle and deasserted at the end of the last data cycle.
BLAST#	**BURST LAST** indicates the last data transfer when a bus access. BLAST# remains active when wait states are inserted and becomes inactive after the final data transfer is complete.
RDYRCV#	**READY/RECOVER** During a data cycle the pin indicates that data can be sampled or removed. 0 = sample data 1 = insert wait state During a recover state the pin indicates that the recover state repeated, This function allows slow external devices longer to float their pins before the next address is driven. 0 = insert recovery state 1 = recovery complete
HOLD	**HOLD** is used by an external device to request access to the bus.
HOLDA	**HOLD ACKNOWLEDGE** indicates to an external device that it has been granted to the bus.
PB_RST#	**PERIPHERAL BUS RESET** indicates when the peripheral bus has been reset with P_RST# or a software reset.
PCE[5]#/ PBI100MHZ#	**PERIPHERAL CHIP ENABLES** specifies which of the six memory ranges are associated with the current bus access. The pin remains valid during the entire bus access. **PERIPHERAL BUS 100MHz ENABLE** is latched at the deasserting edge of P_RST# and it indicates the speed at which the PBI bus operas.
PCE[4]#/PBI66MHZ#	**PERIPHERAL CHIP ENABLES, PERIPHERAL BUS 66MHZ ENABLE** is latched at the deasserting edge of P_RST# and it indicates the speed at which the PBI bus operates.

Table 20. Peripheral Bus Interface Signals (Sheet 2 of 2)

Pin	Description
PCE[3]#/P_BOOT16#	**PERIPHERAL CHIP ENABLES, PERIPHERAL BUS BOOT WIDTH 16 ENABLE** specifies the width of the peripheral bus for Flash accesses during boot up.
PCE[2]#/32BITPCI#	**PERIPHERAL CHIP ENABLES, 32-BIT PCI** is latched at the deasserting edge of P_RST# and it indicates the width of the PCI-X bus to the PCI-X Status Register.
PCE[1]#/RETRY	**PERIPHERAL CHIP ENABLES, RETRY** is latched at the deasserting edge of P_RST# and it determines when the Primary PCI interface disables PCI configuration cycles by signaling a Retry until the Configuration Cycle Retry bit is cleared in the PCI Configuration and Status Register.
PCE[0]#/RST_MODE#	**PERIPHERAL CHIP ENABLES, RST_MODE** is latched at the deasserting edge of P_RST# and it determines when the 80321 is held is reset until the *Intel® XScale*™ microprocessor Reset bit is cleared in the PCI Configuration and Status Register.
WIDTH[1:0]	**WIDTH** denotes the physical memory attributes for a bus transaction. The pins float whenever the bus is relinquished to an external device.

Table 21. PCI Bus Signals

Pin	Description
P_LOCK#	REMOVED
Secondary PCI Bus Signals	REMOVED

Table 22. Serial Port Interface Signals

Pin	Description
SSCKO	**SERIAL PORT CLOCK OUT** is the output bit-rate clock.
SFRM	**SERIAL FRAME** indicates the beginning and end of a serial data word.
TXD	**TRANSMIT DATA** is the outbound serial data pin.
RXD	**RECEIVE DATA** is the inbound serial data pin.
SSCKI	**SERIAL PORT CLOCK IN** is the input bit-rate clock which can be used when a frequency other than the default of 3.7 MHz is needed.

Table 23. Miscellaneous Signals

Pin	Description
HPI	**HIGH PRIORITY INTERRUPT** causes a high priority non-maskable interrupt to the 80321. This pin is level detect only and is internally synchronized.
SDA0 and SDA1	I^{2}C **DATA** is used for data transfer and arbitration on the I^{2}C bus. One SDA pin is used for each I^{2}C bus. SDA0 and SDA1 are multiplexed with GPIO[6] and GPIO[4] respectively.
SCL0 and SCL1	I^{2}C **CLOCK** provides synchronous operation of the I^{2}C bus. One SCL pin is used for each I^{2}C bus. SCL0 and SCL1 are multiplexed with GPIO[7] and GPIO[5] respectively.
RCOMP	**RESISTOR COMPENSATION** is connected through a 30.1Ω 1% ¼ W resistor to ground. This is used to minimize the PCI pin variations due to voltage and temperature variations.
POR#	**POWER ON RESET** is used with an external RC circuit to provide clocks to the core during power.
Vcc33	**3.3 V POWER** balls to be connected to a 3.3 V power board plane.
Vcc25	**2.5 V POWER** balls to be connected to a 2.5 V power board plane.
Vcc13	**1.3 V POWER** balls to be connected to a 1.3 V power board plane.
I_RST#	REMOVED
VccPLL3	REMOVED
80200 Signals	REMOVED

14.0 Interrupt Controller and General Purpose I/O Unit (GPIO)

The 80321 Interrupt Controller Unit (ICU) provides the ability to generate interrupts to both the Intel® XScale™ core and the PCI bus.

14.1 Internal Interrupts

The 80321 Interrupt Controller Unit allows flexible routing of the external interrupts and internal interrupts to be directed to the two internal interrupt exceptions FIQ and IRQ. The internal interrupts include the following:

- DMA Channel 0
- DMA Channel 1
- I^{2}C Bus Interface Units 0 and 1
- Application Accelerator Unit
- Address Translation Unit, ATU
- Two Programmable Timers
- Messaging Unit
- SSP Serial Port Unit
- Memory Controller Unit
- Performance Monitoring Unit

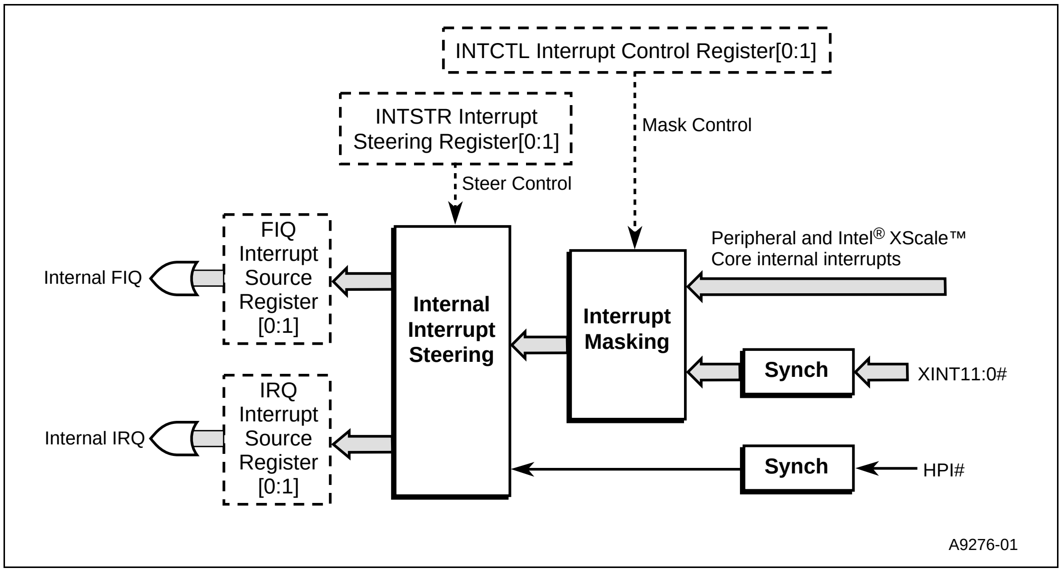
Software can also provide an interrupt generated from a SWI instruction.

14.2 External Interrupts

The 80321 has four external interrupts **XINT[3:0]#** and one external high priority interrupt HPI. Along with these external interrupts, the Peripheral Interrupt Controller provides the ability to direct PCI interrupts. The routing logic enables, under software control, the ability to intercept external PCI interrupts and forward to the PCI interrupt pins, **P_INTA#**, **P_INTB#**, **P_INTC#**, and **P_INTD#** output pins or to the Intel® XScale™ core.

The 80321 registers allows a flexible routing of the external interrupts and internal interrupts to be directed to the two internal interrupt exceptions FIQ and IRQ as shown in the below diagram.

Figure 9. Interrupt Routing



For the 80321 reference implementation board, HPI interrupt is connected to PCI signal SERR# and XINT[1:0] are connected to PCI Bus interrupts INTB, INTA respectively. The reference board makes use of XINT[3:2] to allow other peripheral devices to interrupt the 80321. The 80321 registers allow a flexible routing of the external interrupts and interrupts to be directed to the two internal interrupt exceptions FIQ and IRQ.

14.3 Generating External PCI Interrupts From Internal Source

The Messaging Unit (MU) has the capability of generating interrupts on the PCI interrupt output pins. The MU has four distinct messaging mechanisms. Each allows a host processor or external PCI agent and the 80321 to communicate through message passing and interrupt generation. The four mechanisms are:

- **Message Registers —** allow the 80321 and external PCI agents to communicated by passing messages in one of four 32-bit Message Registers. In this context, a message is any 32-bit data value. Message registers combine aspects of mailbox registers and doorbell registers. Writes to the message registers may optionally cause interrupts.

- **Doorbell Registers —** allow the 80321 to assert the PCI interrupt signals and allow external PCI agents to generate an interrupt to the Intel® XScale™ core.

- **Circular Queues —** support a message passing scheme that uses four circular queues.

- **Index Registers —** support a message passing scheme that uses a portion of the 80321 local memory to implement a large set of message registers.

All four mechanisms can result in Outbound Interrupts to a host processor on the **P_INT[A:D]#** output pins.

14.4 General Purpose Input/Output Support

Eight pins are provided as General Purpose Input Output (GPIO) pins. The eight pins are **GPIO[7:0**]. These pins can be used by the Intel® XScale™ core to control or monitor external devices in the I/O subsystem. The interface for the two I^2C serial ports are multiplexed on to **GPIO[7:4**]. When I^2C port 0 is enabled (Bit 6 of ICR0 is set), **GPIO7** functions as **SCL0** while **GPIO6** functions as **SDA0.** When I^2C port 1 is enabled (Bit 6 of ICR1 is set), **GPIO5** functions as **SCL1** while **GPIO4** functions as **SDA1.**

When an I^2C port is enabled, the GPIO functionality described in the following sections is not available on the associated pins. I^2C ports are disabled following system reset.

14.4.1 General Purpose Inputs

The current state of the eight GPIO pins can be read in “GPIO Input Data Register - GPID”.

14.4.2 General Purpose Outputs

The output function of the GPIO pins is controlled by two registers, “GPIO Output Data Register GPOD” and “GPIO Output Enable Register - GPOE”. The output enables are mapped on a per bit basis to each of the data bits in the GPIO Output Data Register. When a bit of the GPIO Output Enable Register is cleared, the corresponding data bit value in the GPIO Output Data Register is actively driven on the appropriate GPIO pin.

14.4.3 Reset Initialization of GPIO Function

Both the GPIO Output Data Register and the GPIO Input Data Register is initialized to 00H upon assertion of **P_RST#**.

Several 80312 registers have been deleted and replaced with the registers in the table below. The function of the FIQ1ISR and FIQ2ISR registers of the 80312 have been incorporated into the FINTSRC register of the 80321. The function of the IRQISR have been incorporated into the INTSRC register.

Table 24. New/Changed Interrupt Controller and GPIO Unit Registers in Intel® 80321 I/O Processor

Register Name	Internal Bus Address	Default Value	Register Description
INTCTL	FFFF E7D0H	0000 0000H	Interrupt Control Register – a 32-bit Coprocessor 6 control register, register 0, used to specify which interrupts are masked.
INTSTR	FFFF E7D4H	0000 0000H	Interrupt Steering Register – a 32-bit Coprocessor 6 control register, register 4, allows system designers to direct any of the internal or external interrupt sources to either one of the two internal interrupt exceptions, FIQ and IRQ.
INTSRC	FFFF E7D8H	0000 0000H	IRQ Interrupt Source Register – a 32-bit Coprocessor 6 control register, register 8, used to specify which interrupts that are steered to the internal IRQ exception are active.
FINTSRC	FFFF E&DCH	0000 0000H	FIQ Interrupt Source Register – a 32-bit Coprocessor 6 control register, register 9, used to specify which interrupts that are steered to the internal FIQ exception are active.

Table 25. New or Changed Bit Functions of the GPIO Pins for the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
GPOE	FFFF E7C4H	FFH	GPIO Output Enable Register

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 15.

15.0 Peripheral Performance Monitoring Unit - PPMON

The features of the PPMON aid in measuring and monitoring various system parameters that contribute to the overall performance of the processor. The monitoring facility is generically referred to as PPMON – Peripheral Performance Monitoring. The facility is model specific, not architecture; its intended use is to gather performance measurements that can be used to retune/refine code for better system performance.

Events monitored on the 80321 can either be duration events or occurrence events. There are 57 events monitored and five monitoring modes implemented on the 80321. The 80312 has the capability of monitoring 98 events and has ten monitoring modes implemented.

Performance metrics for the Intel® XScale™ core are tracked by the CPMON – Core Performance Monitoring unit. For more details of the CPMON, see *Intel® 80321 I/O Processor Developer's Manual*, Chapter 12.

Table 26. New or Changed PPMON Bit Functions in the Intel® 80321 I/O Processor

Bit Position	Internal Bus Address	Default Value	Bit Function
ESR.3	FFFF E704H	0	This bit along with bits 2:0 are used to determine the monitored interface on the 80321. This bit is no longer Reserved.
PECRx.0	FFFF E714H – FFFF E748H	X	This bit along with bits 31:1 when accessed, return the current count value in the respective event counter. This bit is no longer Reserved.

See *Intel® 80321 I/O Processor Developer's Manual*, Chapter 16.

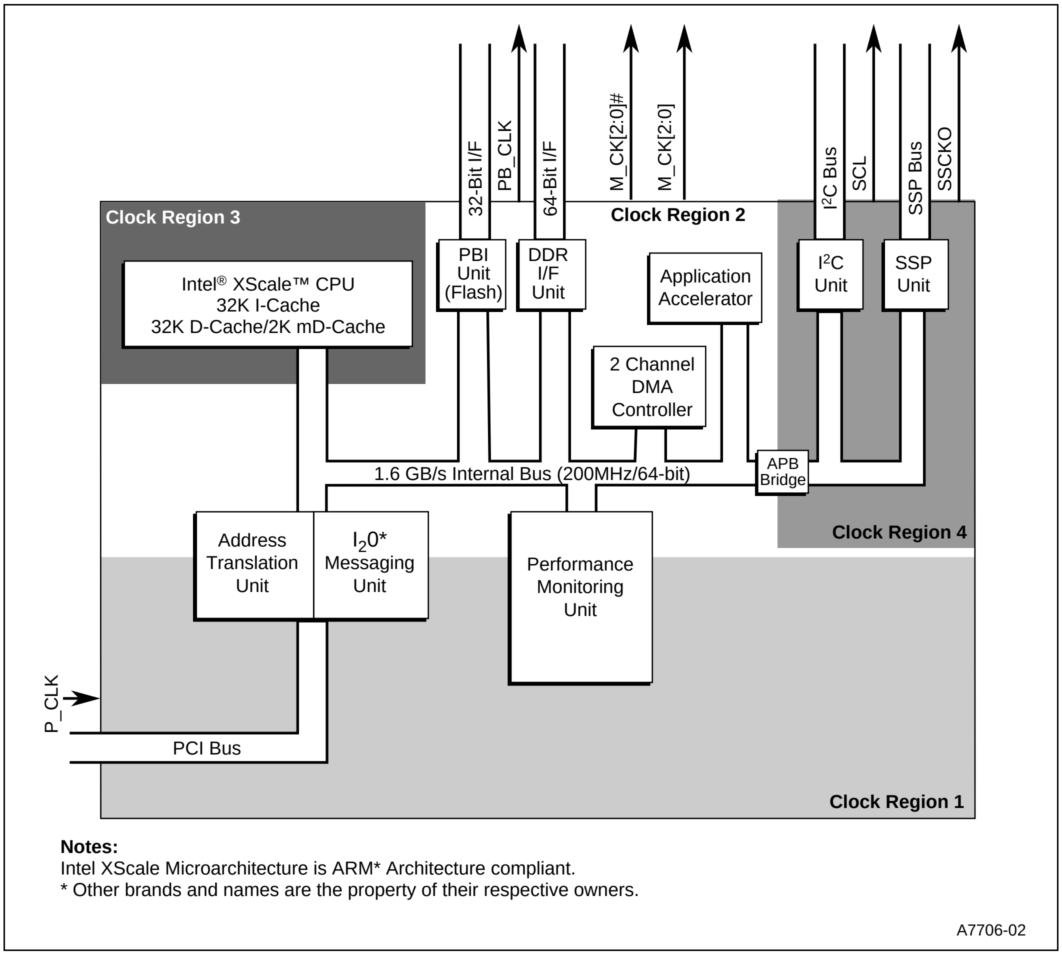
16.0 Clocking and Reset

This chapter provides information on the different clocking domains of the 80321.

16.1 Clocking Theory of Operation

Each region within the 80321 contains different clocking requirements. These regions are shown in Figure 10. These requirements are summarized in the following sections.

Figure 10. Intel® 80321 I/O Processor Clock Generation Unit



Notes:
Intel XScale Microarchitecture is ARM* Architecture compliant.
* Other brands and names are the property of their respective owners.

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16.2 Clocking Region 1

Region 1, contains the main input clock for providing the 80321 with all of its clock sources. This input clock, called the PCI bus clock, is connected to the input pin **P_CLK** and is provided by the system designer. The 80321 supports an input frequency of 33 MHz, 66 MHz, 100 MHz, or 133 MHz for normal operation on the PCI interface. For the 80321, region 1 obtains its input clock as a buffered version of **P_CLK**.

16.3 Clocking Region 2

Region 2, obtains its input clock from the clocking unit specified in clocking region 1. This region is the 80321 internal bus. It supports clock frequencies up to 200 MHz. The clocking unit provides six DDR SDRAM output clocks, based on a dedicated PLL. The clocking unit contains three output clocks, called **M_CK[2:0]**, and three complement clock outputs called **M_CK[2:0]#**. The **M_CK[2:0]** and **M_CK[2:0]#** outputs are used by the DDR SDRAM memory subsystem. Also, region 2 generates an output clock called **PB_CLK** for Peripheral bus interface. **PB_CLK** operation can range from 33 MHz to 100 MHz. Refer to Section 16.0, “Clocking and Reset” on page 41 of this document for more guidelines on routing the clocks.

16.4 Clocking Region 3

Region 3, obtains its input clock from the clocking unit specified in clocking region 1. This region is the Intel® XScale™ core. It supports clock frequencies up to a maximum of 600 MHz operation.

16.5 Clocking Region 4

Region 4, obtains its input clock from the clocking unit specified in clocking region 1. This region is for use by low-speed peripheral units. Currently, these include the I^2C bus interface and the SSP Serial Bus Interface. It supports clock frequencies up to a maximum of 100 MHz operation. The region 4 clock is an integer multiple of the **P_CLK**.

Region 4, contains an output clock SCL used for the I^2C bus interface. The SCL clock frequency for I^2C operation is 100 KHz or 400 KHz. SCL is generated from the internal bus clock. In order to use the I^2C interface, a clock divider value must be written into the I^2C Clock Count Register.

Region 4, contains an output clock **SSCKO** used for the SSP Serial bus interface. The **SSCKO** clock frequency is determined by the SSP Serial Bus operating mode. **SSCKO** is generated from the internal bus clock.

16.6 Output Clocks

Refer to the PC1600 DDR Unbuffered DIMM Specification for the clock skew and loading requirements for the DDR SDRAM devices and section. Refer to the *PCI Local Bus Specification*, Revision 2.2 (e.g., 33 MHz, 66 MHz) and the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 1.0a (e.g., 66 MHz, 100 MHz, 133 MHz) for details on PCI bus clock loading requirements.

See *Intel® 80321 I/O Processor Developer’s Manual*, Chapter 18.

17.0 Peripheral Memory-Mapped Registers (PMMR)

The PMMRs have moved from address range 0000 1000H – 0000 1900H on the 80312 (80312) to FFFF E000 – FFFF E8FFH on the 80321. Because of this, peripheral registers have different Internal Bus addresses equal to the difference in the offset of the PMMR address range, FFFF D000H. Figure 11 and Figure 12 illustrates this difference. Please see Table 3 for the new and changed PMMRs.

Figure 11. Intel® 80310 I/O Processor Chipset Address Space

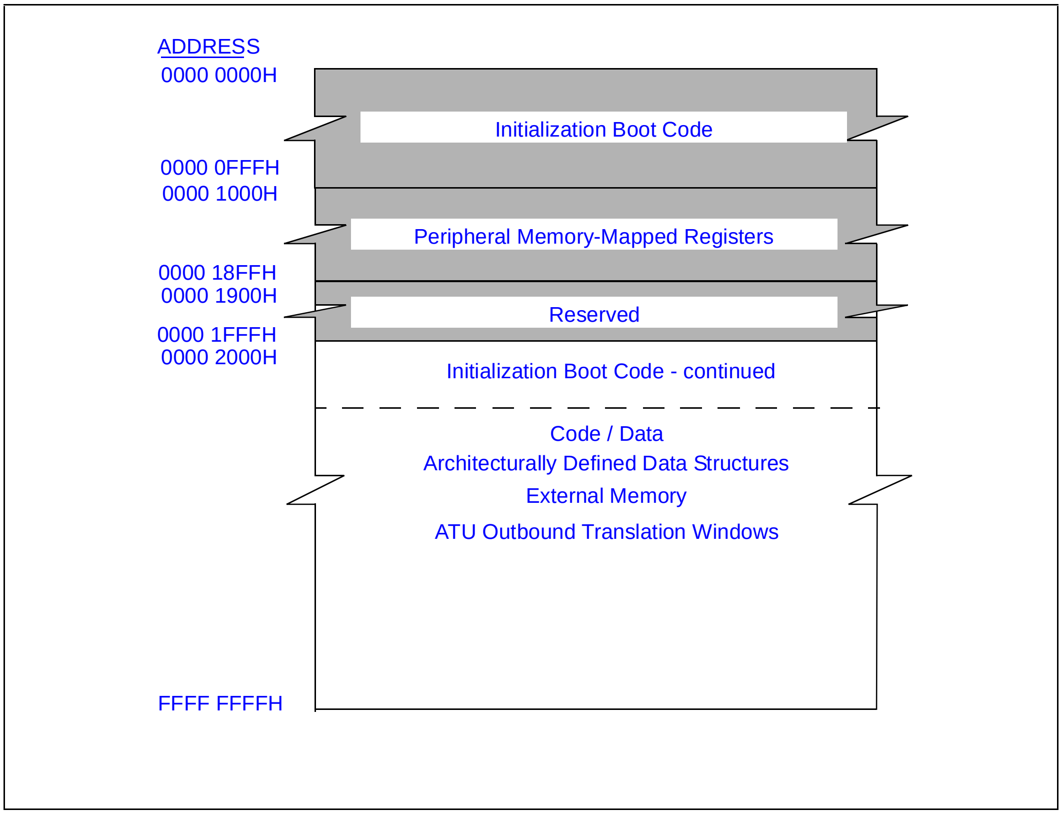
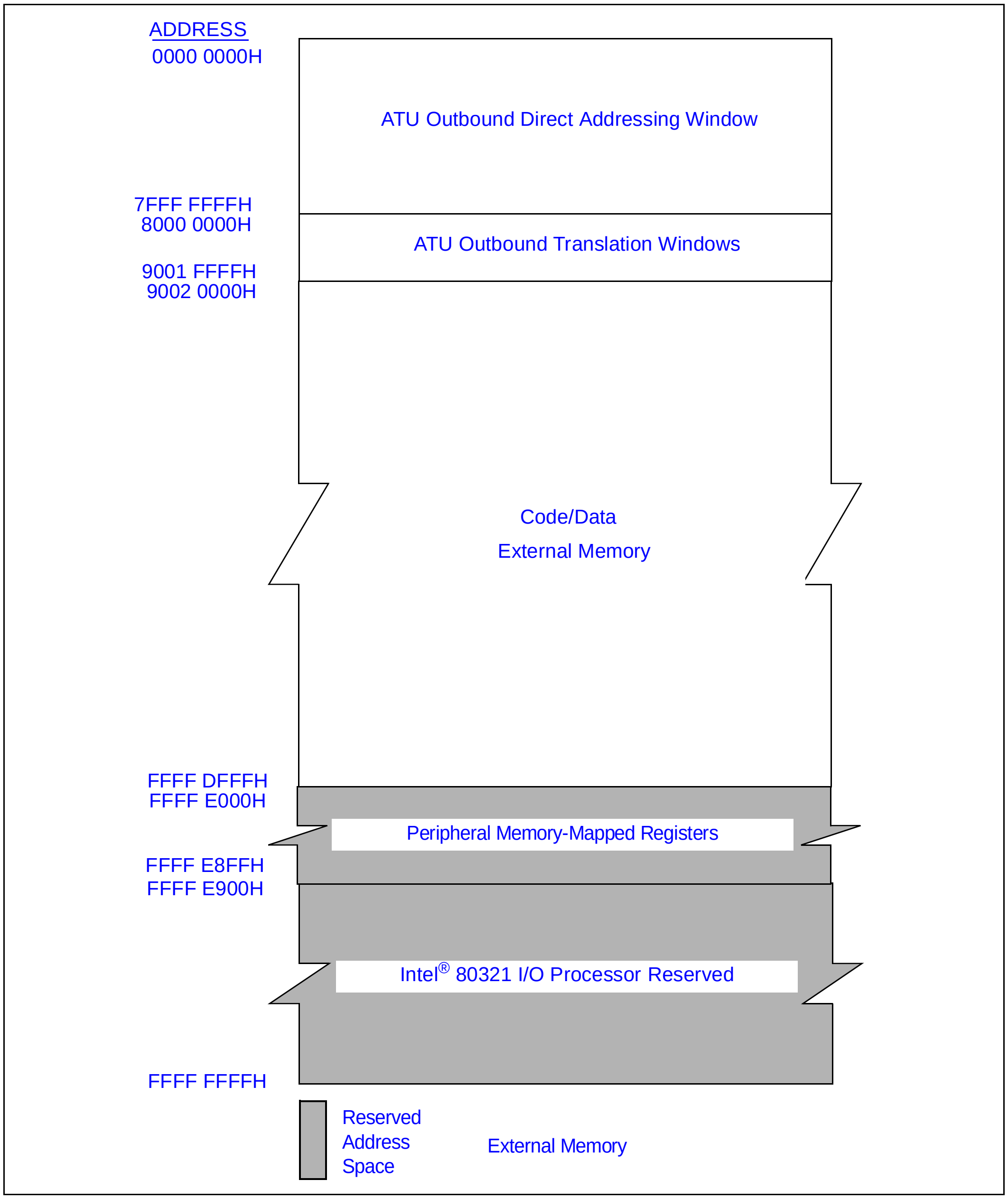


Figure 12 shows the Intel® XScale™ core address space and addresses available to the applications.

Figure 12. Intel® 80321 I/O Processor Address Space



See the *Intel® 80321 I/O Processor Developer's Manual*, Chapter 17.