

# Intel® Media Processor CE 3100

## Errata Update

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*July, 2008*

*Revision 1.6*

Reference Number: E51472-001

**Notice:** The Intel® Media Processor CE 3100 component may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Errata Update.

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# Revision History

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Date	Revision	Reference #	Description
3/12/2008	1.0	24806	Initial document
5/15/2008	1.1	25086	Errata through May, 2008
6/16/2008	1.5	25226	Added Errata section for B step silicon
7/22/2008	1.6		Update errata and spec. information. Initial Public release.

# Preface

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This document is an update to all the Intel® Media Processor CE 3100 silicon bugs visible to the customer. It contains Errata and Specification Clarifications for the Intel® Media Processor CE 3100 SKUs.

## Nomenclature

**Errata** are design defects or errors. Errata may cause the behavior of the Intel® Media Processor CE 3100 to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

## Component Identification via Programming Interface

The Intel® Media Processor CE 3100 may be identified by the following register contents:

Stepping <sup>1</sup>	Revision ID <sup>2</sup>
A0	0000h
B0	0002h

**Notes:**

1. The Stepping number corresponds to bits 3-0 of the ID Register.
2. The Revision ID corresponds to bits 7-0 of the ID Register in the PCI Header.

# Component Marking Information

The Intel® Media Processor CE 3100 is also identified by the following component markings:

Stepping	Top Marking	Notes
A0	Canmore	Engineering Sample Canmore
B0	Canmore	Engineering Sample Canmore

# Summary of Changes

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The following subsections indicate the Errata and Specification Clarifications that apply to the Intel® Media Processor CE 3100, stepping A. Intel® intends to fix some of the errata in a future stepping of the component and to account for the other outstanding issues through documentation or Specification Changes as noted. This summary uses the following notations:

## Codes Used in Summary

o X:	o Erratum, Specification Change, or Clarification that applies to this stepping
o Doc:	o Document change or update that will be implemented
o Fix:	o This erratum is intended to be fixed in a future stepping of the component.
o Fixed:	o This erratum has been previously fixed.
o NoFix:	o There are no plans to fix this erratum.
o (No mark) or (Blank Box):	o This erratum is fixed in listed stepping, or specification change does not apply to listed stepping.
o Shaded:	o This item is either new or modified from the previous version of the document.

# Errata – A Step

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## 1. **PCIE Link Training not working.**

**Problem:** Link Training State Machine transitions from DETECT.QUIET to DETECT.ACTIVE and back repeating indefinitely. No data is seen on TX or RX bits.

**Implication:** N/A.

**Workaround:** Board design workaround. Add pull down 2.1K resistors on the transmitter side to ground before the decoupling capacitor. One 2.1K for TXN and one 2.1k for TXP.

**Status:** No Fix in B-step.

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## 2. **HDMI I2C device not driving SCL.**

**Problem:** The HDMI controller begins an I2C transaction that never completes. After the START condition, the SCL only pulses low once while SDA stays low for the entire scope capture length. Segment pointer address never starts.

**Implication:** N/A.

**Workaround:** Use I2C0 as HDMI I2C with stuffing resistor on board design\*.

**Status:** Fix in B0-step.

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## **Note**

For customers to building boards with A0 silicon, Intel® advises that a provision is made for HDMI I<sup>2</sup>C with stuffing resistors to route these signals to the DDC. In this case, the board can support HDMI I<sup>2</sup>C with B0 silicon.

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## 3. **USB Hub can not be supported.**

**Problem:** USB hub 1.1 and 2.0 does not identify USB devices attached to the hub.

**Implication:** A-step can not support USB hub.

**Workaround:** N/A.

**Status:** Fixed in B0-step.

---

**4. SATA only supports 64B burst size.**

**Problem:** DMA burst size bigger than 64B will result in a system hang.

**Implication:** N/A.

**Workaround:** Keep DMA burst size to 64B.

**Status:** No Fix in B-step.

---

**5. SD and ED bi-level sync slew rate failure.**

**Problem:** Both TV encoders bi-level sync slew rate too fast at SD and ED resolutions. Sync rise is a little faster than fall.

**Implication:** Failure is seen on VM5000/VM6000.

**Workaround:** No

**Status:** No Fix in B-step.

---

**6. PCIe TX eye does not meet specification.**

**Problem:** The PCIe eye pattern shows that the signals pass on amplitude but fail on width, to PCIE electrical specification.

**Implication:** N/A

**Workaround:** Intel recommends using on-board 50MHz oscillator for HPLL.

**Status:** Under Investigation.

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**7. PCI devices BARs are not PCI compliant.**

**Problem:** Linux\* expects that BAR spaces are able to return the size of a device's memory region or IO region by writing 0 to the BAR. PCI devices do not allow this, as the registers are write only.

**Implication:** PCI enumeration has issue.

**Workaround:** Software patch release in PR4.

**Status:** No Fix in B-step.

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**8. UART input clock is faster than what standard Linux expects.**

**Problem:** The reference clock being supplied to the UART is 14.7456MHz. Standard Linux expects a 1.832MHz clock.

**Implication:** This speed is 8x faster than what standard Linux i386 expects.

**Workaround:** Software workaround.

**Status:** No Fix in B-step.

---

**9. USB BAR does not comply with EHCI specification.**

**Problem:** USB BASE address is not correct which results in the Linux EHCI driver no being able to obtain the EHCI register's information.

**Implication:** A software workaround is required for the Linux driver to work.

**Workaround:** Software workaround.

**Status:** No Fix in B-step.

---

**10. SATA is not supported by the Linux driver.**

**Problem:** The SATA PCI header does not confirm completely to be PCI compatible and hence has issues supporting the Linux driver.

**Implication:** A software workaround is required for the Linux driver to work.

**Workaround:** Software workaround.

**Status:** No Fix in B-step.

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**11. SATA memory mapped PCI header is wrong.**

**Problem:** Device ID and the memory mapped PCI configuration header are not correct.

**Implication:** A software workaround is required for the Linux driver to work.

**Workaround:** Software workaround.

**Status:** No Fix in B-step.

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**12. HDMI can not support 1080i/p deep color mode.**

**Problem:** The packing phase signals are incorrect in the non working case, which results in HACTIVE coming in 1 pixel less for 1080i and 1080p in 30 bit mode.

**Implication:** A-step can not support deep color mode.

**Workaround:** N/A

**Status:** Fixed in B0-step.

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**13. Boundary Scan function is disabled.**

**Problem:** The Boundary Scan function is disabled in A0 silicon. There is no plan to enable this function in B0 silicon.

**Implication:** Customer can not run Boundary Scan for the Intel® Media Processor CE 3100 product.

**Workaround:** N/A

**Status:** No Fix in B-step.

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**14. SCH Phase does not meet the expected rate.**

**Problem:** PAL SCH (SubCarrier to Horizontal) phase does not meet the expected rate.

**Implication:** Failure is seen on VM700.

**Workaround:** N/A

**Status:** No Fix in B-step.

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**15. BT601/BT709 TV Encoder Pass-through.**

**Problem:** The TV encoder with pass through Color Space Conversion (CSC) does not produce the correct colors on output.

**Implication:** Failure will be seen on VM5000/VM700.

**Workaround:** N/A

**Status:** Fix in B0-step.

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**16. Bunit Cache Corrupts Graphics Driver Memory.**

**Problem:** Bunit caches CPU uncacheable memory, which causes a communication issue between the graphic driver and graphic engine hardware.

**Implication:** Graphics driver hangs but the rest of the system will continue to be responsive.

**Workaround:** Partial software workaround.

**Status:** No Fix in B-step.

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**17. UART1 TXD has issue when muxing with GPIO \_AUX6.**

**Problem:** Pin Muxing implementation for UART1\_TXD/GPIO\_AUX6 is not fully functional.

**Implication:** When only one of the two UARTs is active, the issue occurs.

**Workaround:** Both UARTs should be enabled in SW.

**Status:** Fix in B0 step.

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**18. SATA NCQ is not functional.**

**Problem:** When the SATA controller enables NCQ (Native Command Queuing) function support, there will be errors for read/write operations.

**Implication:** The testing data shows performance measurement NCQ performance can vary from 2~10%.

**Workaround:** SW workaround to disable NCQ support

**Status:** Under investigation.

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 **Note**

Since SATA NCQ is not functional on the Intel® Media Processor CE 3100, the test data collected in implication is based on previous ICH6 performance tests. The test data based on the Intel® Media Processor CE 3100is under investigation.

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**19. USB handshake timeout.**

**Problem:** When Linux kernel initializes the USB controller, EHCI\_HALT call handshake() to wait for STS\_HALT bit being set. This bit is not set even after timeout, which results in error information for the handshake function.

**Implication:** USB system will not work without SW workaround.

**Workaround:** SW workaround in EHCI\_HALT function to ignore the error message from the handshake function.

**Status:** Under investigation.

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## 20. MFD VC1 Pixel Mismatches on high BW clip.

- Problem:** Replication of some of the reference pixel rows at the top and bottom of the reference frame may be performed incorrectly under the rare occurrence that the current frame is a B-VOP AND the current frame is progressively coded
- One reference frame must be coded as frame-interlaced and the other as progressive
  - The current macroblock must be coded as direct or interpolated
  - The motion vector must be such that part of the reference macroblock is outside of a reference picture boundary.

This incorrect replication results in predicted pixel data at the top and bottom of a frame being incorrect.

- Implication:** The effect will be minor corruption in the bottom pixel rows of macroblocks at the bottom of the displayed frame or in the top pixel rows of macroblocks at the top of the displayed frame. In some cases the corruption may not be observed in the displayed frame because the bottom 8 rows of the decoded frame are not displayed. In other cases, the corruption will be minor because the rows that are replicated are the 2 bottom pixel rows and 2 top pixel rows of an interlaced frame, which most often are very similar to each other. In addition, the macroblock is a direct or interpolated type, which means an average value is taken between the forward and backward reference pixels. This corruption will be restricted to the current decoded frame; it will not propagate to other frames as the B-VOP can not be used as a reference frame.

**Workaround:** N/A

**Status:** No Fix in B-step.

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## 21. DPE soft reset causes hang.

- Problem:** When DPE\_CP does a software reset, the async FIFO in the DPE\_DMA (write slave only) resets its write pointer but its read pointer causes the async FIFO to output an unwanted FIFO\_not\_empty. This caused the output data FIFO to read garbage from async\_.

**Implication:** Running multiple DPE tests when doing DPE soft reset, DPE hangs. Read and write to DPE registers is still working but DPE does not respond.

**Workaround:** Software workaround is available.

**Status:** Fix in B0-step.

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**22. CPU reading from Linux provides different CPU speed for different boards.**

**Problem:** Due to two signals input to Preset and Reset pins of the 8254 timer flop are from different clock domains, this cause the synthesized issue. The async path causes a race condition to be happened and the value can change based on clock skew.

**Implication:** N/A.

**Workaround:** Software patch is added for Linux kernel.

**Status:** No Fix in B-step.

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# Errata – B Step

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## 1. High speed USB not functional.

**Problem:** High speed USB devices exhibit read errors when connected and thus are not recognized by the platform with B0 silicon. USB circuit does not perform Rx data recovery correctly.

**Implication:** With SW workaround, USB 2.0 high speed device is downgraded to be full speed device to be supported.

**Workaround:** N/A.

**Status:** Fixed in B1 Step.

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## 2. PAL WSS errors.

**Problem:** Active video overwrites PAL Wide-Screen Signaling (WSS) data on both TV encoders. To support using WSS for PAL on display pipe B, the vertical blank interval has been increased by 1 line per field. This workaround for WSS causes VM6000 errors because two extra vblank interval lines are being reported. Since HDMI and component use the same timings while connected to pipe A, WSS will not work on component interface at 576i resolution while using Pipe A.

**Implication:** PAL (576i) WSS does not work when analog component is output from pipe A.

**Workaround:** Switch component TV Encoder to Pipe B when component 576i is required.

**Status:** No fix in B1-step.

---

## 3. Color- Space can not convert correctly for RGB content with pre-multiplied alpha.

**Problem:** Due to a Graphic architecture limitation, VDC can not correctly color-space convert RGB content (to BT601 or BT709 color-space) that has pre-multiplied alpha in it.

**Implication:** A plane with pre-multiplied alpha will not be correctly blended if the connected pip's output color space is not RGB.

**Workaround:** No software workaround possible

**Status:** Under investigation.

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#### 4. **Unable to change CPU core/ratio on B0 silicon.**

**Problem:** On the Intel® Media Processor CE 3100 B0, the CPU-internal FSB ratio setting can NOT be overridden via platform straps.

**Implication:** The capability was put in to ease post Si validation. Because of this issue, dedicated system has to be used to validate the various settings. This issue does not impact customers.

**Workaround:** N/A

**Status:** Not fixed in B-1 step.

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#### 5. **SEC FW does not free AES cipher after processing the WrapFlashKey command.**

**Problem:** When sec\_wrap\_flash\_key function is invoked from an application, the SEC FW has a glitch where the following AES operations are not usable until the Intel® Media Processor CE 3100 is rebooted.

**Implication:** This command is only used when updating the Stage 1 boot loader, which will only happen in the manufacturing flow and possibly during an S1 boot loader field update. In both cases, it is highly probably that a reboot will occur after this command is executed. We do not foresee any impact of this issue in a running system.

**Workaround:** Reboot the system after using WrapFlashKey function

**Status:** No fix in B1-step.

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#### 6. **USB2.0 High Speed has errors with specific flash drives on the Intel® Media Processor CE 3100 B1 silicon.**

**Problem:** B1 silicon shows failures during high speed file transfer with two specific USB2.0 flash drives. These two devices are 4GB Corsair Flash Voyager and 32GB OCZ Rally 2. Intel has tested other density flash drives from the same vendors and the devices work fine. Among the vendors and densities Intel have tested with, these two flash drives, 4GB Corsair Flash Voyager and 32GB OCZ Rally 2, exhibit the failures.

**Implication:** Some USB2.0 high speed devices may not work with the Intel® Media Processor CE 3100. Potentially, there could be more USB2.0 high speed devices to be failed with the Intel® Media Processor CE 3100 when doing high speed file transfer.

**Workaround:** N/A.

**Status:** Under investigation.

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#### **Note**

Intel have not done compatibility testing on USB 2.0 high speed function with all available USB2.0 high speed flash drives in the market.

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## 7. HDMI potentially failed in 1080p 36-bit deep color mod

**Problem:** Long trace lengths can lead to excessive clock and data jitter resulting in potential eye diagram failures for 1080p 36-bit (deep color) modes for 59.94Hz.

**Implication:** Inability to pass HDMI certification test

**Workaround:** Keep the HDMI signal traces no longer than 4", fine tune the HDMI TX drive strength and efficiency settings to best fit the board implementation. Also, recommended is use of a 27MHz high precision oscillator for the AVPLL input instead of a crystal

**Status:** Under investigation.

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## 8. HDMI YUV422 output is not correct.

**Problem:** HDMI YUV422 output color is incorrect in pixel repetition modes (480i/576i). This issue is only in YUV 4:2:2 480i/576i. YUV 4:2:2 in 480p/720p/1080i mode works fine.

**Implication:** HDMI YUV422 output failed in 480i/576i mode.

**Workaround:** N/A

**Status:** Under investigation.

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### Note

This issue does not impact HDMI Certification with either YCbCr444 or YCbCr422 passing the tests. In this case, the product can be specified "Yes(YcbCr 4:4:4)" to confirm the product transmit an HDMI video signal using YCbCr (4:4:4 or 4:2:2) pixel encoding under some conditions in the Capability Declaration Form (CDF) for certification.

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# Specification Clarifications

## 1. Add pin D3 as a redundant pin to pin E1 as EXP\_DA[2].

**Problem:** To improve the solder joint reliability for the particular location, A-step pin D3, which is NC, will be Exp\_DA[2].

**Implication:** D3 is a redundant pin to pin E1 as Exp\_DA[2].

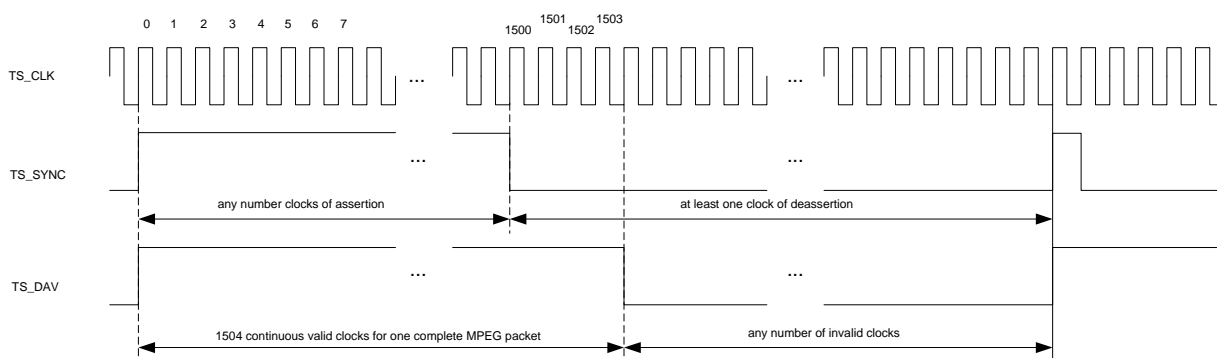
**Workaround:** Connect Pin D3 with Pin E1 in the design.

**Status:** Implement in B-step.

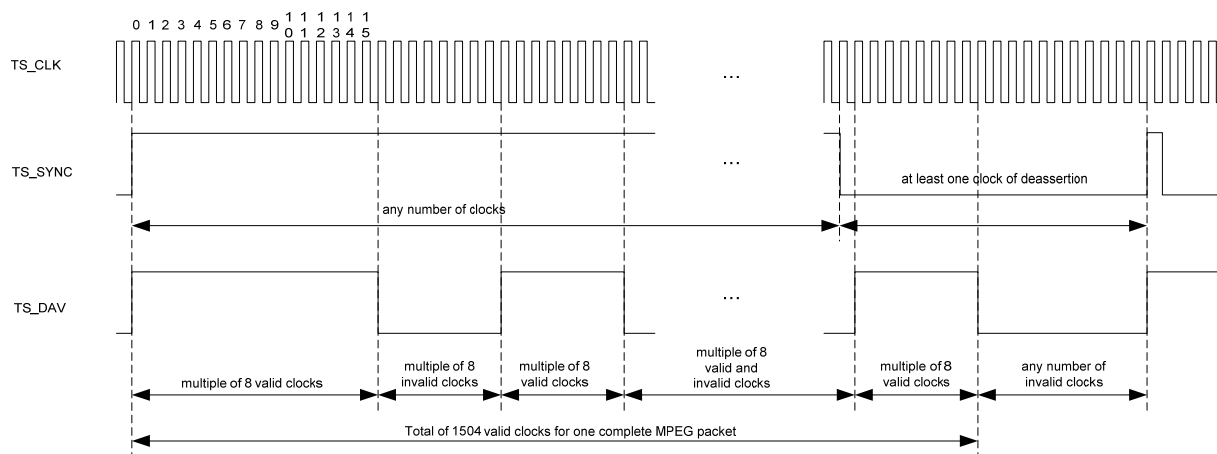
## 2. Transport Stream Timing Requirements:

Transport Stream devices must conform to the Intel® Media Processor CE 3100 required timing specs. Below are the timing diagrams that can be supported.

**Figure 1. Serial Transport Interface Timing with Continuous DAV**



**Figure 2. Serial Transport Interface Timing with Discontinuous DAV**



Note: Devices connected to the Intel® Media Processor CE 3100 serial transport stream input must conform to the timing specifications of the device. The Intel® Media Processor CE 3100 TS Input requires an even byte number of clocks for the 188 byte packet, and expects the data to be byte-aligned. Please refer to EMTS (Electrical Mechanical Thermal Specification) for detail information.